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Design of Low power Area efficient Data Comparator using Multiplexers

[1] J KRISHNA CHAITANYA, [2] K V HAREESH

[1]Student, [2] Asst. Professor

[1]Electronics and Communication Engineering,

[1]MLEC, Singarayakonda, India

Abstract: Data comparators are key arithmetic units used in digital systems to know whether two numbers are equal, or one number is less than or greater than other number. In this work a novel Area and power efficient multiplexer based Data comparator is proposed. The proposed method uses multiplexer to implement borrow equation in a full subtractor .which acts as a elementary processing element of a Data Comparator. The proposed designs are implemented in Dsch tool for gate level designs of AND gate ,OR gate, Multiplexer, Barrow generation unit and high and low value output units and verilog file is generated . Microwind tool is used to get layouts for different Models of Mosfet and different technologies. The moderations in the existing borrow equation of a full subtractor using multiplexer only resulted in reduced number of transistors with lower power. It was found that a 8 bit data comparator will require only 110 transistors and dissipates 17.25uw of power for 90nm technology

Index Terms **– Area efficient, Data comparator, Full subtractor, Half subtractor, Multiplexer, Power efficient**

I. INTRODUCTION

This In images and videos, salt and pepper noise can be eliminated by using basic filtering is MEDIAN filtering the data comparator is basic processing element to

compute median in the Median filter. Dissimilar Median filter architectures were prepared over the years. A need for an acceptable VLSI architecture was require for hardware implementation. Few of the past year works are listed below. Sindhu & Vasanth [1] Implemented a novel set of 8 bit Data comparator which could be a Feasible solution for Rank ordering networks in terms of area, speed and power. Vasanth et al suggested Vasanth sorting with minimal number of comparators for de-noising the image. A 3*3 window is used to order data with 25 comparisons in increasing order. For this sorting novel parallel architecture is designed with 8-bit data comparator. Bitwise data comparator to select high and low values. The advantage of these comparators are it operates at high speed and consumes low power [2].Different designs of full adder comparator is implemented and compared in terms of area, speed and power using DSCH and Microwind tool in 120nm and 70nm technology [3]. Anjuli and Anand used different logic styles for 2-bit magnitude. Four logic designs such as CMOS logic, pseudo NMOS logic , transmission gate and pass transistor logic (PTL) were simulated and observed that PTL with reduced power, power delay product transistor count [4].

An efficient reversible binary comparator using reversible logic gates like not, Feynman (CNOT) and Peres(PG) proposed by Rangaraju et al . The reversible binary comparator contains two stage These are input circuit and the later with one-bit comparator. So, a cell with n-bit reversible binary comparator is designed. PG gate is used to implementing binary comparator for calculating power consumption delay, Garbage outputs and constant inputs. The main advantage of the work is that it has a low quantum cost and garbage output values [5].

Sinha and Tripathi proposed binary decision diagram (BDD) for reduce power consumption. Which is implemented using a 4-bit comparator with register and XNOR gate. The fault of the work is that the proposed methods could not have a optimize area and leakages [6].Vasanth et al proposed a new Carry select comparator and later applied it on a parallel and pipelined modified shear sorting [7]. Novel sequential architecture for Decision based unsymmetrical trimmed midpoint filter (DBUTMPF) proposed by Vasanth et [8].Vasanth et al proposed a new Data Comparator using Borrow look ahead logic. The data comparator will take more area when compared to other data comparator [9,10].Area efficient and reduced power consumption Data Comparator is need with and trade off speed with the computation of Median in their architecture. Hence a suitable Data Comparator has to be proposed. Section II explains the implemented data comparator. Section III gives the simulation results and discussion of proposed work. Section IV gives the conclusion of the paper and V gives future scope of paper.

II. PROPOSED DATA COMPARATOR DESIGN USING MULTIPLEXER

The comparator is an one of very useful combinational circuit used for testing or comparing two binary numbers whether these binary number at one input is greater or less than to another binary number in comparator

,essential unit is XOR gate Basically The Comparators are two types (a).Magnitude Comparator (b). Data Comparator. The previous only the magnitude of the two binary numbers are compare and the later gives the greater and a lesser data itself. The Magnitude comparator produce two outputs to identify whether first input is greater than second input or vice versa . Whereas data comparator is basically two cell comparator, as it compares word A with word B and gives out a Higher and lower value respectively.

In Median Calculation 8 bit Data comparator is a basic processing element.Subtraction is the basic operation in a comparator so full subtractor is used as the Basic processing element in the proposed data comparator a. Fig. 1 gives the basic design of a Data Comparator. In this architecture there are two Multiplexers that choose a high or low value from the given inputs “x” and “y” based on the barrow generated to the control lines from bitwise comparators.

The barrow generator consists of eight bitwise full subtractor, which propagates barrow to select a High and low values from both the input. The starting bit will always have carry to be zero hence a Half subtractor shown in Fig. 2 is considered rather than full subtractor. The Proposed Multiplexer based Data Comparator contain two units 1. Borrow Generation unit and 2. Multiplexer unit to select high and low values.

A. Borrow Generation Unit

Consider the Borrow equation 1 of a full subtractor as the carry equation is used to propagate carry to the multiplexers of Data Comparator architecture given in Fig. 1. Consider 1 bit full Subtractor, where X and Y are inputs, Yin is the borrow in and Yout refers to borrow out. From the truth table of Full Subtractor shown in Table I derive the borrow equation as shown in 1.

$$Yout= X'Y'Yin+X'YYin'+X'YYin+XYYin \quad (1)$$

$$Yout=Yin(XY+X'Y')+X'Y(Yin+Yin') \quad (2)$$

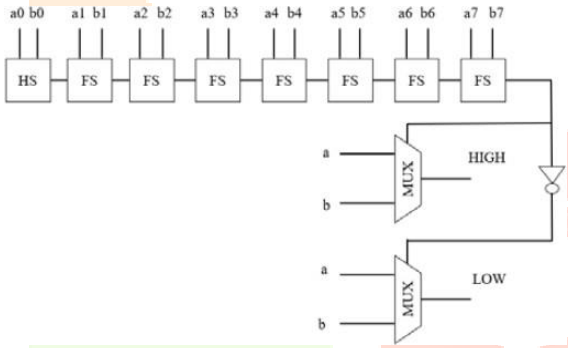


Fig. 1. Basic design of Data Comparator

Alternate form of design is made from Table I.Let the upper half values of the truth table where input “x” will be 0 and the inputs y and yin values changes.Similarly the lower half values of the truth table has “x” as 1. From the table it is observed that if the value of “x” takes 0 different “y”and “yin” respectively ,then the borrow equation produces 0,1,1,1. This can be replaced with an OR gate.Similarly if the value of “x” takes 1 then the borrow equation produces 0,0,0,1 for different “y” and “yin” respectively. This can be replaced with an AND gate. From this logic we can Simplify the borrow equation can be deduced in the form of a multiplexer equation as given in 3.

$$Yout=(X'(Y+Yin))+(X(YYin)) \quad (3)$$

The above equation borrow equation of a full subtractor implemented using multiplexer.The first part of the equation 3 indicates the upper half of the truth table and second half of the truth table indicates lower half of truth table.It indicates that when the input “x” is zero the output will resemble OR gate output of inputs “y” and “yin”.Similarly when the input “x” is one the output will resemble AND gate output of inputs “y” and “yin”. Hence the entire logic will be designed in 2X1 Multiplexer only.

Table 1: Truth table of full subtractor borrow out equation

X	Y	Yin	Yout
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

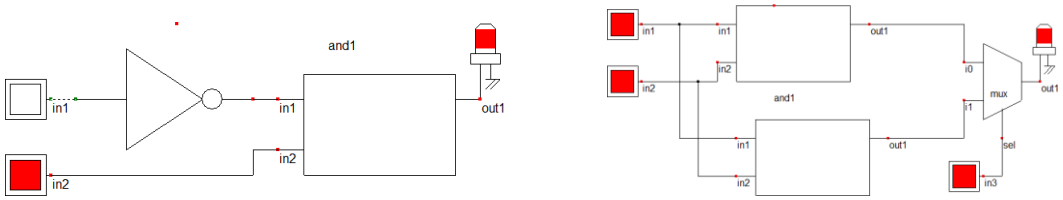


Fig. 2. (a) half subtractor Borrow equation design (b) full subtractor Borrow equation design.

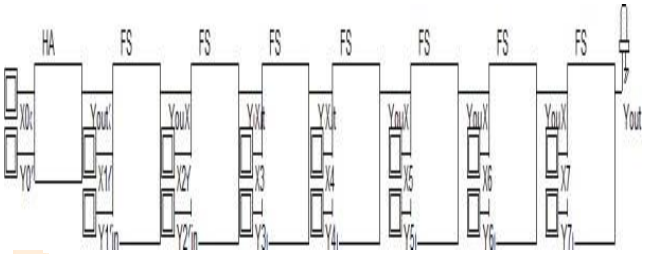


Fig. 3. Borrow Generation Unit

B. Multiplexer Block to choose High and Low values

The output of the Borrow generation unit is given to input of two multiplexers that produce the high and low values between the inputs given to the system. The output of 8-bit full subtractor is given as control line to custom made multiplexers. The Borrow propagation from borrow generation unit is given to upper multiplexer directly and borrow propagated from borrow generator is inverted and give to the control lines of the lower multiplexer. multiplexers compares the given input values and gives a High value and low value as an output based on borrow generated . The Implementation is shown in Fig. 4

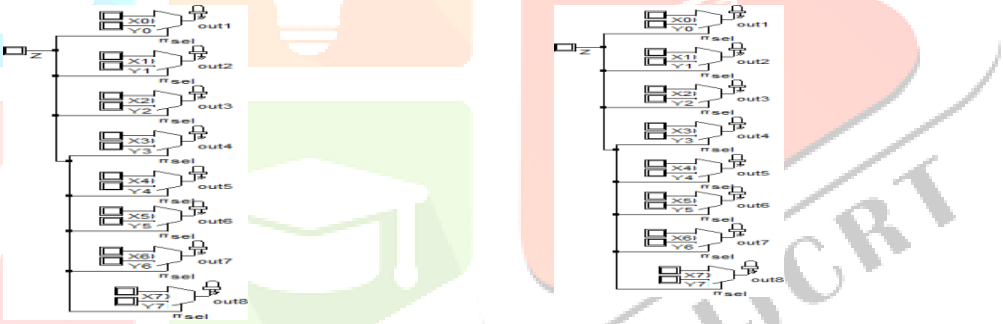
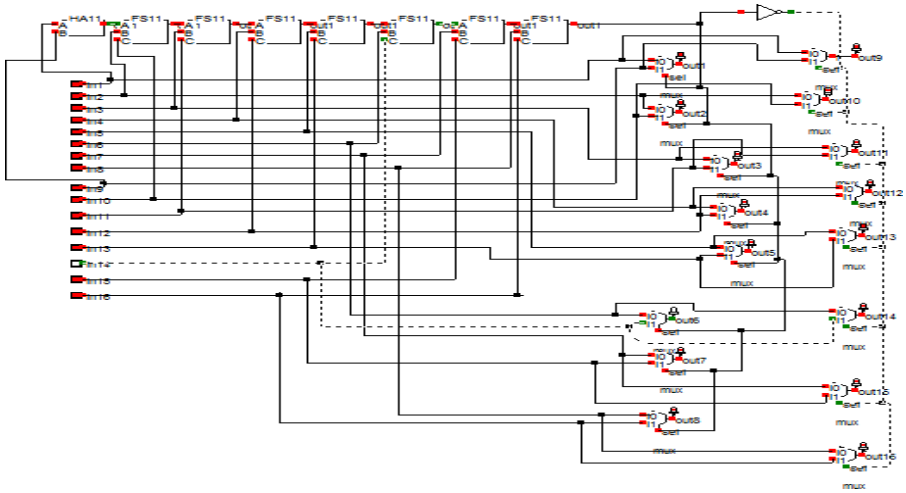
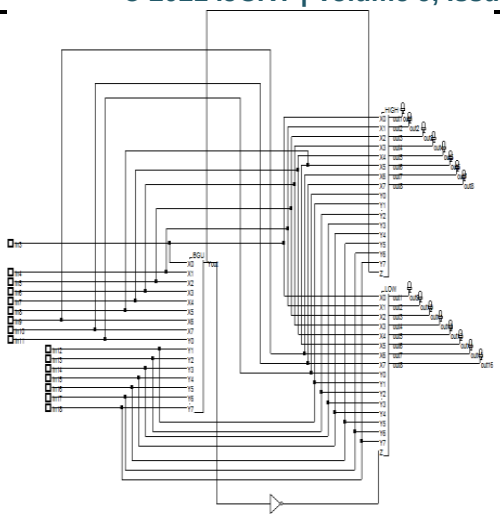


Fig.4. Multiplier of high and low value outputs.

The Proposed design is implemented using Dsch2 and Microwind 2 and simulated the layout for different technologies. Different types of Data Comparators were used for performance comparison with the proposed design.

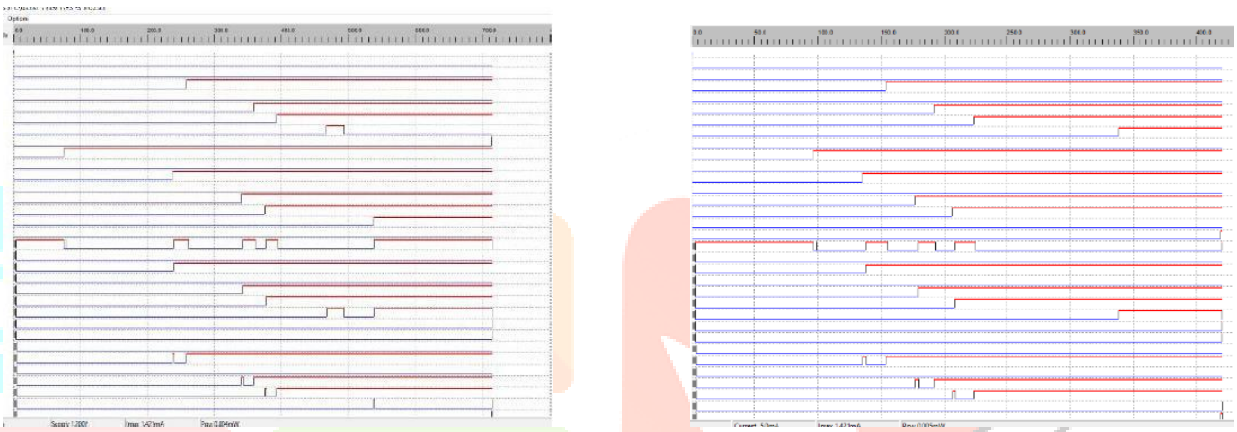


(a)



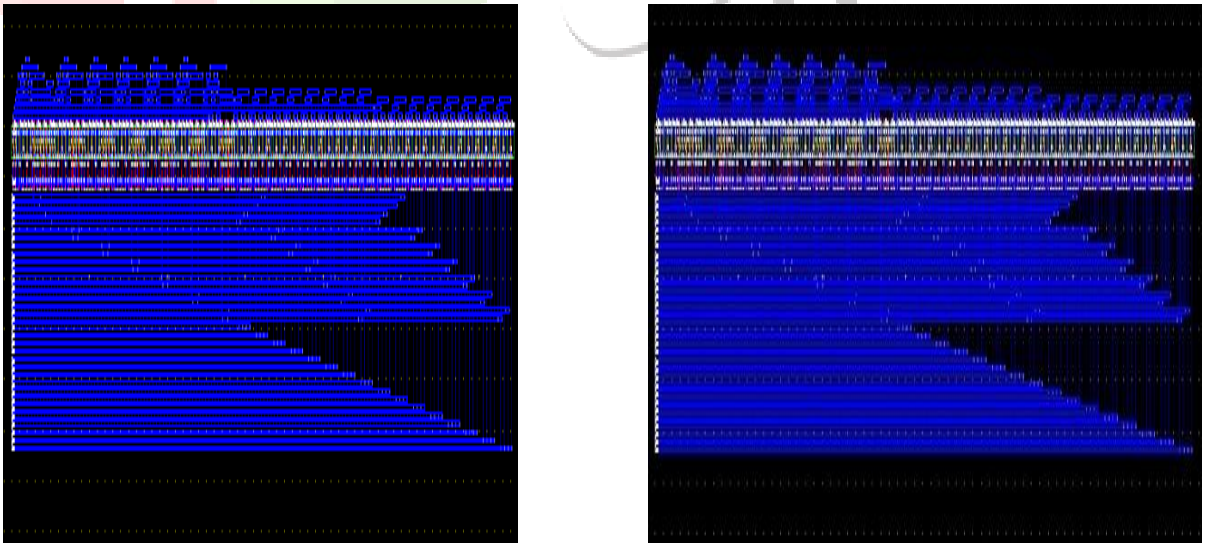
(b)

Fig.5. Proposed Data Comparator designs

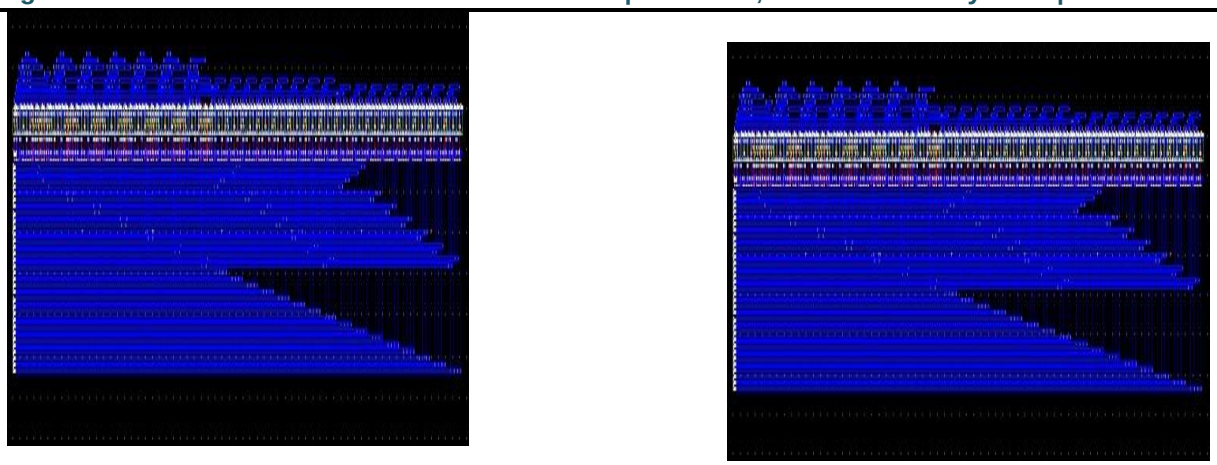


(a) (b)

Fig.6. Simulation results of proposed Data Comparator in Dsch2



(a) (b)



(c) (d)

Fig.7. layout of proposed Data comparator in different technologies (a)0.12um (b)90nm (c)70nm (d) 50nm

Table 2: No.Of transistors required by different data comparator models for different technologies.

Technology	HS_FS LOGIC	FS LOGIC	FS_MUX LOGIC	HS_FS MUX LOGIC	HS_FS AOI LOGIC	HS_FS XOR LOGIC	HS_FS XNOR LOGIC	MUX BASED LOGIC	Proposed Logic
0.6um	299	291	275	263	259	249	242	121	110
0.8um	299	291	275	263	259	249	242	121	110
0.12um	299	291	275	263	259	249	242	121	110
0.18um	299	291	275	263	259	249	242	121	110
0.25um	299	291	275	263	259	249	242	121	110
0.35um	299	291	275	263	259	249	242	121	110
1.2um	299	291	275	263	259	249	242	121	110
50nm	299	291	275	263	259	249	242	121	110
70nm	299	291	275	263	259	249	242	121	110
90nm	299	291	275	263	259	249	242	121	110

Table 3: Power dissipation(mw) by different data comparator models for different technologies.

Technology	HS_FS LOGIC	FS LOGIC	FS_MUX LOGIC	HS_FS MUX LOGIC	HS_FS AOI LOGIC	HS_FS XOR LOGIC	HS_FS XNOR LOGIC	MUX BASED LOGIC	Proposed Logic
0.6um	51.30	43.64	49.402	40.151	35.945	28.14	21.14 12.6	12.6	6.78
0.8um	51.27	49.54	47.997	46.247	43.474	37.91	32.803	16.6	9.51
0.12um	0.533	0.497	0.495	0.441	0.434	0.352	0.170	0.25	0.07
0.18um	2.330	2.659	2.249	2.358	1.956	1.808	0.918	0.72	0.4
0.25um	4.869	5.524	4.715	4.850	4.170	3.664	1.952	2.37	0.9
0.35um	14.73	13.36	16.180	12.973	10.412	9.308	13.173	4.15	2.3
1.2um	70.62	64.99	65.540	64.870	57.057	51.95	75.24	25	15
50nm	0.025	0.024	0.023	0.0216	0.0160	0.017	0.020	0.007	0.001
70nm	0.108	0.101	95.422	0.0895	0.0753	0.072	0.0927	0.073	0.004
90nm	0.375	0.353	0.325	0.317	0.281	0.253	0.250	0.178	0.006

Fig. 7 shows the comparison of proposed layouts of data comparators in different Technologies. Fig. 8 shows the Simulation results of the proposed Data Comparator using multiplexer. The proposed data comparator logic works functionally correct. The gate level diagram for multiplexer based AND gate, OR gate barrow generation unit and high and low value output are designed in Dsch2 software and dsch2 generate verilog file for the logic. In Microwind software ,verilog file is imported to get layout of designs and we can change design technology for proposed logic. The layout is simulated by microwind software tool to analyze proposed design in aspect of transistors, node parameters, delay and power .Different technology files were selected and layouts were simulated in it.

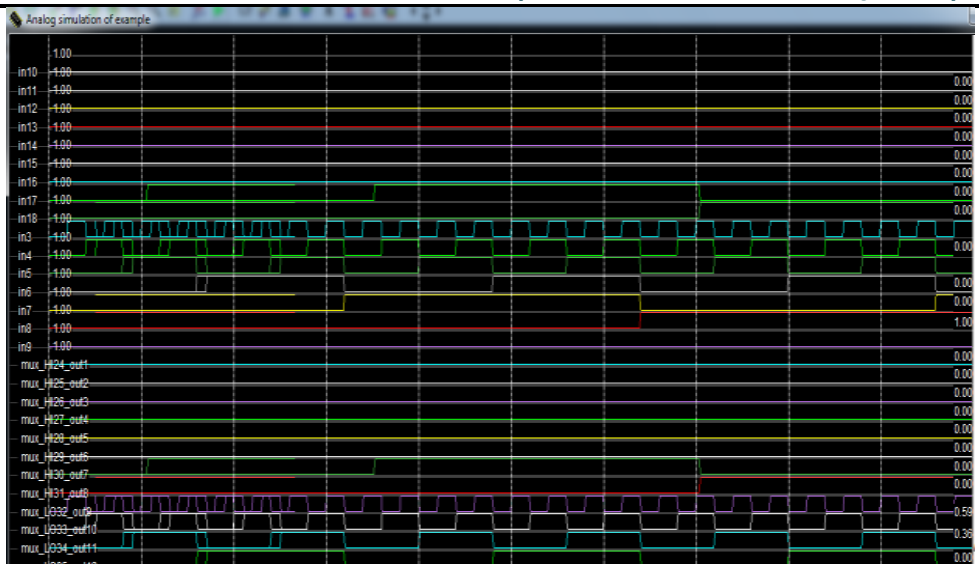


Fig.8. Simulation results of the proposed Data Comparator in 90nm Technology.

Table 2 shows the no. of transistors used by dissimilar Data Comparator logic for different Technologies. Table 3 shows the Power Dissipation (mw) by dissimilar Data Comparator logic for different Technologies. It was observed that the proposed data comparator using Multiplexer requires only 110 transistors (CMOS logic) with the power dissipation of 0.012mw.initially,299 transistors are required to implement data comparator using conventional full subtractor . Different designs of borrow equations were implemented using XOR, XNOR gates, Bit sliced and Multiplexer based. Proposed designs are implemented using multiplexer logic helped in minimization of number of transistors and power dissipation. For 90nm technology, the percentage of transistors reduced from 299 to 110 which results 65% reduction in area. Also, the power consumption for 90nm technology got reduced from 0.375mw to 0.042mw which is 88% power saving. So, proposed Data Comparator using multiplexer is area Efficient and power efficient.

III. CONCLUSION

In this paper we proposed A Novel Data Comparator using Multiplexers for different technology. The multiplexer based data comparators contains full subtractor these full subtractor are implemented only using 2X1 multiplexers. The Multiplexer based data comparator implementations resulted in 65% of area and 88% of power consumption. The proposed logic requires less area and power compared to existing.

IV. FUTURE SCOPE

In any digital and computer system, digital comparators are important element to perform comparison operatiobetween two binary bits. Comparators has the wide range of applications in digital image processing and signal processing .low power and efficient comparator has significant role in modern wireless communication system i.e. multiple input multiple output (MIMO) in decoding algorithms to perform large number of iterations of binary number comparisons. Data comparators used for rank ordering of image applications. Proposed data comparators are used for eliminating salt and pepper noise in images.

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