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# LOW POWER GEFFE AND SMOOTHER COMBINED TEST PATTERN GENERATOR FOR BIST

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***Abstract*—**The increasing complexity of the Very Large Scale Integration (VLSI) circuits necessitates miniaturization and fabrication of the nano-scale device in the intricate manufacturing process. However, this had led to greater process variation, higher probability of defects and worsened the manufacturing yield. Various Automatic Test Pattern Generation (ATPG) tools available today employ powerful heuristics and are capable of generating efficient and compact test sets for a Circuit-Under-Test (CUT). These tools provide tests with high fault coverage, and identify redundant faults in the CUT to a large extent, even though the underlying problem is known to be computationally hard. But, the production tests are primarily aimed only for fault detection and they may not be very efficient for diagnosis. Linear Feedback Shift Registers (LFSRs) are the most widely used pseudorandom Test Pattern Generators (TPGs) in Built-In Self-Test (BIST) systems. This proposes a combined testing methodology for the scan-based BIST. A smoother and Geffe generator are included in the TPG to reduce average power consumption during scan testing, while a group-based selection algorithm is employed for the scan-chain reorder in order to improve the fault coverage. The objective is to produce test pattern with good randomness; then the fault coverage will be better. Fault simulation is done using Xilinx. From the experimental results, it is observed that the proposed methodology achieves better performance than the existing methods.

***Index Terms*—Built-In Self-Test (BIST) System, Geffe Generator, Linear Feedback Shift Register (LFSR), Smoother, Test Pattern Generator**

## I. INTRODUCTION

IN the case of BIST system, minimization of area, power and delay plays a vital role in improving the operational efficiency of the circuit. LFSR is used to eliminate the need of storage elements for area reduction. This reduces the hardware space and directly applied to the CUT [1]. Further, increase in the length of the test pattern develops the fault coverage. This resulted in the increase in the test time and the frequency of the innovative test case generation. Also, it caused increase in the power consumption [2] and damage of the Circuit Under Test (CUT). Hence, development of the fault coverage is one of the important measures in the BIST [3]. The usage of weighted techniques for the generation of test patterns could provide fault coverage. It can also determine the problems of test pattern resistance. Recently, the strategies for low power become a major challenge in the VLSI systems [4].

Several methods are available to reduce the power consumption in the CUT. Abu-Issa and Abdallatif [5] presents a weighted based cell segmentation algorithm for multiple scan-chains BIST in order to reduce the average power consumption during the scan in of new test vectors, and to reduce the test application time. This technique is based on selecting the best group of cells to be connected in the same scan-chain. This group of cells should have the same or very close weight of logic 1's and 0's that will be optimal to get the highest fault coverage in a specified test length. Then each scan chain input will be connected to an output of a combinational circuit located after the Linear Feedback Shift Register that will generate biased test vectors according to the optimal weight of this segment of cells in the scan-chain. Thus, increasing the fault coverage and smoothing the applied test patterns which will reduce the power consumption.

This design is divided into two main stages: The first stage is to find the weight of logic 1 and logic 0 for each cell in the scan chain, while the second stage works in dividing the scan-chain into multiple segments such that each segment will include the scan cells that have approximately the same weight. The area overhead of this design is the area needed to replace the XOR gates in the phase-shifter LFSR with one or two-level combinational circuits. This area is considered to be negligible because the

added combinational logic circuit in the design is either one level (in this case it was efficient to use one gate of up to 4 inputs) or two-levels (in this case it was efficient to have the first level of up to three logic gates, each gate is up to three inputs, the second level is one gate of up to three inputs). The big number of different combinational circuits that can be implemented was sufficient enough to produce any needed weight of any scan-segment. The area overhead (sometimes positive and sometimes negative) is comparable with the area of the XOR gate used in the phase shifters.

In BIST, LFSR is commonly used in the test pattern generator and output response analyzer. A major drawback of LFSR is that the pseudorandom pattern generator. It has high switching activities in the CUT which can cause excessive power dissipation. The LFSR usually needs to generate very long pseudorandom sequences in order to achieve the target fault coverage.

To overcome the existing drawbacks, a new testing methodology is proposed for the scan-based BIST. A smoother and Geffe generator is included in the TPG to reduce average power consumption during scan testing, while a group-based selection algorithm is employed for the scan-chain reorder in order to improve the fault coverage with reduced switching activity. The patterns generated by the pseudo-random pattern generator are smoothed by the smoother, and then the smoothed patterns are shifted into the scan chain. Since there are fewer bit-transitions in the smoothed patterns, the power consumed in the BIST process will be reduced. The pseudorandom properties of the LFSR lead to high fault coverage during the set of testing operations.

The work is organized as follows: Section II describes the existing works related to the testing and scanning of the BIST system. Section III explains the proposed testing methodology. Section IV presents the performance analysis of the proposed methodology and Section V concludes the work with the benefits of including Geffe generator in the BIST system.

## II. LITERATURE SURVEY

This section describes the existing works related to the testing and scanning of the BIST system. Abu-Issa and Quigley [6] presented a novel low-transition LFSR that is based on the new observations about the output sequence of a conventional LFSR. The proposed design, called as bit-swapping LFSR (BS-LFSR) comprised of an LFSR and a 2 times 1 multiplexer. When used to generate test patterns for scan-based BIST, the number of transitions that occur at the scan-chain input during scan shift operation were reduced by 50% when compared to those patterns produced by a conventional LFSR. Hence, the overall switching activity in the circuit under test was reduced during the test applications. The BS-LFSR is combined with a scan-chain-ordering algorithm that orders the cells in a way that reduces the average and peak power in the test cycle or while scanning out a response to a signature analyzer. These techniques had a substantial effect on average and peak-power reductions with negligible effect on the fault coverage or test application time. Experimental results on the benchmark circuits had shown 65% and 55% reductions in average and peak power, respectively. However, it suffered due to higher switching activity.

Liang et al. [7] proposed a novel TPG for BIST, which generated Multiple Single-Input Change (MSIC) vectors in a pattern. A reconfigurable Johnson counter and a scalable SIC counter were developed to generate a class of minimum transition sequences. The proposed TPG was flexible to both the test-per-clock and the test-per-scan schemes. A theory was also developed to represent and analyze the sequences and to extract a class of MSIC sequences. The MSIC sequences have the favorable features of uniform distribution and low input transition density. Simulation results demonstrated that the MSIC sequences can save the test power and impose less overhead for a scan design. But, the fault coverage is less.

Xiang et al. [8] introduced two-stage scan architecture to constrain transition propagation within a small part of scan flip-flops. Most scan flip-flops were deactivated during test application. The first stage included multiple scan chains, where each scan chain is driven by a primary input. A group of scan flip-flops in the second stage was driven by each scan flip-flop in the multiple scan chains. Scan flip-flops in different stages used separate clock signals. Test signals assigned to scan flip-flops in the multiple scan chains were applied to the scan flip-flops of the second stage in one clock cycle after the test vector has been applied to the multiple scan chains. There was no transition at the scan flip-flops in the second stage when a test vector was applied to the multiple scan chains. High power reduction was achieved. However, area overhead was not considered in the work.

Power consumption during the scan-based testing operation can be higher than during the normal mode operations. This caused yield loss and degradation of reliability. Kang et al. [9] proposed a scan cell reordering algorithm to reduce the test power consumption during scan-based testing. The proposed algorithm considered both the shift-out operations and shift-in operations. A Cumulative Weighted Transition (CWT) was proposed and compared to reduce the test power consumption. Experimental results show that the proposed method greatly reduced the average power during scan testing. But, power consumption during the ordering was high.

As the scan-based testing enabled higher test coverage and quicker test time, it was widely used by most system-on-chip (SoC) designers. However, as there were million number of logic gates, a number of scan cells lead to excessive power consumption and produced a low shifting frequency during the scan shifting mode. Seo et al. [10] present a new scan shift power reduction method based on a scan chain reordering (SR)-aware X-filling and a stitching method. There is no need to require an additional logic for reducing the scan shift power, just a little routing overhead. Experimental results show that this method improves scan shift power consumption on benchmark circuits in most cases compared to the results of the previous works. But, it suffered from the unnecessary pattern generation.

## III. PROPOSED METHOD

In the proposed method, the test patterns are generated and applied to the Geffe generator. The Geffe generator makes use of three LFSRs: LFSR0, LFSR1, and LFSR2. The bit generated by LFSR0 selects either LFSR1 or LFSR2, and the corresponding bit from the selected LFSR is used in the final output sequence. A 2-to-1-multiplexer is used to make the selection and creates the nonlinear forward transformation. The smoother is used for the smoothing of the patterns generated by the pseudo-random pattern generator. Then, the smoothed patterns are shifted into the scan chain [11]. Since there are fewer bit-transitions in the smoothed patterns, the power consumed in the BIST process will be reduced.

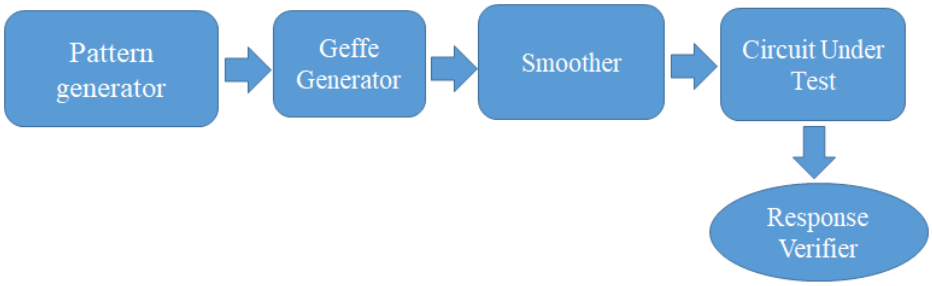


**Figure.1 Block Diagram of the proposed methodology**

### *A. LFSR*

LFSR is a shift register whose input bit is a linear function of its previous state. The most commonly used linear function of single bits is Exclusive-Or (XOR). Thus, an LFSR is most often a shift register whose input bit is driven by the XOR of some bits of the overall shift register value.

The initial value of the LFSR is called as the seed, and because the operation of the register is deterministic, the stream of values produced by the register is completely determined by its current (or previous) state. Likewise, because the register has a finite number of possible states, it must eventually enter a repeating cycle. However, an LFSR with a well-chosen feedback function can produce a sequence of bits that appears random and has a very long cycle. The sequence of numbers generated by an LFSR or its XNOR counterpart can be considered a binary numeral system just as valid as Gray code or the natural binary code.

The arrangement of taps for feedback in an LFSR can be expressed in finite field arithmetic as a polynomial mod 2. This means that the coefficients of the polynomial must be 1s or 0s. This is called the feedback polynomial or reciprocal characteristic polynomial. For example, if the taps are at the 16th, 14th, 13th and 11th bits, the feedback polynomial is expressed as

$x^{16} + x^{14} + x^{13} + x^{11} + 1$

The number "one" in the polynomial does not correspond to a tap – it corresponds to the input to the first bit (i.e. x0, which is equivalent to 1). The powers of the terms represent the tapped bits, counting from the left. The first and last bits are always connected as an input and output tap respectively. Figure.2 shows the 16-bit LFSR and Figure.3 shows the LFSR circuit.

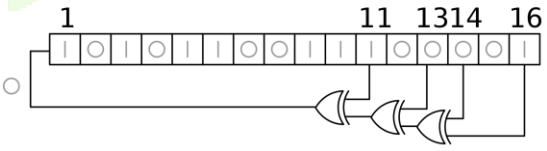


**Figure.2 16-bit LFSR**

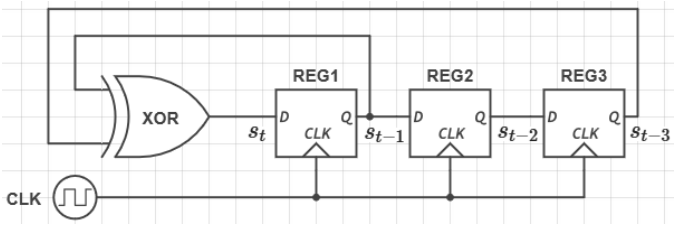


**Figure.3 LFSR Circuit**

*B. Geffe Generator*

Proposed method comprises three LFSMs and a 2-to-1 multiplexer. A common choice for these LFSMs is the LFSRs which can achieve maximum cycle length (i.e. LFSRs which can be described by a primitive polynomial). Proposed system makes use of three LFSRs: LFSR0, LFSR1, and LFSR2 . The bit generated by LFSR0 selects either LFSR1 or LFSR2, and the corresponding bit from the selected LFSR is used in the final output sequence. A 2-to-1 multiplexer is used to make the selection and creates the nonlinear forward transformation. Figure.4 presents the Geffe generator comprising three LFSRs connected. LFSR2 is used as a control generator to connect either LFSR1 or LFSR3 to the output, but not both together. If the control generator produces '0', then LFSR1 is connected, and if it produces '1', then LFSR3 is connected. The resulting Geffe sequence is based on the binary sequences generated by the LFSRs [12].

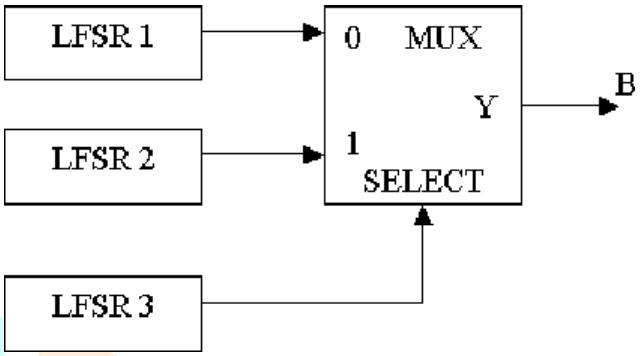


Figure.4 Geffe Generator

The objective of a random number generator (RNG) is to produce random binary numbers which are statistically independent, uniformly distributed and unpredictable. RNGs are necessary in many applications like cryptography, communication, VLSI testing, probabilistic algorithms, and so on. RNG randomness evaluation is performed by using a seed encryption

A new LFSR architecture is presented for scan-based BIST that fully exploits the encoding ability of an LFSR by using more than one cells of the LFSR for feeding the scan chain of the CUT, in different test phases In the proposed technique, the segmentation is performed by simply retaining one copy of a pattern as a reference pattern and used to specify whether the successive patterns are equal or unequal to the retained reference pattern or not.

Test sequences generated by the Geffe generator have large cycle period, and are able to achieve considerably more transitions that those created by linear machines. Geffe generators have equal ability in detecting stuck-at faults in combinational circuits as linear generators do. In the case of diagnosing stuck-at faults in sequential circuits, the Geffe generator performs much better than the linear machines. Because of these benefits, Geffe has been suggested as a desirable pseudo-random pattern generator in the arena of obtaining a high coverage for delay faults and stuck-at faults for sequential circuits.

Selective Huffman coding has recently been proposed for efficient test data compression with low hardware overhead. In this work, it is shown that the already proposed encoding scheme is not optimal and a new encoding scheme is presented, which is optimal. Moreover, the proposed encoding always offers better compression. In terms of hardware overhead, the new scheme is as low-demanding as the old one.

Huffman coding technique is basically a statistical coding scheme, which is a fix-to-variable coding scheme. It represents data blocks of fixed length by variable length code words. Symbols occur more frequently have shorter code words than symbols that occur less frequently. This will reduce the average number of bits for a code word. Therefore, compression is achieved. An example of deriving the Huffman code is shown in Table 1 [13]. In this example, the test set is divided into 4-bit blocks. Table 1 shows the frequency of occurrence of each of the possible blocks. The compression ratio is determined by how skewed the frequency of occurrence is.

0010 0100 0010 0110 0000 0010 1011 0100 0010 0100 0110 0010 0010 0100 0010 0110 0000 0110 0010 0100 0110 0010 0010 0000 0010 0110 0010 0010 0010 0100 0100 0110 0010 0010 1000 0101 0001 0100 0010 0111 0010 0010 0111 0111 0100 0100 1000 0101 1100 0100 0100 0111 0010 0010 0111 1101 0010 0100 1111 0011

Table 1 Huffman Coding

| Symbol | Freq. | Block | Huff. Code |
|---|---|---|---|
| $S_0$ | 22 | 0010 | 10 |
| $S_1$ | 13 | 0100 | 00 |
| $S_2$ | 7 | 0110 | 110 |
| $S_3$ | 5 | 0111 | 010 |
| $S_4$ | 3 | 0000 | 0110 |
| $S_5$ | 2 | 1000 | 0111 |
| $S_6$ | 2 | 0101 | 11100 |
| $S_7$ | 1 | 1011 | 111010 |
| $S_8$ | 1 | 1100 | 111011 |
| $S_9$ | 1 | 001 | 111100 |
| $S_{10}$ | 1 | 1101 | 111101 |
| $S_{11}$ | 1 | 1111 | 111110 |
| $S_{12}$ | 1 | 0011 | 111111 |
| $S_{13}$ | 0 | 1110 | - |
| $S_{14}$ | 0 | 1010 | - |
| $S_{15}$ | 0 | 1001 | - |

In general, test patterns generated by commercial ATPG tools contain massive unspecified bits (don't-care bits) that can be assigned with 1's and 0's in a way to skew the frequency distribution. This is helpful to maximize the compression efficiency. In the work proposed by Lu et al. [13], two don't care assignment techniques are proposed. However, only compatible characteristics are used in their techniques. Two blocks are compatible if there is no conflict in any bit position of the two blocks. For our complementary coding techniques, beside the compatible blocks are exploited, complementary blocks are also searched. Therefore, the compression algorithm is proposed in this paper to perform don't care assignment. In the proposed algorithm, there is an initial search for the most frequently occurring unspecified block F1. Thereafter, it is compared with the next most frequently occurring unspecified block F2. If there is no conflict in any bit position, these two blocks are merged by specifying every bits position if there is specified bit in either block. All F2 blocks in test set are appended with 0 to indicate that it is merged with F1 block. For example, if block F1 00XX is merged with block F2 0X1X, the result is 001X. All F2 blocks in the test set will be changed to 0001X.

Alternatively, if there is a conflict, F1 is compared with the complement of F2. If there is no conflict in any bit position, then they are merged. All F2 blocks in the test set are appended with 1 to indicate that it is merged with F1 block in its complementary form. For example, if F1 is 00XX and F2 is 1X0X, block 00XX is merged with block 0X1X, which is the complement of block 1X0X. The resulted block is 001X and all F2 blocks in the test set are changed to 1001X. Thereafter, F1 is compared with all the other unspecified blocks in decreasing order of frequency and merged if possible. This process is finished if there is no more block that can be merged with F1. This process is then repeated until there is no more blocks that can be merged in the test set. Any remaining X's can be randomly assigned 0's or 1's since it has no effect on the compression ratio.

## IV. Performance Analysis

Simulation is done using the XILINX. Figure.5 shows the initial seed generation and Figure.6 presents the three LFSR patterns. Table 2 depicts the comparative analysis of the parameter utilization by the existing and proposed methods. Figure.7 depicts the performance analysis of the existing and proposed methods. The graph shows that there is a considerable reduction in the time and area based on the implementation results. The proposed algorithm significantly reduces area consumption when compared to the existing system.

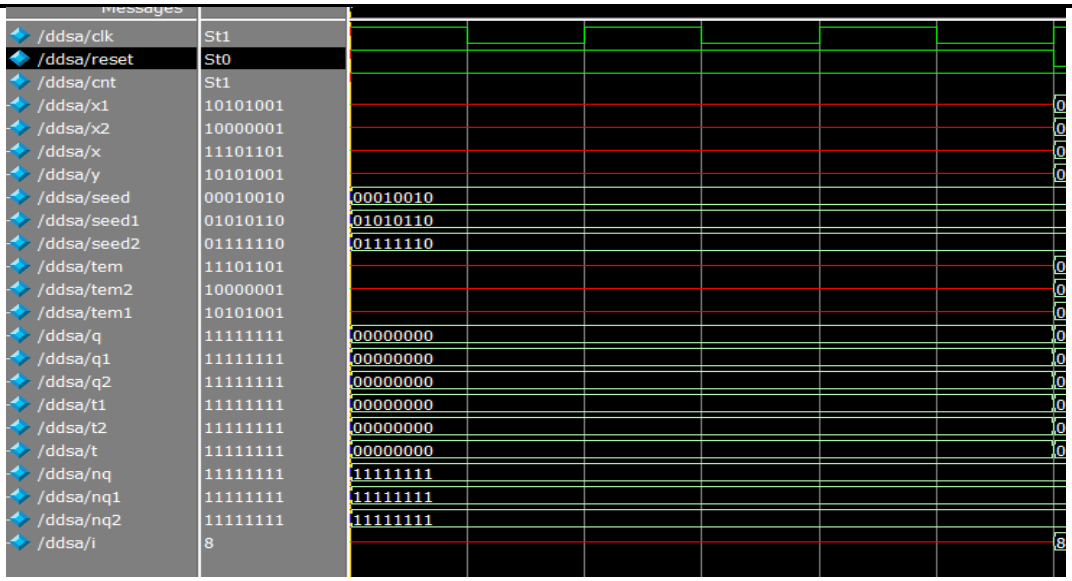


**Figure.5 Initial seed generation**

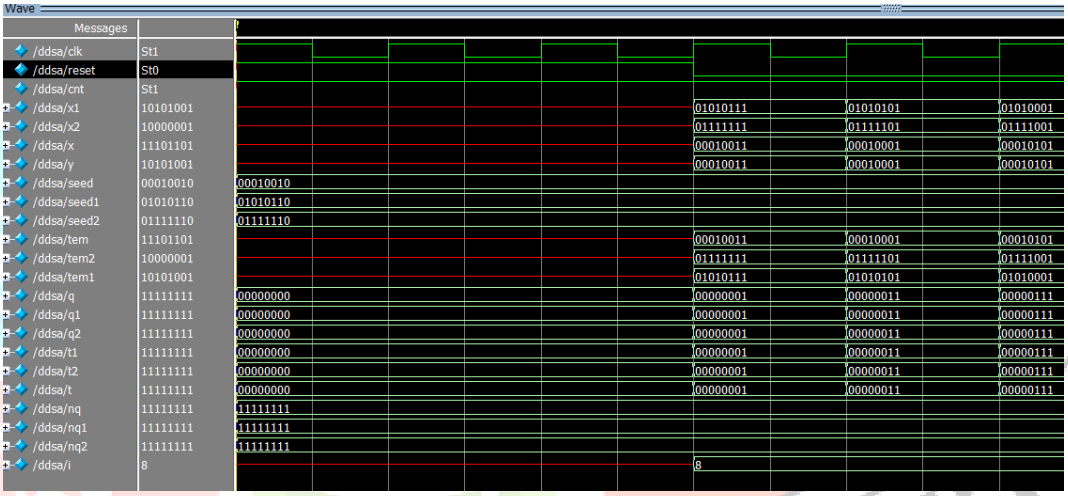


**Figure.6 Three LFSR patterns**

**Table 2 Comparative Analysis of Parameter utilization by the existing and proposed methods**

| S. No | Parameter | Existing | Proposed |
|---|---|---|---|
| **1** | Slices | 10 | 9 |
| **2** | Slices FF | 18 | 17 |
| **3** | LUT | 11 | 7 |

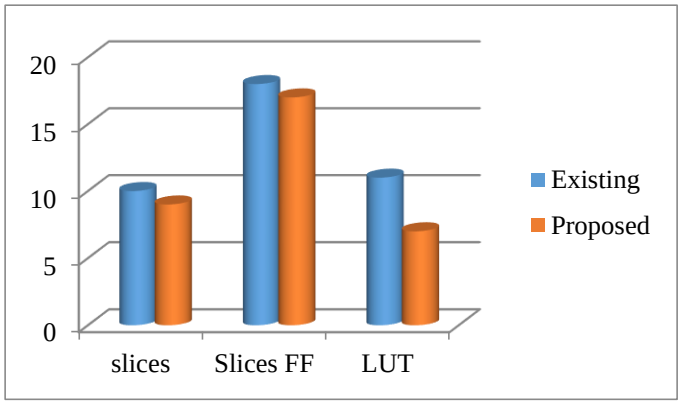


**Figure.7 Performance Analysis of the existing and proposed methods**

## V. CONCLUSION

The increasing complexity of modern integrated circuits leads to a critical need for cost-efficient test solutions. To address such test challenges, sophisticated test strategies such as BIST have been developed over two decades. The fundamental idea in BIST is to integrate the test pattern generation and output response analyzer for the CUT. The redesign by Huffman compressed Geffe generator uses the technique of LFSR embedding to reduce the hardware overhead. According to our experiment, the Geffe modification can cut down the area usage on average. More importantly, the fault simulation results show the modified Geffe generator is capable to maintain the fault detection ability of the original Geffe generator. The redesign approach presented in this paper offers a possibility of using Geffe generators in BIST to deliver high fault coverage with reasonable area overhead.

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