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A NOVEL COPLANAR BASED XOR/XNOR STRUCTURE FOR DESIGN OF QCA Circuits

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***Abstract*—**Quantum-dot Cellular Automata (QCA) is a nanoscale computational fabric being explored by the Very Large Scale Integration (VLSI) research community due to the difficulties in the mounting of the CMOS transistors. This work uses QCA devices and uses those devices to build a simple field programmable gate array (FPGA). The FPGA is a combination of multiple Configurable Logical Blocks (CLBs) tiled together. In this work, a novel XOR/XNOR-function logic gate with two inputs, two enable inputs and one output is proposed and designed in QCA nanotechnology. A design rule for specialized architecture design is presented using programmable devices and introduced a simulation engine tuned to efficiently simulate QCA circuits designed for this architecture. In order to demonstrate the functionality and capabilities of the proposed QCA based XOR/XNOR architecture, performance is evaluated and analyzed. The proposed XOR/XNOR logic gate has a superb performance in terms of area, complexity, power consumption and cost function in comparison to some existing QCA-based XOR architectures. Moreover, some efficient circuits based on the proposed XOR/XNOR gate are designed in QCA.

***Index Terms*—Exclusive OR (XOR), Exclusive NOR (XNOR), Full Adder, Quantum-dot Cellular Automata (QCA), Very Large Scale Integration (VLSI)**

I. INTRODUCTION

Recent trends in microelectronics technology have gradually changed the conventional strategies used in VLSI circuits. Establishing an efficient methodology is one of the key to design VLSI chip successfully. The design of microelectronics system is strongly influenced by the fact that transistor and featured size have continuously influenced, while density and frequency have increased. VLSI will undoubtedly play a key role in a technical revolution which yields a great benefit through application in communications, leisure and education The major advantages of VLSI technology might be as follows: development of new functions and application, low cost, light weight, and low power dissipation, improvement in reliability and safe, possibility of being used to highly sophisticated control system and more advanced service function through systemization.

Addition is a fundamental operation for any digital system, digital signal processing or control system. A fast and accurate operation of a digital system is greatly influenced by the performance of the resident adders. Adders are also very important component in digital systems because of their extensive use in other basic digital operations such as subtraction, multiplication and division. Hence, improving performance of the digital adder would greatly advance the execution of binary operations inside a circuit compromised of such blocks. The performance of a digital circuit block is gauged by analyzing its power dissipation, layout area and its operating speed. Adders are commonly found in the critical path of many building blocks of microprocessors and digital signal processing chips. Adders are essential not only for addition, but also for subtraction, multiplication, and division. Addition is one of the fundamental arithmetic operations. A combinational circuit that performs addition of two bits is called as Half Adder. One that performs addition of three bits is called as a Full Adder. The performance of a traditional arithmetic circuit has limits such as high energy consumption and high cost related to manufacturing, verification and testing. Hence, the programmable processors are developed to overcome these issues.

QCA technology is a promising alternative [1-5]. Compared with traditional CMOS technology, the computing paradigm of QCA technology has the advantages of ultra-high density, fast switch speed in terahertz frequency range and ultra-low power consumption. Since QCA technology is very different from current CMOS technology, it is obvious that different and novel design methods are needed to design the circuit. A novel XOR/XNOR logic gate has been presented and then several complex circuits have been proposed based on the XOR/XNOR logic gate. The performance of the proposed XOR/XNOR logic gate was verified by physical verification and simulation. It was shown that the proposed XOR/XNOR logic gate has the less numbers of cells and less

area. The cost of the proposed XOR/XNOR design is low. The proposed XOR/XNOR can be used as a basic logic gate in designing of QCA based large and complex circuits (1-bit full adder, 4-bit adder) so it is very flexible to be used for complex circuit design.

The work is organized as follows: Section II describes the existing works related to the QCA design. Section III explains the proposed XOR/XNOR design and QCA components. Section IV presents the simulation and comparative analysis of the proposed design and Section V concludes the proposed work.

II. LITERATURE SURVEY

This section describes about the existing works related to the QCA architectures. Roohi et al. [6] developed a new Parity-Preserving Reversible Gate (PPRG) with rich fault-tolerance features and reversibility attributes, by using QCA technology. Our proposed PPRG gate was designed in a manner such that equal parity was provided for each input set and its corresponding output. Due to the resilient cascadability, the utility of the proposed PPRG was enhanced further. Performance of the proposed PPRG design was validated by implementing thirteen standard combinational Boolean functions of three variables. Switching and leakage energy dissipation were low. Finally, fault detection and isolation properties were formalized into a concise procedure.

QCA technology is a promising alternative technology for the CMOS technology, due to low-power consumption, high-speed and high-density devices. In the QCA technology, the ultra-dense and low-latency digital circuits were designed. One of the important digital circuits is Full Adder (FA). Adelnia and Rezai [7] designed and evaluated a new and efficient multilayer QCA full adder circuit. In the designed circuit, sum and carry outputs were designed in separated layers. Then, a novel and efficient 4-bit Ripple Carry Adder (RCA) circuit was designed based on this new FA circuit. The proposed QCA circuits were simulated using QCADesigner tool version 2.0.3. The simulation results demonstrated that the proposed 4-bit QCA RCA requires 135 QCA cells, 0.06 μm2 area and 5 clock phases.

Balali and Rezai [8] presented and evaluated a novel single-layer four-bit QCA RCA circuit. The developed four-bit QCA RCA circuit was based on the novel QCA full adder circuit. The developed circuits were simulated using QCADesigner tool version 2.0.3. The simulation results show that the developed circuits have advantages in comparison with existing single-layer and multilayer circuits in terms of cell count, area occupation and circuit latency.

Arani and Rezai [9] proposed and evaluated a novel serial–parallel QCA multiplier circuit based on a designed efficient full-adder circuit. The designed circuits were simulated using QCADesigner version 2.0.3. The results demonstrate that the proposed circuits have advantages in comparison with other QCA circuits in terms of cell count, area, and cost.

Campos et al. [10] proposed Universal, Scalable, Efficient (USE), and easily manufacturable clocking scheme. It solved one of the most limiting factors of the existing clock schemes, the implementation of feedback paths and easy routing of QCA-based circuits. Consequently, USE considerably facilitated the development of the standard cell libraries and design tools for the QCA technology, besides avoiding the thermodynamics issues. There was a significant reduction in the area and delay in comparison with the existing advanced clocking schemes.

III. PROPOSED METHOD

Traditionally, QCA circuits regarding their logical function are implemented by the majority and inverter gates. However, our proposed work presents the novel XOR/XNOR logic gate design based on the cell level methodology [11]. The expected output is achieved by the influence of the cell towards each other. In contrast to previous XOR/XNOR designs, our proposed gates are not majority and inverter based. Figure.1 shows the schematic diagram of the proposed coplanar configurable cell. The XOR/XNOR gate consists of 12 QCA normal cells. Figure.2 shows the layout of XOR/XNOR gate in the polarization enable mode. When the polarization value of enable inputs ‘e’ is ‘0’, it performs the XNOR operation and when ‘e’ is ‘+1’, it performs XOR logic operation. The QCA layout of XOR gate is depicted in Figure.3.

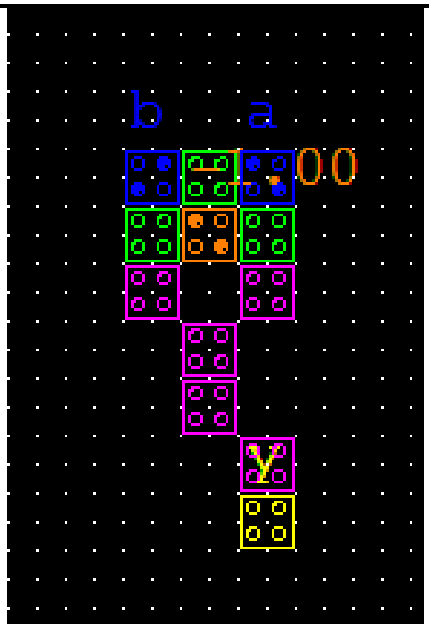

Figure.1 Schematic Diagram of the proposed coplanar configurable cell

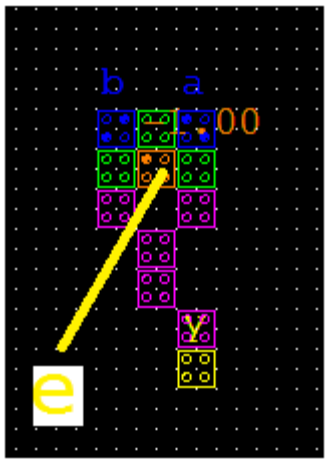

Figure.2 Layout of the XOR/XNOR gate in the polarization enable mode

A. Full Adder

Full adder is the basic element in performing all arithmetic and logical operations in ALU of a processor. To obtain an efficient architecture in terms of latency, area and delay here a coplanar implementation of Full adder has been designed which is given in Figure.4. Coplanar crossover is preferred over multilayer crossover because properly aligned regular QCA cells and 45° rotated cells that do not interact with each other could be used. Also the complex circuits could be realized easily using coplanar crossover. This adder comprises of an inverter and a Majority Voter gate. So, minimum number of logic gates has been preferred to minimize the QCA cell count and delay. Let the three inputs of full adder are A_0, B_0, and C_0 and their corresponding outputs are Sum and Carry. The inputs are given to the full adder using three-input MV gate. The sum output of full adder is derived as per following equations. Finally derived equations representing the sum and carry output of the full adder are given in the below equations

$$Sum = A_0'B_0'C_0 + A_0'B_0C_0' + A_0B_0C_0 + A_0B_0'C_0' \quad (1)$$
$$Sum = A_0'(B_0'C_0 + B_0C_0') + A_0(B_0C_0 + B_0'C_0') \quad (2)$$
$$Sum = A_0'(B_0 \oplus C_0) + A_0(B_0 \oplus C_0') \quad (3)$$
$$Sum = A_0 \oplus B_0 \oplus C_0 \quad (4)$$
$$C_{out} = MV(A_0, B_0, C_0) \quad (5)$$
$$C_{out} = (A_0B_0) + (B_0C_0) + (A_0C_0) \quad (6)$$

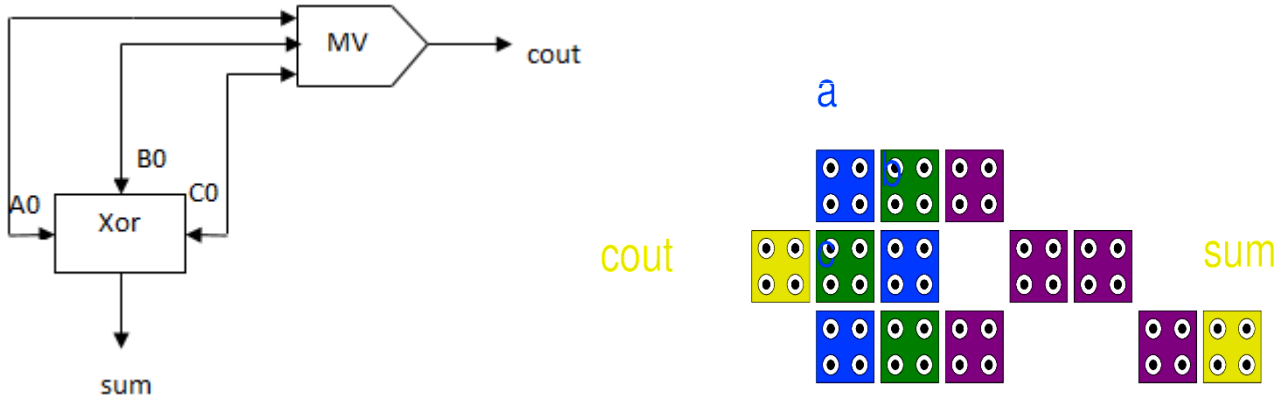

Figure.4 Schematic Diagram of 1-bit Full Adder

The proposed adder requires only thirteen QCA cells with two clock phases which was not yet achieved in previous design. The area required for the proposed full adder is about 0.009μm^2 which reinforces the implementation of the design. This design attains the lowest latency.

B. Elements of QCA

1) Quantum Dot

Quantum dots are nanostructures created from standard semi conductive materials such as Si/SiO. These structures can be modeled as quantum wells during real time manufacture. In order to implement a system that encodes information in the form of electron position it becomes necessary to construct a vessel in which an electron can be trapped and counted as there or not there.
A quantum dot acts a vessel and stores logic states not as voltage levels, but based on the position of individual electron. Electrons, once trapped inside the dot, do not alone possess the energy required to escape. Smaller a quantum dot is physically, the higher the potential energy necessary for an electron to escape. Techniques for fabricating quantum dots are electron-beam lithography, self-organization, and formation of depletion bubbles. Figure.5 shows the Quantum Dot.

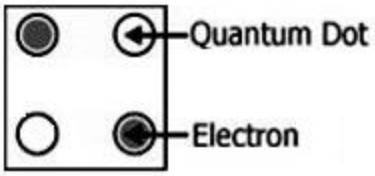

Figure.5 Quantum Dot

2) Cell structure

The cell is charged with two free electrons, which are able to tunnel between adjacent dots. These electrons tend to occupy antipodal sites as a result of their mutual electrostatic repulsion. Thus, there exist two equivalent energetically minimal arrangements of the two electrons in the QCA cell. These two arrangements are denoted as cell polarization. Binary information is encoded in the charge configuration of the QCA cell to represent logic 1 and 0.

Coulomb repulsion causes the electrons to occupy antipodal sites; the ground state charge distribution may have the electrons aligned along either of the two diagonal axes. The cell polarization has been defined as a quantity which measures the extent to which the charge distribution is aligned along one of these axes. The electrons exactly localized on sites two and four will result in P = + 1, while electrons on sites one and three yield P = -1. Figure.6 presents the QCA cell.

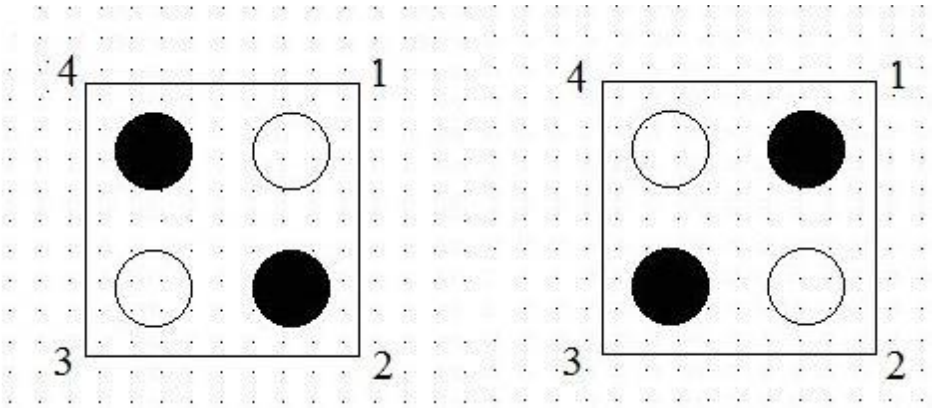

Figure.6 QCA Cell

3) Clocking Scheme

The signal flow in a QCA wire is controlled by clocks. To achieve controllable data directions, the cells within a QCA design are partitioned into the so-called clock zones that are progressively associated to four clock signals, each phase shifted by 90°.This clock scheme, named the zone clocking scheme, makes the QCA designs intrinsically pipelined. As the main source of the synchronization, a clock plays a key role in the QCA circuit. QCA circuit areas are organized into four clock zones.

QCA circuits use clock signals for transmission of signals and clock signals control the QCA circuits. It has four different phases. The four different phases are switch, hold, release and relax. Due to the tunnel barrier between the dots the clock signal stops tunneling and at the same time allowing the electrons to tunnel in the other clock phase shows the clocking scheme when an individual cell is affected with clock signal. Figure.7 depicts the clock phases.

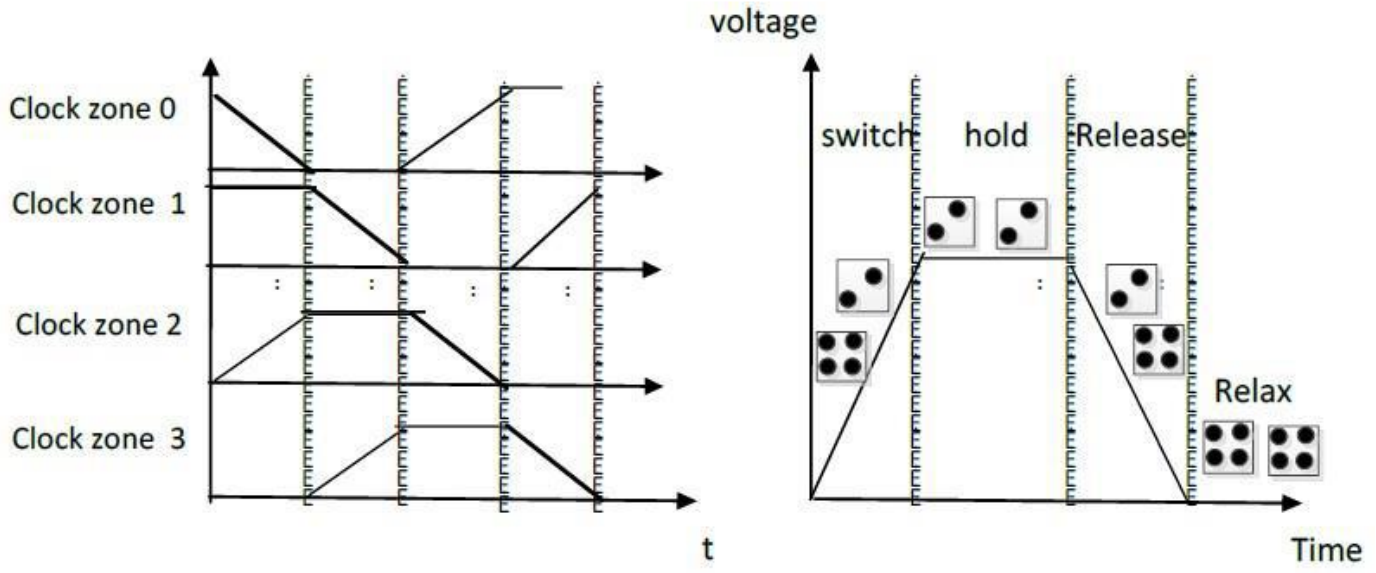

Figure.7 Clock Phases

During the switch phase, electron tunneling is stopped as the tunnel barrier between the dots rising, electrons thus tunneling is stopped and due to the polarization of its input the electron in the cell become localized Switching occurs by refreshing its state. During the hold phase as the barrier remains high thus no electron tunneling takes place. The polarized cells are latched. The cell is refreshed every cycle.

During Release phase, the electrons becomes free and the cell starts to lose its polarization due to the lowering of electron barrier. During the relax phase, the barriers are low, the electrons are free to tunnel and delocalize. There is a 900 phase shift from one clock zone to the next. In each clock zone, the clock signal has four states: high-to-low, low, low-to-high, and high. The cells in each clock zone behave like a single latch.

The cell begins computing during the high-to-low state and holds the value during the low state. The cell is released when the clock is in the low-to-high state and inactive during the high state. This allows information to be pumped through the circuit as a result of the successive latching and unlatching in cells attached to different clock cycles. These four clocking zones named as clock zone 0, clock zone 1, clock zone 2, clock zone 3; are implemented in QCA Designer tool. Each cell can be independently attached to any one of the four clocking zones.

4) QCA Wire

A series of QCA cells act like a wire. Adjacent QCA cells interact in an attempt to settle to a ground state determined by the current state of the inputs. Columbic forces will cause adjacent cells to interact. The state of the cells will always tend to the lowest energy. Transmitting information through a “wire” is done by forcing the polarization of a cell at one end. The polarization of the input cell is propagated down the wire. Any cells along the wire that are anti-polarized transmit the information.

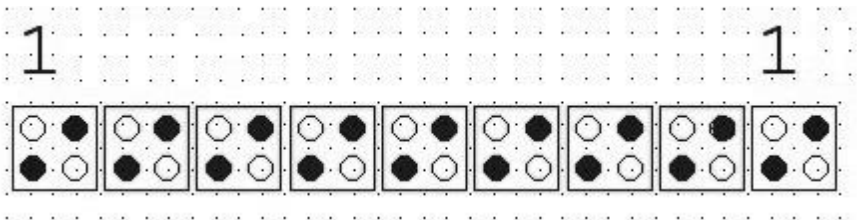

Figure.8 QCA Wire

5) Memory Loop

The clocking mechanism of QCA systems allows each clock zone to act as a memory cell, for one quarter clock period, so connecting four subsequent clock zones will produce a memory effect during one clock period. Given the basic memory cell construct, a value has to be inserted into the loop and read from it, in order to make it useful. Unlike CMOS memory, QCA has no equivalent for “static memory”. Memory storage in this design is based on circulating memory model. The memory loop is divided

into four consecutive clocking zones each latching in succession.

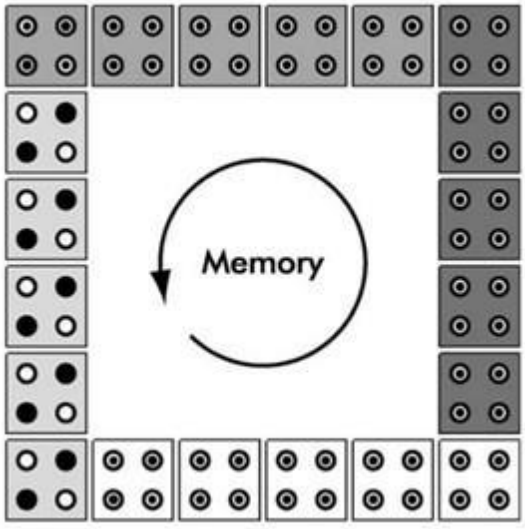

Figure.9 QCA Memory Loop

The stored memory continuously circulates in the loop. This means that information is transmitted through each cell and not retained. Each cell erases its own state every cycle of the clock. As a result, memory units must be created using loops of cells that continuously circulate the stored information. To be used as a memory cell, a loop of the cells is needed, in which a series of clock zones are used. The different shades of grey represent the different clocking zones to which cells are attached.

Each shade of gray represents a different clocking zone. The darkest shaded cells are attached to clock 0, and the others are represented by successively lighter shades. The cells which have polarizations, shown directly above them, are fixed to that polarization by denoting them as -1.00 and 1.00. Fixed polarization cells are required since the fundamental logic gate in QCA is the majority gate, by fixing one of its inputs to either a 1 or 0 we can generate the standard AND, OR operations.

6) Majority Logic Synthesis

The Majority Gate (MG) is a result of majority logic synthesis. Given three inputs *a*, *b*, and *c*, the MG performs the logic function provided that all input cells are associated to the same clock signal clk*x* (with *x* ranging from 0 to 3), whereas the remaining cells of the MG are associated to the clock signal clk*x*+1. The output cell will polarize to the majority polarization of the input cells. The majority gate performs a three-input logic function. Assuming the inputs is A, B and C, the logic function of the majority gate is

$$m(A, B, C) = A \cdot B + B \cdot C + A \cdot C \quad (7)$$

A separation of at least two cells between signal interconnect wherever the possibility for cross-talk exists; an example is the gap between the memory loop and some of the fixed polarization cells. There are some areas in the design where this was not necessary; e.g., interconnect attached to clocks 0 and clock 2. In this case, there is no problem with cross-talk because the two interconnects do not simultaneously transmit.

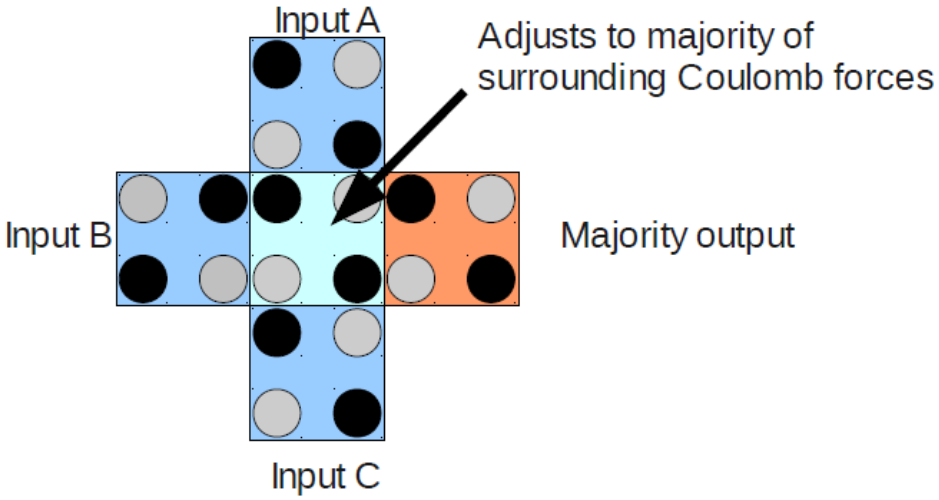

Figure.10 Majority Voter

Using this technique, minimal majority expression and an optimal QCA layout can be obtained. Furthermore, this method removes all the redundancies that are produced in the process of converting a decomposed network into a majority network.

7) Logic Gates in QCA

Large digital circuits using quantum-dot cellular automata (QCA) cells can be designed by means of basic design of AND, OR and NOT gates. When any one of the three inputs is fixed to one, it performs OR operation; while any one of the three inputs is fixed to "0", it performs AND operation. By fixing the polarization of one input as logic "0", AND gate is obtained. Figure.11 presents the AND gate and Figure.12 shows the OR gate in QCA. By fixing the polarization of one input as logic "1", OR gate is obtained. Figure.13 shows the XOR conversion.

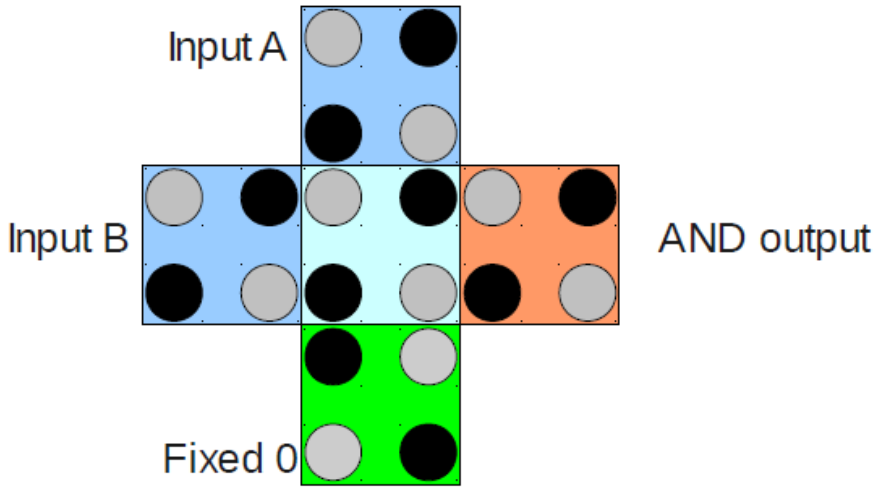

Figure.11 AND gate in QCA

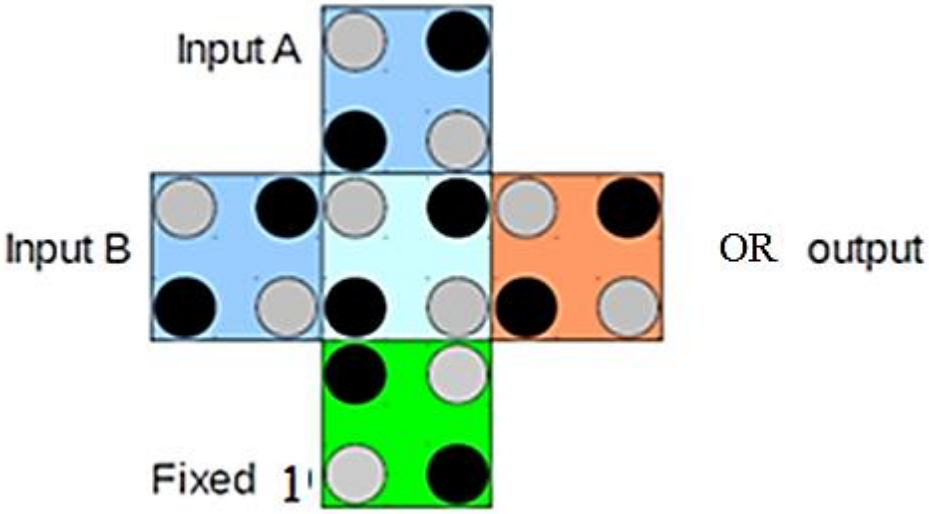

Figure.12 OR gate in QCA

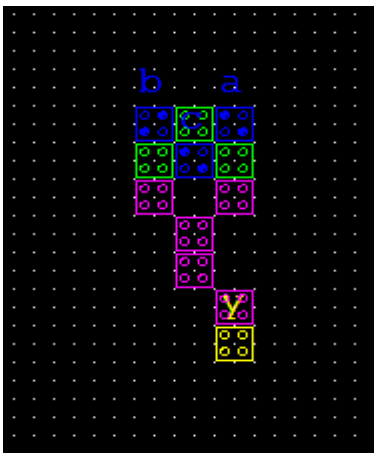

Figure.13 XOR conversion

IV. PERFORMANCE ANALYSIS

A. Design Tool

A QCAD Designer is a well-known simulation tool used to create QCA circuits and verifying its functionality [15]. This tool provides two simulation engines they are bistable engine and coherence vector engine. By performing simulation, the bistable is more favorable than the coherence vector engine usually produces the results. Four clocking zones are implemented in QCA Designer tool and each cell can be independently attached to any one of the four clocking zones.

The QCA cells are 18-nm wide and 18-nm high; the cells are placed on a grid with a cell center-to-center distance of 20 nm; there is at least one cell spacing between adjacent wires; the quantum-dot diameter is 5 nm; the multilayer wire crossing structure is exploited; a maximum of 16 cascaded cells and a minimum of two cascaded cells per clock zone are assumed. The bistable engine is used for simulations with the options shown. QCA Designer is the "state of the art" QCA layout editor and simulator.

B. Simulation Results

In this work, the proposed logic gate is implemented and simulated by using QCADesigner software. It is clear than this proposed structure could implement XOR and XNOR logic function by controlling the values that enable inputs. The simulation results of XOR and XNOR logic functions are shown in Figure.14. When a = 0, b = 0, the output will be f = 0. When a = 0, b = 1, the output will be f = 1. Thus, all the values of the output bit 'f' are in accordance with inputs 'a' and 'b'. This result satisfies the theoretical values of XOR gate, which indicates the accuracy of the design. Similarly, it is seen that when a = 0, b = 0, the output will be f = 1. When a = 0, b = 1, the output will be f = 0. Thus, all the values of output bit 'f' are in accordance with inputs 'a' and 'b'. This result satisfies the theoretical values of XNOR gate, which indicates the accuracy of the design.

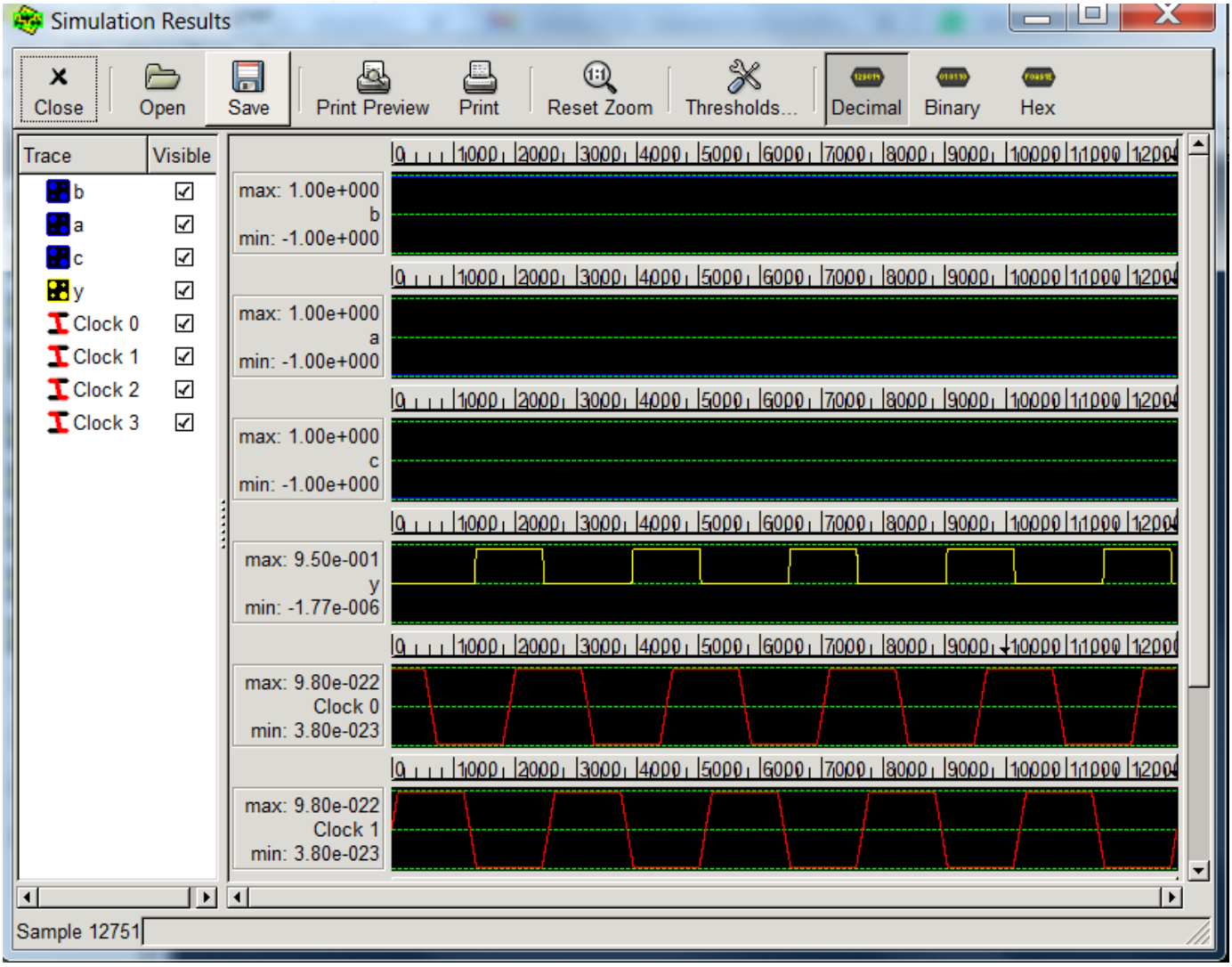

Figure.14 Input and output sequence of configurable cell

The proposed XOR/XNOR logic gate is used as a module to implement large and complex logic circuits (such as adder, comparator, multiplexer, etc.). In this way, it is theoretically possible to design efficient circuits. Compared with the existing XOR designs [16-18], the proposed XOR design has less numbers of cells and occupies lesser area. The proposed XOR gate has a single latency (e.g. 0.25 clock cycle), while 0.75 clock cycle, 0.5 clock cycle and 0.5 clock cycle are reported in the works [19-21]. Figure.15 and Figure.16 illustrate the input and output sequences. Figure.17 presents the proposed 4 bit cell and Figure.18 shows the bistable vector setup.

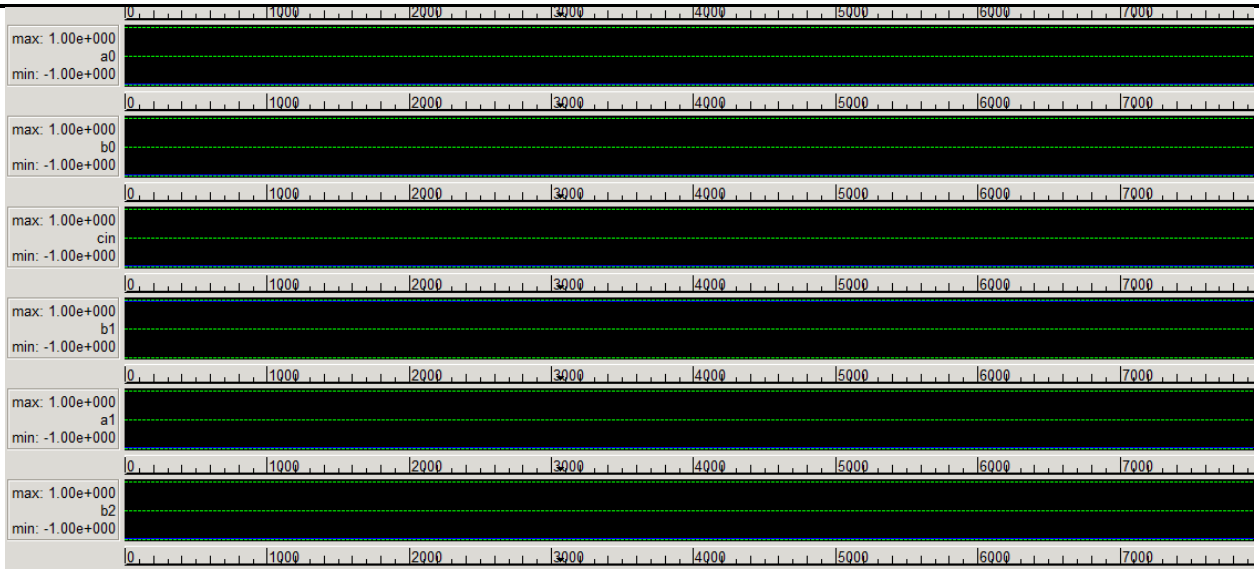

Figure.15 Input Sequence

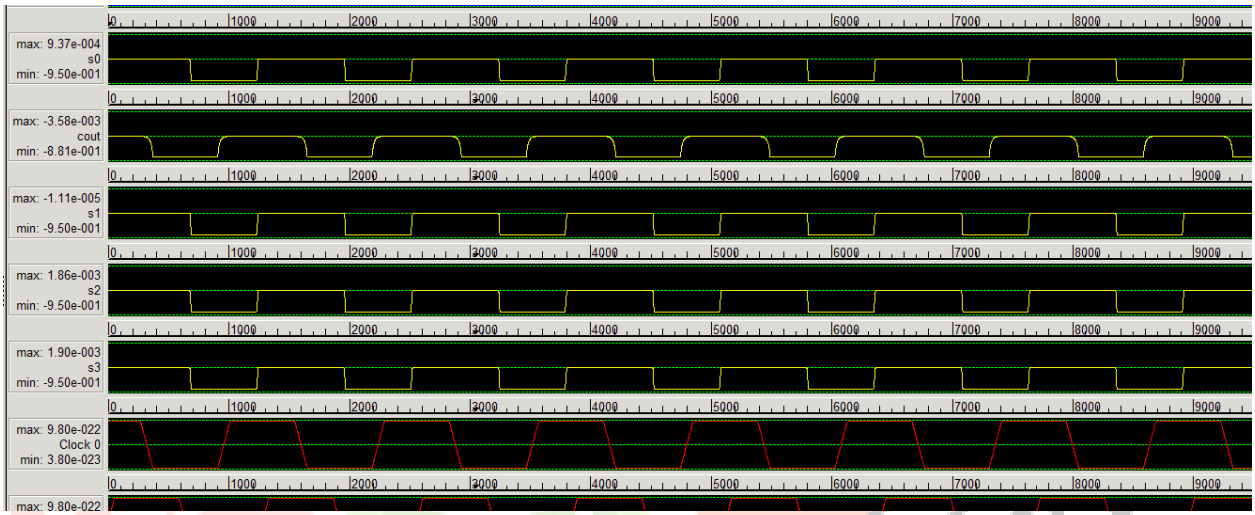

Figure.16 Output Sequence

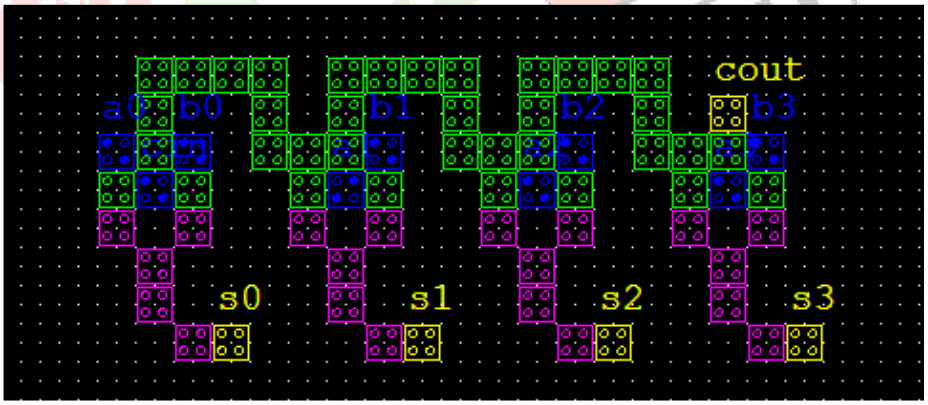

Figure.17 Proposed 4-bit cell

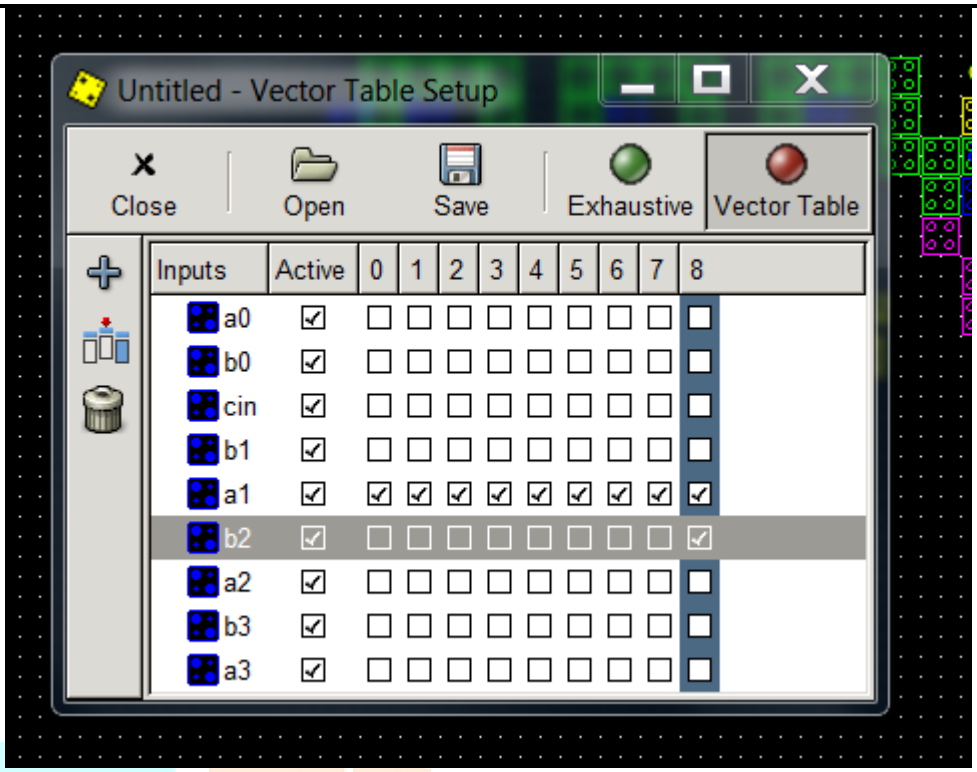

Figure.18 Bistable vector setup

C. Comparative Analysis

Table 1 presents the comparative analysis of the gate count, cell count, area and latency for the existing and proposed works. The proposed design required less number of gates, cells, occupied area and latency than the existing works.

Table 1 Comparative analysis of the gate count, cell count, area and latency for the existing and proposed works

Works	Gate count	Cell count	Area	Latency
A. M. Chabi et al [12]	4	29	0.03	0.75
S. Sheikhfaal et al [13]	3	32	0.25	1
M. Balali et al [14]	1	14	0.14	0.5
K. Walus et al [15]	5	60	0.09	1.5
M. T. Niemier et al [16]	5	54	0.08	1.5
S. Hashemi et al [17]	3	67	0.06	1.25
Proposed	1	12	0.01	0.5

V. CONCLUSION

In this work, a novel XOR/NOR logic gate is introduced. The study has a direct application in designing some usefully programmable circuits in QCA domain where efficient is an objective. First, a novel XOR/XNOR logic gate has been presented and then several complex circuits have been proposed based on the XOR/XNOR logic gate. The performance of the proposed XOR/XNOR logic gate was verified by physical verification and simulation. It was shown that the proposed XOR/XNOR logic gate has the less numbers of cells and less area. The cost of the proposed XOR/XNOR design is 0.01, which is the lowest overall cost. The proposed XOR/XNOR can be used as a basic logic gate in designing of QCA based large and complex circuits (1-bit full adder, 4-bit adder) so it is very flexible to be used for complex circuit design.

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