A NOVEL FIR FILTER DESIGN USING GDI

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TECHNIQUE BASED HYBRID ADDER AND BOOTH MULTIPLIER

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Abstract: Digital filters are used for computation, band selection, signal preconditioning, signal analysis and estimation, etc. Hardware with high efficiency are required to cope up with the rapid growth in digital signal processing applications. Digital filters are classified into two types namely, Finite Impulse Response (FIR) and Infinite Impulse Response (IIR). Due to the linear phase response and inherent stability, FIR filters are more commonly used than IIR filters. The digital filter primarily separates the unwanted signal from the wanted signal. Hybrid adder is the combination of two adders or having a logic style design in the existing adder. The multiplier using the Booth algorithm is a well-known technique for high-speed and low-cost multipliers. The hybrid adder and booth multiplier has improved performance when compared with other adders and multipliers. In this paper, a novel FIR filter is designed using GDI technique-based hybrid adder and booth multiplier. The 8-bit and 16-bit FIR filter s are designed using the proposed GDI technique-based hybrid adder and booth multiplier which saves 22.83% of power and 31.07% of delay. The proficient FIR filter using GDI technique has favorable circumstances over the conventional FIR filter. Simulation is done using Tanner EDA tool in 180nm technology and the results obtained shows a significant improvement in power consumption and delay.

Index Terms **- Carry Increment adder, Carry Skip adder, Finite impulse response (FIR) filter, Gate Diffusion Input (GDI) Technique, Hybrid adder, Modified Booth multiplier.**

I. INTRODUCTION

Very Large-Scale Integration is the process of creating an Integrated Circuit by combining thousands of transistors into a single microchip. Quick advancement in the VLSI fabrication process brings about the expansion of densities of the integrated circuit. With the progression of innovation that is occurring in the universe, the increase of power dissipation has ended up the major impediment against the further advancement of VLSI circuits.

Hardware with high efficiency are required to cope up with the rapid growth in digital signal processing applications. Digital filters are used for computation, band selection, signal preconditioning, signal analysis and estimation, etc. Digital filters are classified into two types namely, Finite Impulse Response (FIR) and Infinite Impulse Response (IIR). Due to the linear phase response and inherent stability, FIR filters are more commonly used than compared to IIR filters. The digital filter primarily separates the unwanted signal from the wanted signal [1].

The FIR filter is realized using different combinations of adder and multiplier blocks. Faster adders and multipliers result in faster operation of the FIR filter. Tanner EDA tool is used to perform power consumption and delay analysis on the digital designs. Such analysis is used to choose optimal combinations of adders and multipliers.

Addition is one of the fundamental arithmetic operations. Adders mainly used in VLSI systems like DSP architecture specified applications and microprocessors. To determine the overall performance of the system which is created by the critical path in the adders. To enhance the performance of the adder cell, the hybrid adder is one of the significant goals.

Adder is a hub element of the complex arithmetic logic circuits like addition, division, multiplication, exponentiation, and so forth. The requisition for the Very Large-Scale Integration (VLSI) system is blooming. If a device becomes the most important brain then it is capable of computing FPU and ALU. ALU is accountable for all the computations which have been used for logical calculations such as division, subtraction, multiplication, logical operations and addition. [4].

The semiconductor industry noticed an unforeseen growth of integration of worldly-wise multimedia-based applications into electronic gadgetry like mobiles since the last decade. But the concern of this arena is to reduce the power consumption which gets increasing beyond the operating frequency range. Delay is one of the problems not only this the consumption of power and also the consumption of area is the major problem faced by the engineers.

Different types of logic styles are apt to esteem, one performance slant to the expense of the others. The styles which are used in the logic gates influence the size, power consumption, speed and complexity that takes place in the wiring of the circuit at the end of the day. Circuit delay represents the inversion levels, series-connected transistors and the size of transistors with the capacitors which is connected with intra cell wire. Circuit size is represented by the number of transistors used and the size of it with wiring complexity taken place while executing the process. Some adders were designed using a single logic style instead some adders were designed by using more than one logic style during the implementation process.

Adding two numbers was done by a digital circuit is also known as an adder. In computers and processors, adders were used in Arithmetic logic units or ALU for the purpose of addresses calculation, increment and decrement operators, table indices and similar operators too.

The most important components used in ALU, FPU and multiplier are adders. In filter design, adder and multiplier were the important parts. so to improve the speed of these kinds of devices the circuits which are heavily used in these devices should be replaced that is none other than adders itself. Adders are classified into various types. They are Half adder and Full adder [4].

HALF ADDER:

A device which can compute the addition of two bits as i/p and produce the sum and the carry then it is known as half adder. This half adder can be designed by using 2 logic gates such as AND gate and Ex-OR gate.

LOGICAL OPERATION:

- The output of the sum i.e., EX-OR gate becomes high if one of the i/p values such as A or B is high i.e., 1.
- The sum will be 0. If both the inputs A and B are high or low.
- If both the inputs are high then the output of the Carry bit will also be high.

The equations the sum and carry of the half adder is represented below,
The sum can be represented as:
Sum = A'B+AB'
The carry can be represented as:
Cout = A.B

FULL ADDER:

If a device has the ability to compute three input bits and produce two outputs which are denoted as the sum and carry then it is called a full adder. Full adder is a combinational circuit which is used to add the binary values with not only the two input instead with three inputs and the third input is named as carry-in and the output is represented as carry out. It also performs the addition operation of three inputs, A, B and Carry in (Cin) [4]. The input combinations can be represented in eight possible ways and each possible way has its own sum and carry out (Cout). The full adder circuit is designed by using simple logic gates.
The equations of the sum and carry of the full adder are represented below,
The sum can be represented as:
Sum = A XOR B XOR C
The carry function is given by:
Cout = AB + BC + CA

There are so many ways to design Full Adder. Complementary metal-oxide devices (CMOS), Transmission Gate (TG) logic and Complementary pass logic (CPL) were all some logics that are used to design the full adder circuit.

As the demand for high computational speed along with compact area and low power consumption is becoming indispensable, it's very important for the most fundamental components to be highly efficient.

A hybrid adder is designed by combining two different adders or else by implementing a new logic style in the conventionally existing adders. By using two adders the addition is performed in this hybrid adder. The addition of the Least Significant Bit (LSB) is carried out by one adder and the Most Significant Byte (MSB) process is done by another adder. The main objective of this paper is to design a novel FIR filter by using the designed hybrid adder is to make it more efficient than an individual adder

ADVANTAGES OF HYBRID ADDER:

- High Speed,
- Reduce Power consumption,
- Reduction transistor counts,
- Minimize the delay.

APPLICATIONS OF HYBRID ADDER:

- Cellular phones,
- Smart cards,
- Laptops.

RADIX-4 BOOTH MULTIPLIER

The multiplier using the Booth algorithm is a well-known technique for high-speed and low-cost multipliers. Many types of research have been taken place on booth multiplier because of the radix - 4 booth multiplier. Even though it reduces the output bit into half, it also increases the time of compression [21]. In order to get a better system performance, the circuit of the radix-4 Booth multiplier must be improved.

The modified multiplier scheme is commonly in the CPU and the DSP processor design. Encoding, array, parallel and series multiplier are some types of multipliers. The Series multiplier has the simplest structure than others, the parallel multiplier is of higher speed, if it is based on symbol operation then the matrix multiplier is no good and the encoding one is much more efficient when it is used on symbol operation [21]. Therefore, the encoder and the decoder are modified in order to reduce area and increase the whole speed and further GDI technique is also used.

In this paper, the novel gate diffusion input (GDI) technique-based hybrid adder is proposed and implemented in the radix-4 booth multiplier circuit. Further In this paper, the design of a 16-tap finite impulse response (FIR) filter using GDI technique-based hybrid adder and radix-4 booth multiplier is proposed which has several advantages over the ordinary adders and multipliers. The 16-tap FIR filter using GDI technique-based hybrid adder and radix-4 booth multiplier is designed for DSP applications that have high speed and low power consumption compared with the conventional adders and multipliers.

OBJECTIVE

- ➢ To propose GDI technique-based hybrid adder to improve power consumption and delay.
- ➢ To implement GDI technique-based hybrid adder in radix-4 booth multiplier.
- ➢ To implement the proposed hybrid adder and booth multiplier circuitry in the 16-tap finite impulse response (FIR) filter.
- ➢ To reduce the power consumption and to improve the speed and overall performance of the 16-tap FIR filter using the proposed technique.

II. GDI BASED FIR FILTER

Digital filter is of two types one among them is FIR filter which is used in Digital Signal Processing (DSP) applications and the other type is IIR. The disadvantage of this filter is that it requires a higher filter order than the IIR filter to reach the given performance level. Correspondingly, the delay of these filters is often much greater than for equal performance IIR filters. Due to its low power consumption and high speed, the GDI technique based Hybrid adder and Radix-4 booth multiplier are used to design the FIR filter.

FIR FILTER

One of the most extensively used filters is the FIR filter. They are often used in digital communication systems. For example, a digital radio receives and down-converts analog signals to an intermediate frequency (IF). It then converts the analog output of the IF stage to a digital signal followed by the use of an FIR filter to select the desired frequency. The number of taps in the FIR filter is directly proportional to the stopband attenuation of the FIR filter. Thus, as the number of taps of the filter increases, the filter attenuates unwanted signals better. But the increase in the number of taps also increases the hardware complexity and power dissipation of the filter. This trade-off exists in the filter design.

FIR is a filter whose response to any finite length input is of finite duration in signal processing because it returns to zero in a finite time but in IIR filter internal feedback occurs and also it may continue to respond indefinitely

The Nth order FIR filter's impulse response lasts exactly at N+1 sample (from the first non-zero element through the last non-Zero element) before it settles in zero. FIR filters can be analog or digital and continuous-time or discrete-time.

For a formative discrete-time FIR filter of order N, for the most recent input the values were given by the output sequences with a weighted sum:

$[n] = b0[n] + b1x[n-1] + \cdots + bnx[n-N]$

$= \sum bi\ .\ [n-i]\ N\ i=0$

where:

- ✓ $[n]$is the input signal,
- ✓ $[n]$is the output signal,
- ✓ is the filter order; an Nth-order filter has (N+1) terms on the right-hand side
- ✓ is the value of the impulse response at the i'th instant for $0 \le i \le N$ of an Nth-order FIR filter. If the filter is a direct form FIR filter then is also a coefficient of the filter.

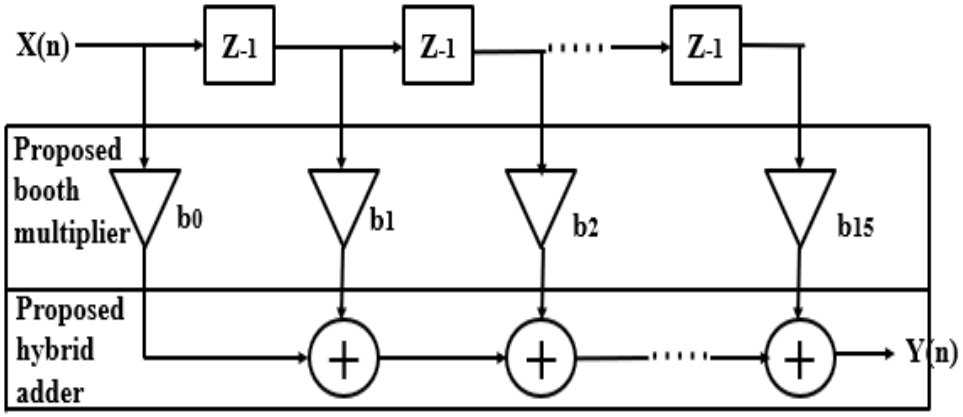

Fig 1 Circuit diagram of proposed 16-Tap FIR filter

Figure 1 illustrates the circuit diagram of proposed 16-tap FIR filter. The proposed FIR filter consists of delay, multiplier and adder. The proposed hybrid adder is implemented in the booth multiplier to reduce the power consumption and delay over the conventional FIR filter design with high speed and low power consumption. A 16 tap FIR filter is designed using Tanner EDA tool to check functionality of the filter which can be used for DSP applications.

III. DESIGN OF GDI BASED HYBRID ADDER AND MULTIPLIER FOR FIR FILTER

The circuit diagram of the 4-bit Hybrid adder is shown in figure 2. It consists of two adders. The hybrid adder is either designed by combining two separate adders or by implementing a logic styles in the existing adder. The two adders which are used for the design of hybrid adder are Carry skip adder and Carry increment adder.

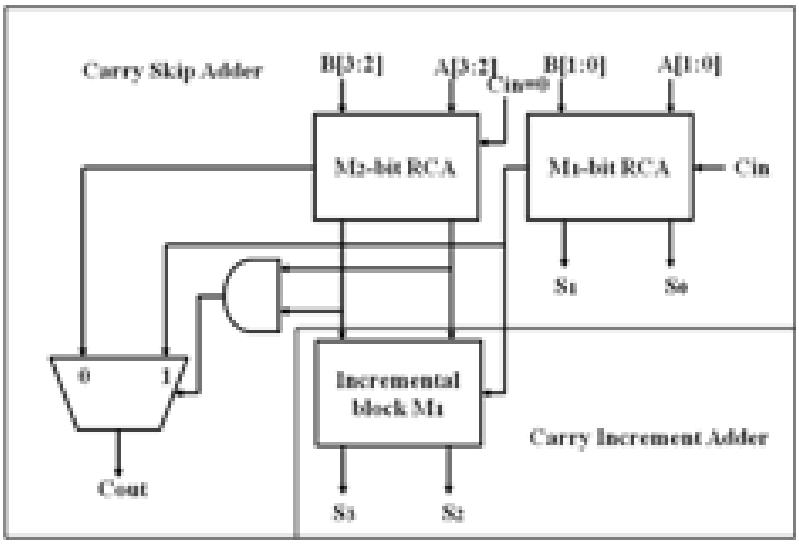

Fig 2 Circuit diagram of 4-bit Hybrid Adder

In this proposed, hybrid adder the Carry Skip adder consists of Ripple Carry Adder (RCA), AND gate and Multiplexer. The RCA circuit is designed simply by cascading Full adder blocks. The carry-out of any full adder is propagated to the next stage as carry-in and the calculation continues in the next block.

ADVANTAGES OF CSkA

- ✓ Critical path delay is much smaller than RCA.
- ✓ Efficient in terms of power consumption and area usage.
- ✓ Power delay product is smaller than those of carry select adder and parallel prefix adder structure.
- ✓ Benefits from relatively short wiring lengths as well as a regular and simple layout.

The AND gate is used to generate the select line input for the Multiplexer. The input of the AND gate would be the propagate value of the M2-bit RCA. The input of the Multiplexer would be the Cout of the M1-bit RCA and the M2-bit RCA.

The Conventional Full adder and Multiplexer are the two main peripheral components of this hybrid adder: by the optimized design of these two components low power high speed hybrid adder can be obtained. The Figure 2 shows the Circuit diagram of 4-bit Hybrid adder.

A multiplexer (or mux) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. A multiplexer of inputs has select lines, which are used to select which input line to send to the output. Multiplexers are mainly used to increase the amount of data that can be sent over the network within a certain amount of time and bandwidth. A multiplexer is also called a data selector. Multiplexers can also be used to implement Boolean functions of multiple variables. In

analog circuit design, a multiplexer is a special type of analog switch that connects one signal selected from several inputs to a single output. In digital circuit design, the selector wires are of digital value. In the case of a 2-to-1 multiplexer, a logic value of 0 would connect I0 to the output while a logic value of 1 would connect I1 to the output. In larger multiplexers, the number of selector pins is equal to where is the number of inputs. Figure 3 represents the circuit diagram of 2 to 1 Multiplexer. A 2-to-1 multiplexer has a boolean equation where 'A' and 'B' are the two inputs, S is the selector input, and Z is the output,

$Z = (A.S') + (B.S)$

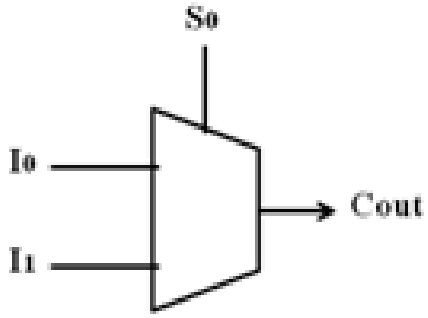

Fig 3 Circuit diagram of 2 to 1 Multiplexer

A Carry Increment Adder, an adder implementation that uses HA blocks for carry propagation. Carry propagation in HA is much faster than that of FA. That's why the total propagation delay in CLA is much less that other adder circuits. First two sum from the RCA is directly taken from the block, but rest is calculated from the carry-out of the first block and rest input through conditional incremental circuit. Second block will continue the operation by summing and creating carry-out. Incremental circuit is containing Half Adders. The increment operation will take place based on the carry-out of the 1st block.

As carry propagation delay is less in half adder than in full adder so, the total propagation delay through the increment adder is less. As the incremental circuit contains Half Adder it takes less time to generate the carry, so the delay is less than RCA circuit.

ADVANTAGES OF CIA

- ✓ Circuit complexity is less.
- ✓ It has a simple and regular layout in comparison with Carry Look Ahead Adder.
- ✓ Effective in higher (more numbers of) bit operation.

The GDI Logic based full adder consists of only 10 transistors to implement the sum and carry function. The Circuit delay is determined by the number of inversion levels, the number of transistors in series, transistor sizes (i.e., channel widths), and the intra cell wiring capacitances. Circuit size depends upon the number of transistors, their sizes and on the wiring complexity. Figure 4 represents the Circuit diagram of 4-bit Hybrid adder using GDI technique.

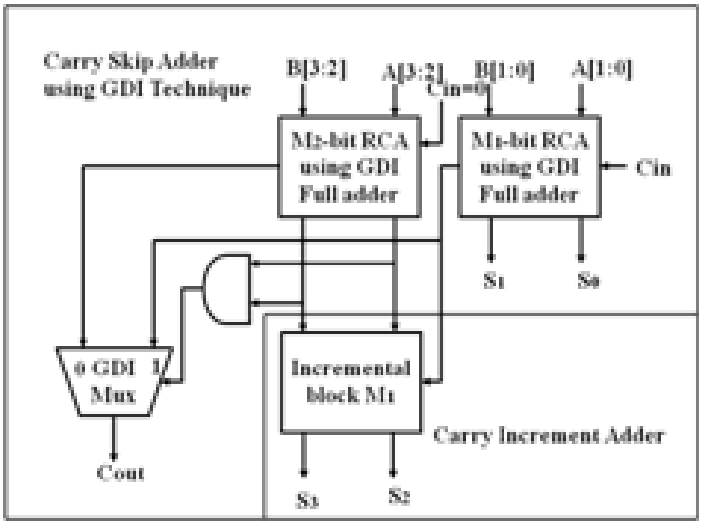

Fig.4 Circuit Diagram of 4-bit Hybrid adder using GDI Technique

In GDI logic based full adder, only 10 transistors are used to implement the sum and carry function. The sum and carry cell are implemented in a cascaded way i.e. firstly the XOR cell is implemented and then using that XOR as input, sum as well as carry cell is implemented. For GDI adder the sum as well as carry cell is designed using GDI technique. The advantage of this adder is if this adder is to be used in a wide range of supply voltages (for example 0.8V-3V), then this GDI design is suggested to use. Figure 5 represents the circuit diagram of Ripple carry adder using GDI technique.

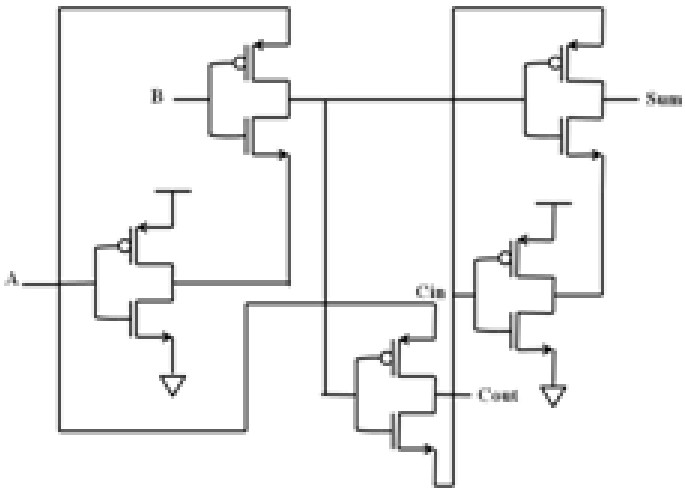

Fig.5 Circuit diagram of Ripple carry adder using GDI technique

The GDI method is based on the use of a simple cell. At the first look the design is seems to be like an inverter, but the main differences are the connections. Figure 6 shows the circuit diagram of GDI Multiplexer. GDI multiplexer consists of only two transistors. By using this GDI technique, the power consumption is reduced with the delay because it use minimum number of transistors to calculate the output.

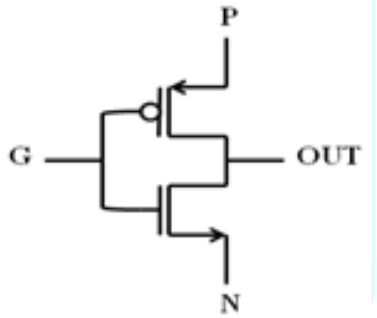

Fig 6 Circuit diagram of GDI Multiplexer

Incremental circuit is a part of the hybrid adder using GDI techniques. The incremental circuit that uses half adder (HA) blocks for carry propagation. Carry propagation in HA is much faster than that of full adder (FA). That's why the total propagation delay in CLA is much less that other adder circuits. First two sum from the RCA is directly taken from the block, but rest is calculated from the carry-out of the first block and rest input through conditional incremental circuit. Second block will continue the operation by summing and creating carry-out. Incremental circuit is containing Half Adders. The increment operation will take place based on the carry-out of the 1st block.

As carry propagation delay is less in half adder than in full adder so, the total propagation delay through the increment adder is less. As the incremental circuit contains Half Adder it takes less time to generate the carry, so the delay is less than RCA circuit.

RADIX-4 BOOTH MULTIPLIER USING GDI TECHNIQUE

The proposed radix-4 Booth multiplier using Gate diffusion input technique consists of the 3-bit Booth encoder/decoders, the Sign Extension Trick, and the hybrid adder which is based on Gate diffusion technique. The block diagram of 4-bit Radix-4 booth multiplier using GDI technique shown in fig.7 This proposed GDI based Radix-4 Booth multiplier consumes low power and delay improvement rather than conventional Radix-4 booth multiplier.

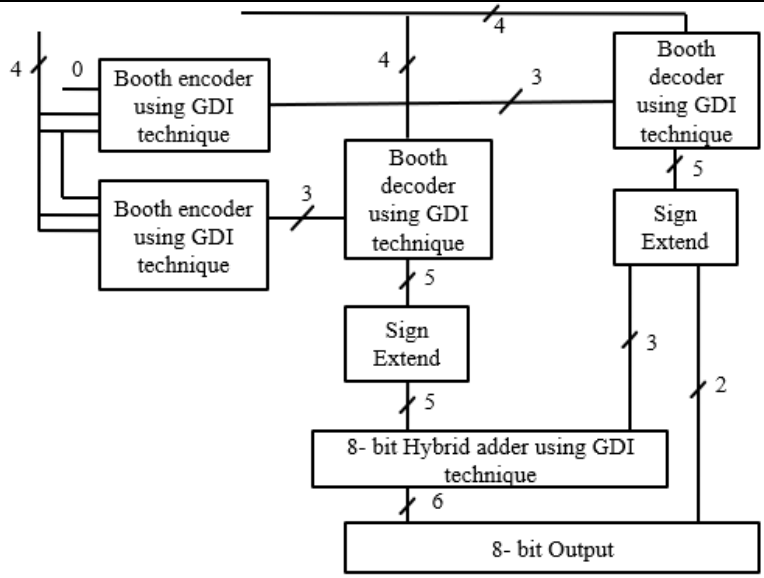

Fig 7. Block diagram of 4-bit Radix-4 booth multiplier using GDI technique

ADVANTAGES

- ➢FIR filters can have exactly linear phase.
- ➢FIR filters are always stable.
- ➢FIR filters design methods are generally linear.
- ➢FIR filters can be realized efficiently in hardware.
- ➢FIR filters start up transient have finite duration.

IV. RESULTS AND DISCUSSION

The novel FIR filter is designed using gate diffusion input (GDI) technique-based hybrid adder and booth multiplier. The proposed FIR filter shows a considerable reduction in power consumption and delay. This proficient low power and high-speed FIR filter is designed using the proposed hybrid adder and booth multiplier for DSP applications. The following tabulations are carried out In this paper to justify the performance of the proposed FIR filter. The implementation of FIR filter is done by using Tanner EDA software.

TABLE I. Comparison table for different logic based full adders simulated in Tanner EDA tool in terms of power and delay.

Design	**Power (µW)**	**Delay (ns)**
GDI adder	0.827	0.527
Conventional Full adder	1.835	10.17
Proposed Hybrid adder [9]	21.88	19.91
Proposed PTL-GDI adder [15]	2.46	9.98

From table I it is observed that compared to other full adders GDI adder consumes low power and delay is also reduced. Therefore, GDI adder is used in the ripple carry adder of the proposed Hybrid adder.

TABLE II. Comparison table for different types of adder in terms of power and delay

Design	Size	Power	Delay (ns)
GDI based hybrid adder	8	29.24 µW	1.994
	16	85.34 µW	1.036
Carry Look ahead	16 bits	2.0053 mW	1.809
Carry Increment	16 bits	3.000 mW	2.026
Carry Skip	16 bits	2.005 mW	3.047
Proposed Carry Skip [1]	16 bits	3.018 mW	2.05
Proposed SQRT CSLA [12]	16 bits	19665.2 mW	5.55

From table II it is observed that GDI based hybrid adder give faster results. Also their delay does not increase significantly in proportion to the number of bits they operate on. This is of significance in the design of fast filters.

TABLE III. Comparison table for different multiplier using different adders in terms of power and delay

Design	Size	Power	Delay (ns)
GDI based Booth	8	471.899 µW	7.475
Conventional Booth	8	549.687 µW	29.139
Modified booth [17]	-	11 mW	26.103
Array using Shannon [3]	4	0.5398 W	1.20
Baugh-Wooley using Shannon [3]	4	0.4925 W	0.84

TABLE III. Comparison table for different FIR filter in terms of Tap, power and delay

Design	Tap	Power	Delay (ns)
Using Proposed GDI based Hybrid adder and Booth multiplier	8	117.171 µW	3.010
	16	557.244 µW	3.580
Using Altered Carry Skip adder and Vedic multiplier [1]	16	7.282 mW	7.733
Conventional method MAC [11]	5	17.92 µW	5.09
	9	36.39 µW	6.35
Proposed method MAC [11]	5	13.95 µW	5.44
	9	27.42 µW	7.37

The tanner EDA tool is used to design the schematic diagram for proposed 16-tap FIR filter as shown in figure 8

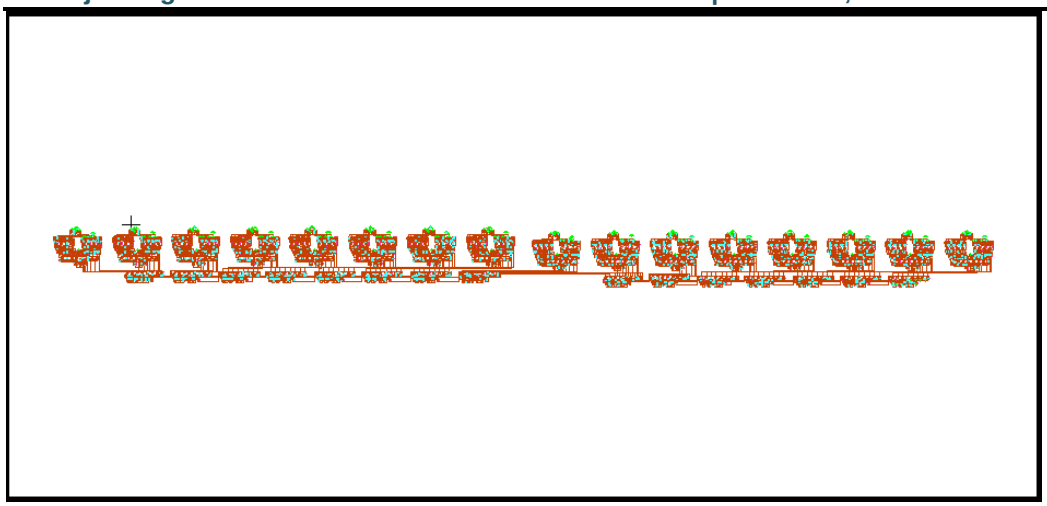

Fig 8 Schematic diagram for proposed 16-tap FIR filter

V. CONCLUSION

In this paper, a low power and high-speed FIR filter using GDI technique-based hybrid adder and booth multiplier was designed. Adder and Multiplier are the two main peripheral components of the FIR filter which were designed using novel GDI technique for a new low power high speed FIR filter. The 16-bit hybrid adder design using the GDI technique has 85.34 µW of power and 1.036 ns of delay. Similarly, the Booth multiplier using the GDI Technique saves 14.15% of power and 24.59% of delay compared to conventional methods. In this paper, the design of 8-Tap FIR filter using GDI technique has 117.171 µW of power and 3.010 ns of delay and similarly for the design of 16-Tap FIR filter adder, GDI technique has 557.244 µW of power and 3.580 ns of delay. Thus, from the simulation results it was observed that the proposed FIR filter using GDI technique has a low power consumption and high speed.

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