IJCRT.ORG ISSN : 2320-2882

INTERNATIONAL JOURNAL OF CREATIVE RESEARCH THOUGHTS (IJCRT)

An International Open Access, Peer-reviewed, Refereed Journal

VLSI Architecture of Reconfigurable hard decision Viterbi Decoder

1N.GLORY PRISCILLA 2D.VIJAYA SRI 3DR.M.RAMESH PATNAYAK

1Phd scholar, Andhra University,Visakhapatnam,AP,INDIA.

2Assistant Professor, Satya Institute of Technology and Management.

3Professor,Department of Instrument Technology, Andhra University, Visakhapatnam,AP,INDIA.

ABSTRACT:

In order to control errors in data transmission through a noisy channel Viterbi algorithm has served as a powerful tool meant for interpreting the conventional codes. It is centred on extreme possibility algorithm for interpreting the data? While coming to hardware implementation of Viterbi algorithm became crucial as it drain large amount of assets because of its complexity. This paper confers the implementation of an efficient VHDL execution of a Viterbi decoder by means of the concept of pipelining to diminish the critical path. There by improving the operating frequency of the design and improving the through put using Modalism and Xilinx ISE tools for simulation and synthesis of modules respectively.

KEYWORDS: Error correcting code, convolutional codes, Viterbi algorithm, convolutional codes.

I.INTRODUCTION

Viterbi Decoder (VD) mostly recommended aimed at fault detection and rectification in satellite, broad space communication which is identified and chosen as a competent technique used for the realisation of utmost likely hood interpreting the convolutional codes. It is known to be some of the competent techniques for interpreting convolutional codes. In order to convey message through piercing conduit convolutional code proposes far improved outcomes now compare to block codes .Specific spare bit included on or after encoder sideways aimed at decreasing the chance of mistakes in the gesture to find survivor route which is accumulate in Survivor Path Metric Unit. .Continuous stream of bits are encoded by the convolutional coding technique which is also an efficient method for solid conclusions. Viterbi decoder (VD) primarily includes 4 elementary building blocks: Branch Metric Unit (BMU), Add Compare Select Unit (ACSU), Survivor Path Memory (SPMU) and Trace Back Unit (TBU), purpose of BMU be there to define the branch metric, branch metric is the hamming distance among whole obtained also predictable signals .ACS Unit computes the selection of the bit which is

Trace Back Unit meant for point the actual bit. That is used in the encoder input .So many mechanisms used for implementation of area effective and great speed Viterbi decoder. Many bandwidths – active systems uses Trellis coded modulation (TCM) schemes. Naturally, hires a high-rate convolutional code pointers towards more difficulty in Viterbi decoder on behalf of TCM decoder , although uncertainty constriction length of the convolutional code employed in a 4-dimentional TCM structure insightful space communications takes a constriction length of7: nevertheless computational difficulty in the consistent VD is identical towards that of a VD aimed at an amount -1/2 convolutional code per a control length of 9 owing at great figure of changeovers among trellis .Then in links of power intake ,less-power structures must stay exploited for the VD in a TCM decoder. Error correcting code is a technique for finding errors consecutively and spot-on it grounded on the stable constraints such as bit length etc. This study is so termed as coding theory. Error finding is the modest technique that is examination of digits, solicitations are credit card number faults. It is also named as the block codes

Demodulating digital gesture as of analog signal which is degraded through the noise. Forward Error correction codes Size symbols, bits or fixed size blocks (packets) are executed through Block codes. Real-world block codes can interpret polynomial time in block length. Convolutional codes will build up bit or

Decoding tolerates acute optimum decoding effectiveness by the growing restraint length of the convolutional code

mainly used in the CD players and mobile phones. The sum of the digits given by some number. In theory of coding forward error correction is a technique meant for reducing faults in the data conversation in noisy channels. The main subject is the sender encodes the message evading the retransmission by the error correcting codes. The receiver accepts the encoded message and finds the faults in the message avoiding retransmission. This gives the facility to evade resending the data in the opposed channel in secure band width .This procedure is useful where the circumstances are round to retransmit is extra cost capable and single way communication .The data which is transmitted and deposited in the loading devices to execute the corrupted data. It employs the digital bit stream with a modular carrier and also employed in multicast communications.

Receiver executes FEC technique which is in form of digital bit stream or else demodulation of a digital bit stream with modular carrier .It is used in multicast communications also. It employs Soft-decision algorithm used for

(FEC) are classified in to two types. Perdetermind

stream of random length and remain interpreted by the Viterbi algorithm and extra procedures remain employed .Viterbi

and on account of epidemic growing complication. It can be twisted into a block code, if chosen, by “tail-biting”.

II.METHODS AND MATERIAL

1. Related Work

Viterbi algorithm is simply peculiar specimen of huge procedures which is of curiosity towards plan alike dealing out styles. Hence this one is salient towards

develop practises and gears in what way towards recruit added resemblances keen on algorithm–level. We trust in evocation of altogether 3 styles of

detection of answers on both stages remain a stage nowadays .Still, a portion of labour leftovers must be completed. In height speed less power VD is aimed at TCM structures pre-calculation style which includes T-algorithm competence lessens the power intake of VDs deprived of dropping interpreting speed significantly.

As we observe the per-calculation procedure, wherever the most appropriate pre-calculation stages remain designed and debated .This algorithm stays appropriate design aimed at TCM structures which continuously work on high-degree convolutional codes. To conclude, we offer a plan instance Together the ACSU and SMU remain altered toward properly decode the gesture. ASIC synthesis and power approximation outcomes will display that, compare with full-trellis VD system, pre-computation VD might lower the power intake via 70% by solitary 10% decrease in extreme interpreting rapidity. The principal aim of this study is to relent the improvements acquired by the designers with the application of Viterbi algorithm.

Research mostly focusing on the seriousness of the Viterbi algorithm in the functional applications along with the VHDL code .Research helps the students not only connected to the communication but it also benefits the students in the field of decoders. It is one of the competent techniques aimed at decreasing the mistakes though the communication technique is in progress .In order to put the Viterbi algorithm in an exact way VHDL code is used. At a distance from several codes, researcher nominated VHDL code for this research as it plans high capability in planning the electronic systems. Students, business people and one can effortlessly appreciate and study the Viterbi algorithm ideas and can attain extra information on the VHDL code and also tools which are used in this research. Great-speed Little-power model of a Viterbi Decoder aimed at trellis code modulation(TCM) structures which is offered now in paper .It is fine documented that the Viterbi decoder (VD) is the presiding module defining the total power utilisation of (TCM) systems is implemented in this paper .It is enough to know that the Viterbi decoder (VD) is the main module defining the total power utilisation of TCM decoders .We recommend a pre-calculation structural design included by procedure for VD which can successfully lessen the power utilisation deprived of mortifying the decoding rapidity. The universal answers to originate the best pre-calculation stages are included in this paper. Operation outcome of a VD aimed at degree -3/4 convolutional code engaged in a TCM structure displays that compare using filled trellis VD, pre-calculation style lessens the power utilisation .We need to reveal our principal investigation marks on Viterbi Decoder design aimed at IOT presentation .They made-up a 802.11ah simulator, route the simulation and estimated the performance of a structure in connection with the Viterbi decoder's parameter for example trace-back length L, input data bit-width D and LLR shortened assessment. Simulation effects shows that together BER & PER demonstrations are upgraded condition L assessment improved. Though, L is made more it is sufficient the performance up gradation becomes inconsequential. Choosing the L in series beginning 20 to 40 is our counsel. In count, they must show the condition D assessment rises as of 1 bit to 4 bits, together BER, PER Performances remain enhanced. Specifically when D rises from 2 to 3, they mention to take D =3 meant for hardware expansion. As a final point, they display taking D=3 bits, we must shorten LLR assessment near E=1.75. By doing this we can attain top BER and PER presentation not there some hardware adjustment. This paper offers the architecture and application of effective design aimed at 3GPP-LET .Turbo decoder mostly contains soft-input soft –output (SISO) decoder for attaining great output inter leaver also deinter leaver. Turbo decoder involves Branch Metric Unit (BMU), State Metric Unit (SMU) Log-Likelihood Ratio Computation Unit (LLR), Add Compare select unit(ALU) .Result obtained for Turbo decoder based on the speediness of ACS (Add compare select) unit comprises carry-look ahead adder, Digital comparator and Muxer will rises output and decreases zone structure. In broadcasting of data, turbo coding supports to attain

nearby Shannon limit. TC is a progressive error fixing method extensively employed in communication industry. Turbo encoder & decoder are the main wedges in present communication systems to reach finest capable data response through least probable faults recommended turbo decoder built on soft output Viterbi Algorithm (SOVA). MATLAB is used simulate to small bit fault degree in Turbo Decoder. Whole design of Turbo decoder is implied by Verilog HDL and also synthesized by Xilinx EDA through Spartan 3E. An area effective and in height speed design hard decision Viterbi decoder by means of encrypting speed of 1 /2and control length of k=3 is submitted. This paper presents structure which is applied in the satellite communication. Recommended Viterbi decoder is executed in field programmable gate array (FPGA) moreover application specific integrated circuit (ASIC) by UMC 0.18 µm technology

Wherever extreme operating frequency is 423.566MHz in FPGA also 427 MHz in ASIC and suggested design profits less area together with high speed.

III.PROPOSED WORK

In this work we have suggested to design an efficient VHDL execution of a Viterbi decoder using the idea of pipelining to decrease the critical path (maximum combinational path delay), thereby enhancing the operating frequency of the design and upgrading the throughput.

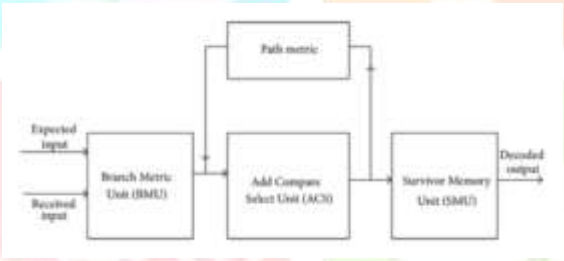

Figure1.Block diagram of Viterbi Decoder

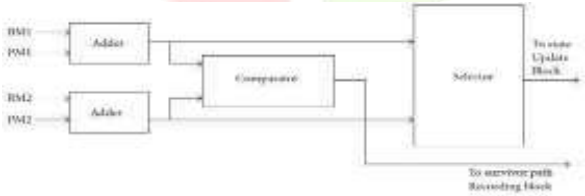

Figure2.Architecture of ACS

Pipelining a design is achieved by adding pipeline registers to combinational paths in order to lower the critical path delay .In the design above, the non-pipelined design has a critical path delay of 4ns .When pipeline registers are added to the combinational paths, the critical path delay is decreases from 4ns to 2ns .This allows the pipelined design to run twice as fast as non-pipelined design, thus improved performance by a factor of 2. However, the faster clock results in higher power dissipation. While critical path reductions are the outcome of pipelining there is an increase in latency as pipeline depth increases. In the example above, the pipeline depth is 1, so a latency of 1 clock is introduced at output S.

IV.RESULT AND DISCUSSION

Pipeline a design is achieved by adding pipeline registers to combinational paths in order to decrease the critical path delay. In the design above, non-pipelining design has a critical path delay is reduced from 2ns to1ns.This allows the pipelined design to run twice as fast as the non-pipelined design therefore it improves the performance by a factor of 2. However, the faster clock will result in higher power dissipation. While critical path reduction is the outcome of pipelining, there is an increase in latency as pipeline depth increases. In the example above, the pipeline depth is 1, so a latency of 1clock cycle is introduced at output. Another drawback of pipelines can cause an increase in area by up to 20 %. The non-pipelined Viterbi decoder has an area utilization of above 21% whereas the pipelined Viterbi decoder has an area utilization of above 35%.

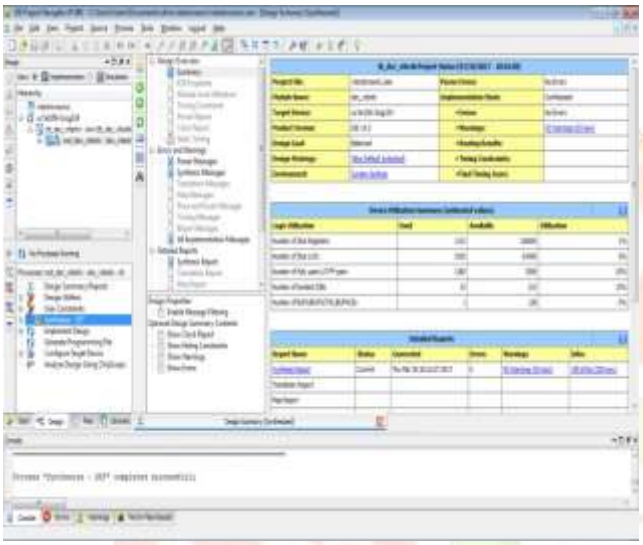

Figure 3. No pipelined design area report

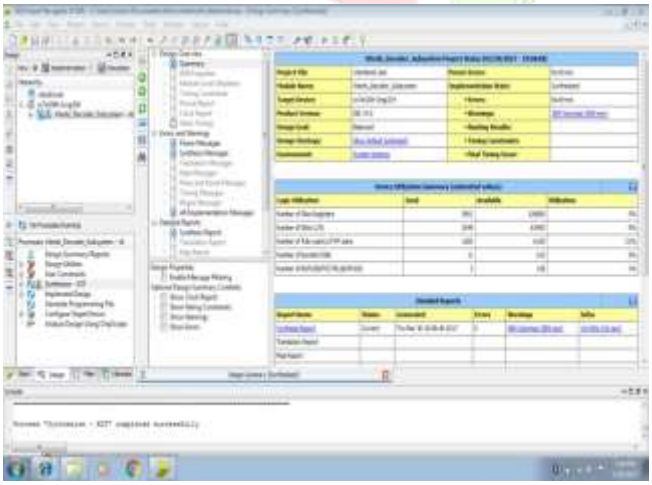

Figure 4. Pipelined design area report

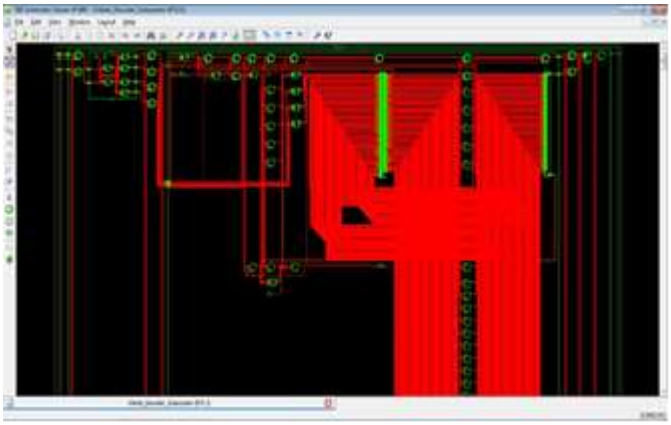

Figure 5. Nonpipelined design RTL view

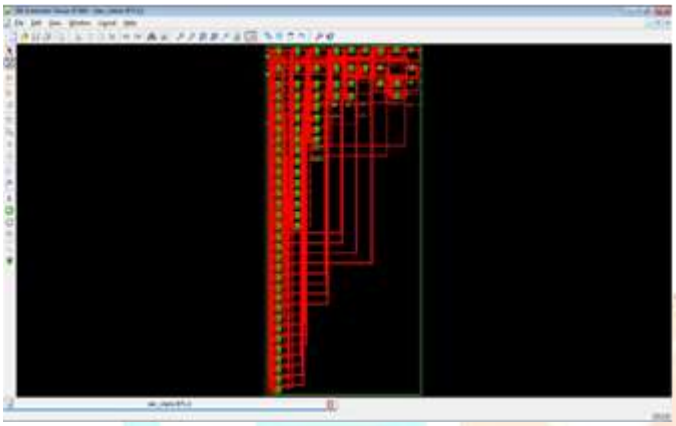

Figure 6. Pipelined design RTL view

V.CONCLUSION

We have been able to design an efficient VHDL operation of a Viterbi decoder using the idea of pipelining in order to reduce the critical path (maximum combinational path delay), thereby improving the operating frequency of the design and enhancing the throughput of a design.

VI.REFERENCES

[1] A.Viterbi "Convolutional codes and their performance in communication systems," IEEE Trans. Common. Technology., vol. COM-19, pp.751–772, Oct. 1971.

[2]J.A. Heller, and I. W. Jacobs, "Viterbi decoding for satellite and space communications," IEEE Trans.Commun. Technol., vol. COM19, pp. 835-848, Oct. 1971.

[3] Manzoor R, Rafique A, Bajwa K.B."VLSI Implementation of an Efficient Pre-Trace Back Approach for Viterbi Algorithm"2007:27- 30.

[4] A.Viterbi,"Convolutional codes and their performance in communication systems" IEEE Trans Communications. Technology.,Vol. COM-19, pp.751–772, Oct. 1971.

[5] P. Singh, S.Vishvakarma"RTL level implementation of high speed- low power Viterbi encoder and decoder" Proc. IEEE ICIST 2013 pp 345-347, March 2013.

[6] M.Veshala, T. Padmaja, K. Ghanta"FPGA based design and implementation of modified Viterbi decoder for a Wi-Fi receiver" Proc. IEEE ICT 2013, pp. 525-529, April 2013.

[7] Kelvin Yi- Tse Lai, "An efficient metric normalization architecture for high-speed low power Viterbi decoder" Proc. IEEE TENCON 2007.

[8]S. Simmons, "Breadth-first trellis decoding with adaptive effort," IEEE Trans. on Common. vol. 38, pp. 3–12, Jan. 1990.

[9] H-D Lin, "Architectures for Viterbi Decoding and ML Estimators for Controllable Markov Sources," Master's thesis, University of California at Berkeley, May. 1988.

[10] G. Ungerboeck, "Adaptive maximum likelihood receiver for carrier modulated data-transmission systems," IEEE Trans. Communications, Vol. 22, no. 5, pp. 626-636, May. 1974.