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ENERGY EFFICIENT MULTIPLICATION USING DVS MULTIPRECISION AND OPERAND SCHEDULING

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Abstract

Multiplication is the basic arithmetic operation. In DSP **(digital signal processing)** a lot of arithmetic operations require the use of multiplications. The performance of 3D computer graphics, gaming, Embedded systems, DSP etc, are particularly depends on the performance of multiplication steps. Multipliers have more area, long latency and consume high amount of power. Critical factors in the design of multipliers are chip area and speed of multiplication and require less hardware. Scaling of technology node increases power-density more than expected. This paper is focused on Multi Precision (MP) reconfigurable multiplier combined with various precision methods, parallel processing (PP), razor-based dynamic voltage scaling (DVS), and MP operands scheduling to give optimum level of performance for various operating conditions. Adapting to the run-time workload of the targeted application, razor flip-flops combine with a dithering voltage unit, because of this the multiplier is able to achieve the lowest power consumption. Use of single switch dithering voltage unit and razor flip-flops help to minimize the safety margins in voltage and overhead in DVS. The more amount of silicon area and power requirements are reduced because of reconfigurable structures. In this paper we design the multiplier in three ways and compare their performance. We can obtain the efficiency and also achieve silicon area reduction in the range of 11.1% by using AIMS 0.35 technology. Using ModelSim6.3 software we can design the multiplier structure and Xilinx synthesis Tool is used for power and area analysis.

Index Terms:

Multiplier, Razor Flip Flops, Operand Scheduler, Multiplicand, Multi precision, Dynamic Voltage Scaling, Dithering technique

1. Introduction

Today, 'energy crises' is the main problem faced by the worldwide technologies. So, the main aim is reduction in power consumption of circuit to avoid the energy crises problem. Increasing demand of technology required the processors have great challenge to handle the complex processes, assembling million number of processor cores on the single IC. Because of this IC fabrication, main processor combines with co-processor to perform some operations like addition, subtraction, multiplication, division, etc, as well as doing signal processing operations, Computer Graphics, Gaming etc.

Recent Development in VLSI Design can obtain require amount of reduction in Multiplier's power consumption. Because of portability, power dissipation is the main constrain. The mobile device consumer demands more features and extended battery life at a lower cost. Consumers demand for increase in portability, yet high performance multimedia and communication products imposes stringent constraints on the power consumption of individual internal components. Of these, multipliers perform one of the most frequent arithmetic This spurious switching activity can be mitigated by balancing internal paths through combination of architectural and transistor-level optimization techniques. In addition to internal path delays, dynamic power reduction can also be achieved by monitoring the effective dynamic range of the input operands .so as to disable unused sections of the multiplier truncate the output product at the cost of reduced precision. This is possible because, in most sensor applications, the actual inputs do not always occupy the entire magnitude of its word-length.

Multipliers perform one of the most frequently encountered arithmetic operations in digital signal processors (DSPs). For embedded applications, it has become essential to design more power-aware multipliers. The power aware multipliers uses new technology called Multi precision which include some characteristics (i) non negligible silicon and power overhead, (ii)Performance and throughput reduction brought by the shut-down of parts of the circuit and/or use of reduced supply voltage and(iii) restriction and great margins to the operating condition versatility of the multiplier.

Normally multiplication process has implemented variants of the basic "**Shift Addition**" method in FPGA. Some of the preeminent methods of multiplier implementation in the FPGA

paradigm are "**Size Reduction in Accumulator, Ripple Carry Adder, Carry Save Adder, LUT&PP, Computed Partial Product, and Wallace Trees",** above mentioned multiplier implementations, the Wallace tree multipliers are highly used in VLSI implementation, because it reduce the depth of the adder chain and also minimize the time complexity. The most efficient multiplier structure will vary depending on the throughput requirement of the application. The 1st step of the design process is the selection of the required circuit structure for Multiplication operation. There are various structures to perform the multiplication operation starting from the simple serial multipliers to the complex parallel multipliers, any speed improvement in the multiplier will improve the operating frequency of the digital signal processors or can be traded for energy by optimizing circuit sizes and the voltage supply. This paper addresses high-level optimization techniques for multiplication and uses "**Booth and Wallace Tree Multiplier"** multipliers. In this paper for the power reduction requirement we combine the following processes like Dynamic voltage scaling (DVS) with Multi Precision (MP) & Operand Scheduling technique.

2. EXISTING SYSTEM

Today's full-custom DSPs and application-specific integrated circuits (ASICs) are designed for a fixed maximum word-length so as to accommodate the worst case scenario. Therefore, an 8-bit multiplication computed on a 32-bit Booth multiplier would result in unnecessary switching activity and power loss. Various works .are implemented for word length optimization, pair of input are routed for to the smallest multiplier that can compute the result to take advantage of the lower energy consumption of the smaller circuit.

Share and reuse the structure concept was used, 8-bit multiplier is reused for the 16-bit multiplication, adding scalability without large area penalty. Extended this method by implementing pipelining to further improve the multiplier's performance. A more flexible approach with several multiplier elements grouped together to provide higher precisions and reconfigurability. Reference analyzed the overhead associated to such reconfigurable multipliers. This analysis showed that around 10%–20% of extra chip area is needed for 8–16 bits multipliers. Combining multi precision (MP) with dynamic voltage scaling (DVS) can provide a dramatic reduction in power consumption by adjusting the supply voltage according to circuit's run-time workload rather than fixing it to cater for the worst case scenario [4]. When adjusting the voltage, the actual performance of the multiplier running under scaled voltage has to be characterized to guarantee a fail-safe operation.

2. Multiplier Structure and Operation

Multiplication structure consists of 5 basic blocks to their operations.

1) MP multiplier.

2) Input Operands Scheduler (IOS) → Used to reorder the input data into a buffer, to reduce the required power supply voltage transitions,

3) Frequency Scaling Unit (FSU) implemented using a **Voltage Controlled Oscillator (VCO) → used to** generate the required operating frequency of the multiplier;

4) Voltage Scaling Unit (VSU) implemented using a voltage dithering technique →Used to limit silicon area overhead. Its function is to dynamically generate the supply voltage so as to minimize power consumption.

5) Dynamic Voltage/Frequency Management Unit (VFMU) → receives the user requirements (e.g., throughput). VFMU sends control signals to the VSU and FSU

To generate the required power supply voltage and clock frequency for the MP multiplier.

Initially, the multiplier operates at a standard supply voltage of 3.3 V. If the razor flip flops of the multiplier do not report any errors, this means that the supply voltage can be reduced. This is achieved through the VFMU, which sends control signals to the VSU, hence to lower the supply voltage level. When the feedback provided by the razor flip-flops indicates timing errors, the scaling of the power supply is stopped. Proposed Multiplier not only combined Multi Precision & Parallel Processing, and also combines DVS with operand scheduling technique. PP can be used to increase the throughput or reduce the supply voltage level for low power operation. Our multiplier comprises 8 × 8 bit reconfigurable multipliers. These building blocks can either work as nine independent multipliers or work in parallel to perform one, two or three 16 × 16 bit multiplications or a single-32 × 32 bit operation. Booth radix-4Wallace tree structure similar to that used in designing the building blocks of our MP multipliers. However, because of its larger size, the 32 × 32 bit fixed width multiplier exhibits an irregular layout with complex interconnects. This limitation of tree multipliers happens to be addressed by our MP 32 × 32 bit multiplier, which uses a more regular design to partition, regroup, and sum partial products.

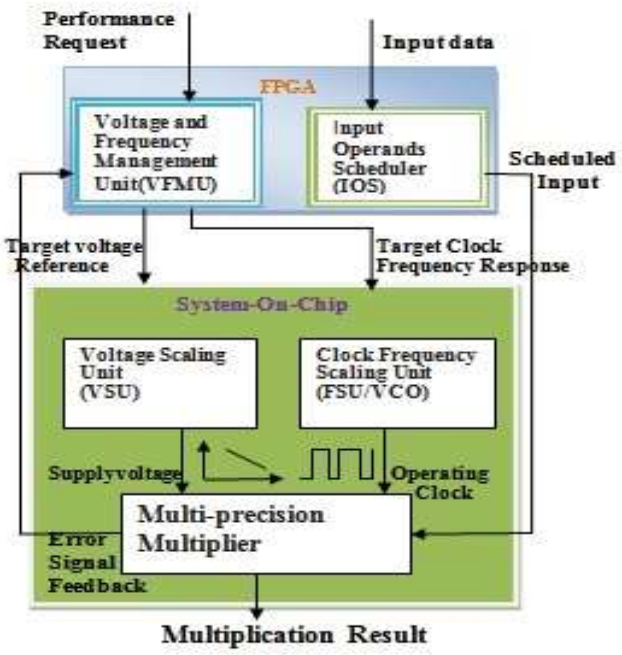

Fig 1: Overall multiplier system architecture.

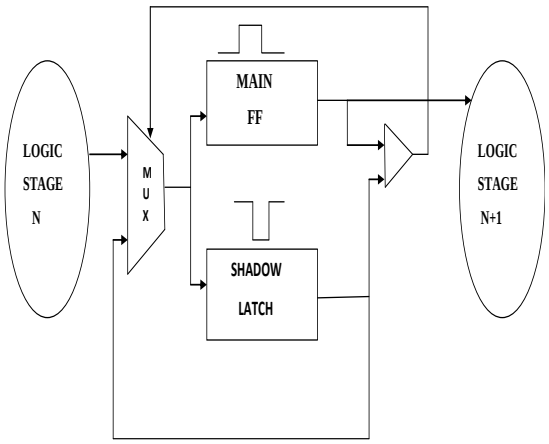

Fig. 2 Conceptual view of razor flip-flop.

A dynamic power supply and a VCO are employed to achieve real-time dynamic voltage and frequency scaling under various operating conditions, near-optimal dynamic voltage scaling can be achieved when using voltage dithering, which exhibits faster response time than conventional voltage regulators. Voltage dithering uses power switches to connect different supply voltages to the load, depending on the time slots. The razor technology is a breakthrough work, which largely eliminates the safety margins by achieving variable tolerance through in-situ timing error detection and correction ability. This approach is based on a razor flip-flop, which detects and corrects delay errors by double sampling. The razor flip-flop operates as a standard positive edge triggered flip-flops coupled with a shadow latch, which samples at the negative edge. Therefore, the input data is given in the duration of the positive clock phase to settle down to its correct state before being by the shadow latch. The minimum allowable supply voltage needs to be set, hence the shadow latch always clocks the correct data even for the worst case conditions. This requirement is usually satisfied given that the shadow latch is clocked later than the main flip-flop.

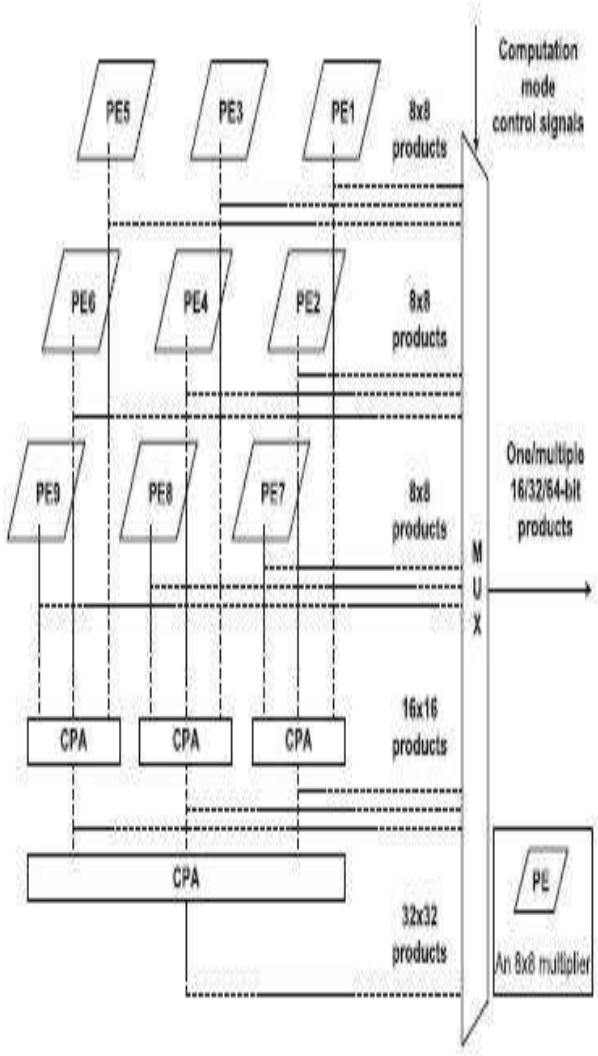

Fig 3: Possible configuration modes of proposed MP multiplier

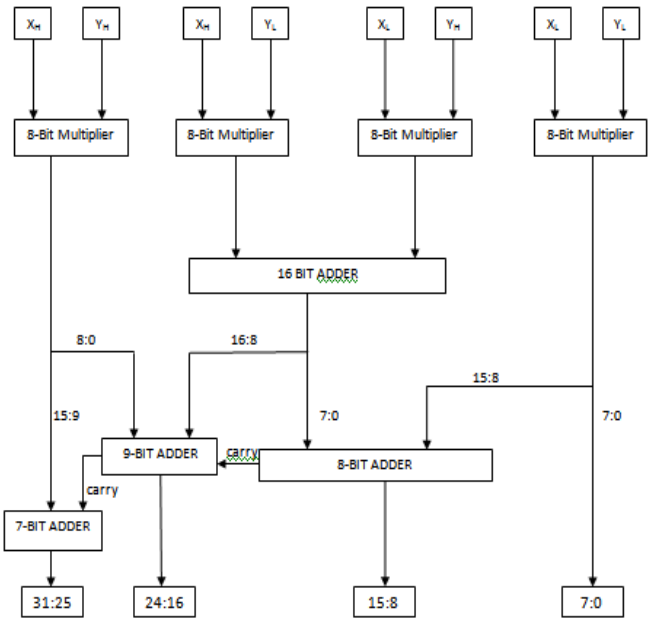

Fig.4: 4 – Sub block Multiplier structure (Fixed Width)

3. SIMULATION RESULTS

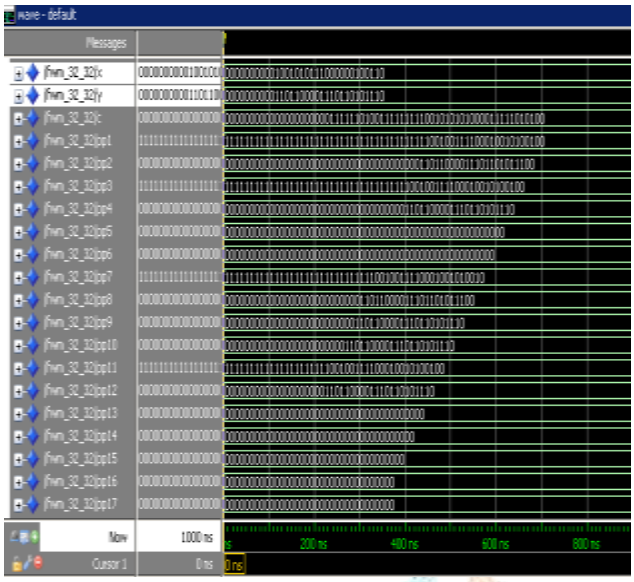

Fig 5. Simulation result of Fixed Width Multiplier.

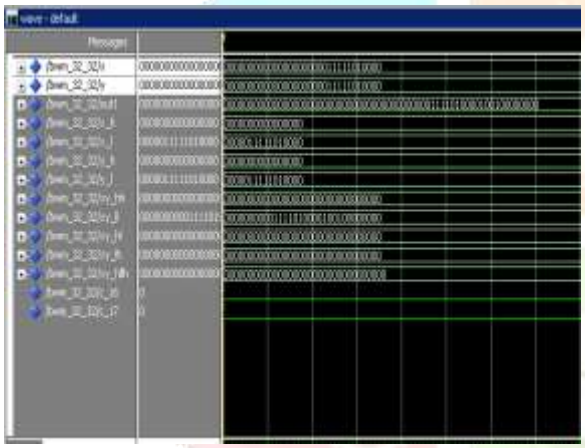

Fig 6. Simulation result for 4 sub block Multiplier.

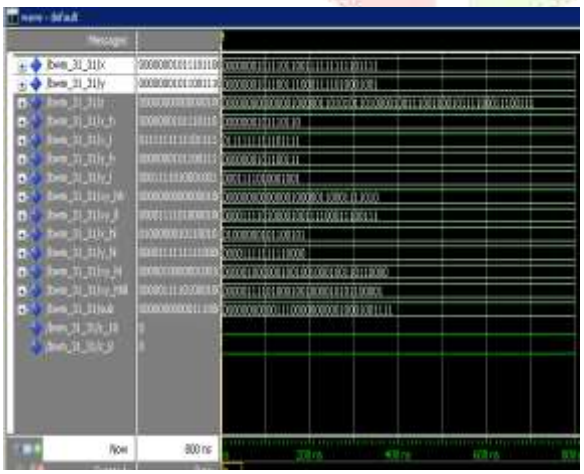

Fig6.Simulation Result for 3 Sub block Multiplier

5. PROPOSED SYSTEM

Only required amount of Bits could be used, remaining bits can be kept in OFF condition. This will lead to achieve optimum level power consumption during multiplication process.

5. FUTURE WORK

Using 3 Sub block multiplier structure, adder Positions could be changed for delay reduction. And using 4: 2 compressor techniques for Power consumption also efficiency can be increased. And this multiplier bit is used on a FIR FILTER.

6. CONCLUSION

Proposed a novel MP multiplier architecture featuring, respectively, 28.2% and 15.8% reduction in silicon area and power consumption compared with its 32 × 32 bit conventional fixed-width multiplier counterpart. When integrating this MP multiplier architecture with an error-tolerant razor-based DVS approach and the proposed novel operands scheduler, 77.7%–86.3% total power reduction was achieved with a total silicon area overhead as low as 11.1%.

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