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Crosstalk Avoidance with Low Power and Low Area in ASIC Applications

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***Abstract*---Cross talk is a common issue in ASIC design for technologies lesser than 180nm. It is more complicated in larger designs like System on Chip and Network on chip. Crosstalk noise effects the timing performance and degrades the signal which is passing from one module to another module in a chip. Generally ASIC implementations use special crosstalk removal circuits which consume more power and more area. In order to avoid crosstalk and delay we have used "Bus Encoding Method". Bus Encoding Method aims to reduce the overall activity factor and there by reduces the consumption in system. This method avoids the crosstalk by low power and low area. We designed 18T Full adder circuit as testing sequence for crosstalk analysis. crosstalk avoidance can be achieved by low area and low power.**

Keywords---Crosstalk noise; 18T full adder; Bus encoding; Crosstalk avoidance; 180nm technology; Low power dissipation;

I. INTRODUCTION

In digital circuits, noise has become a serious problem to scale back the performance of the whole system. to take care of the area, power and delay, there are four basic principles are needed like to form clock tares fast, scaling the edge voltage, improve the interconnect densities and high performance circuit. With the assistance of interconnect densities, the coupling capacitance are often improved also as by using faster clock rates, on-chip slew time are often increased [1]. Normally, crosstalk may be a sort of noise which is introduced by unwanted coupling between two neighbouring wires [2]. Coupling effect increase the crosstalk delay and reduce the signal integrity. we'd like to model interconnects, which holds the general information of physical characteristics just like the distance between the nets or overlap. thanks to the facility consumption and changing the logical level the noise causes delay and therefore the overall system may be a failure. to attenuate the consequences of Nano scale some methods are used like buffer insertion, wire spacing, driver sizing, buzzer sizing. during this method, buffer sizing and driver sizing methods are so difficult to use post rout stage [3].

Coupling noise is additionally called as cross talk noise, which affects within the digital VLSI circuits. While changing the days , the cross talk can affect the signal delays [4]. thanks to this crosstalk noise, VLSI circuits are a failure and generate the delay effects. When the signal is highly random, it is not possible to provide a deterministic delay fault metric. Most of the method have been obtained [5], [6], but none of them take care about the crosstalk effects in their analysis [7]. Author Chen introduced a generating test algorithm to reduce the crosstalk delay. The algorithm mainly concentrates on the coupled capacitive nodes and test pattern generation to activate worst coupling case. Even this algorithm is also affected in the critical path due to the crosstalk noise. Because of this problem, the delay also strongly coupled to the circuits to degrade the performance [8]. In our proposed method bus encoding method is introduced to resolve this problem. This method includes the decoding process, which getting the input from encoder output. Finally, the area, power and crosstalk noise of the entire circuits will be minimized in our proposed method than the conventional methods.

II. RELATED WORK

Giampierolovat et al. [9] has introduced intraband conductivity sensors with grapheme capacitance. In this paper, the conductivity sensor elements have been derived from the Boltzmann equation under the relaxation time. This equation derived for current density on grapheme Nano ribbons (GNR). But this equation only valid for low wave numbers only. The output waveform is degraded due to thresholding problem and the weakness of the GNR. Then, it is discretion and it produces weakly non- local effects model in GNR.

Kedarkarmarkar et al. [10] has implemented code word generation with crosstalk couplings. In this paper, bus encoding technique has been proposed to improve the performance. This coding technique is very easy to scalable and automotive. By using basic blocks such as multipliers and adders, the code word has been calculated. This result compare area and power. But this model not considered about the delay.

Qijun Lu et al. [11] has proposed a single walled carbon Nanotube (SWCNT) interconnects. In this paper, with the help of SWCNT, the bundle interconnection was evaluated to reduce the crosstalk delay. This method can reduce the crosstalk delay but not efficient in more number of execution situation. In that situation, the delay can be exceeded. Feng shi et al. [12] has introduced cross talk avoidance codes (CAC) based on novel pattern classifications. In this paper, they classified new classification pattern with new family CACs. In this method have some drawbacks like these models have some limited accuracy and the signal is overlapped. So, we can't get proper crosstalk rectifying a signal in output.

LiboQian et al. [13] has introduced propagation characteristics of coupled MLGNR interconnects. In this paper, based on equivalent single conductor (ESC), extracted some parameters like: equivalent resistance, inductance and capacitance. It is not possible to reduce the delay noise with high intensity.

III. PROPOSED METHODOLOGY

Fig 1. shows the circuit used for analysing cross talk. The circuit has two outputs that are carrying and sum. Both outputs of the circuit are degraded because of the crosstalk effect. Total circuit is implemented by using pass transistor logic. The above circuit has 3 main logic components, they are XNOR, MUX, and inverter based buffer. Mainly, cross talk of the circuit is directly proportional to the number of nodes which are connected near to each other. In the above given circuit, the cross talk is mainly created due to the inverter buffer. In this circuit, the buffer circuit is used to maintain the constant voltage level for logic 0 and 1. In this project, we are using cadence tools to analyse the cross talk of the entire circuit.

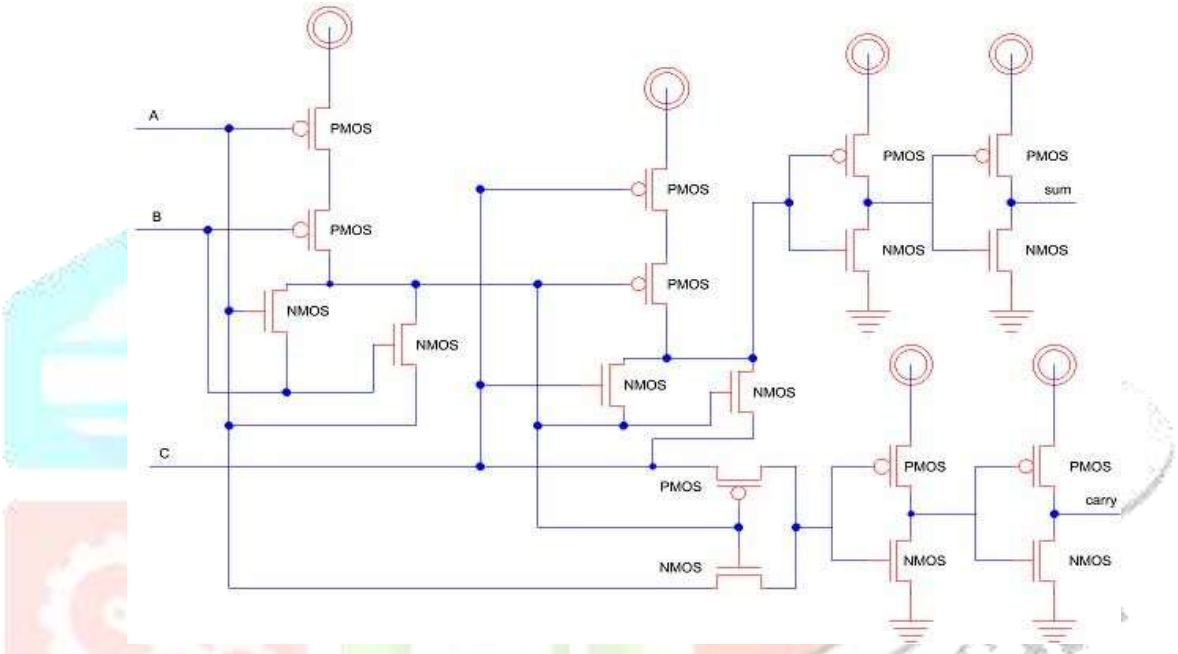

Fig. 1. 18T FA Circuit Used for Data Generation

A. Overview of crosstalk estimation

In practical circuits, many interconnects couple with various interconnects, i.e. with various aggressors. We assess the pinnacle noise voltage brought about by every aggressor individually, and find out the greatest noise voltage at the sink by superposition. The victim net with one aggressor is mentioned as two partially coupled interconnects (Fig. 2).

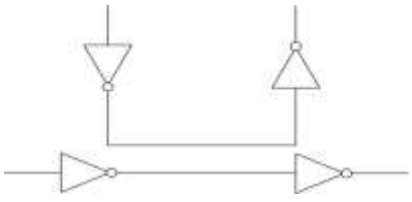

Fig. 2. Two Coupled Interconnects

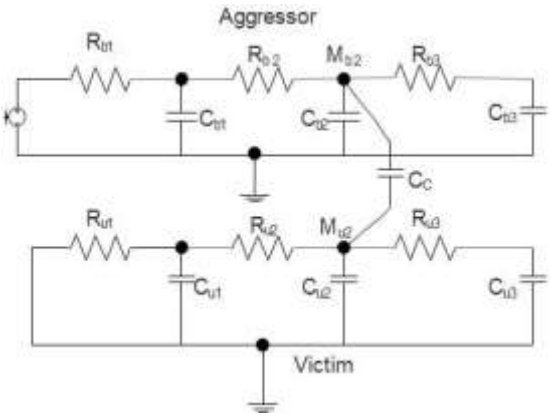

Fig. 3. Two Partially-Coupled Interconnects for Crosstalk Estimation

The incompletely coupled interconnects in Fig. 2 are displayed as a proportional circuit appeared in Fig. 3. Ru1 is the powerful driver resistance of the victim net. The hub Mu2 relates to the centre purpose of the coupling interconnects. Ru2 is the resistance between the source and Mu2, and Ru3 is the resistance amongst Mu2 and the sink. Cc is the coupling capacitance between the victim and the aggressor. The capacitances Cu1, Cu2 what's more, Cu3 are spoken to as C1/2, (C1 + C2)/2, and C2/2 + Cl separately, where C1 is the wire capacitance from the source to Mu2, C2 is the wire capacitance from Mu2 to the sink, and Cl is the capacitance of the beneficiary. The parameters of the assailant wire, Rb1, Rb2, Rb3, Cb1, Cb2, Cb3, are resolved likewise. The additionally builds up a strategy that can apply interconnects with branches into the model circuit of Fig. 3.

From fig.3, the peak voltage V Peak is expressed as,

V Peak = (Ru1 + Ru2) Cc Vdd / Tu * (Tu/Tb) –Tb/Tu- Tb Where, Tu and Tb is mentioned as total victim, and total aggressor voltage.

Tu = Ru1 (Cu1 + Cu2 + Cc + Cu3) + Ru2 (Cu2 + Cc + Cu3) + Ru3*Cu3 Tb = Ra1 (Cb1 + Cb2 + Cc + Cb3eff) + Ru2 (Cb2 + Cc + Cb3eff)

Here, Cb3eff = Ca3 (1- e-T/Rb3*Cb3) where, T = Ra1 (Cb1 + Cb2 + Cc + Cb3) + Ru2 (Cb2 + Cc + Cb3)

IV. ENCODING METHOD

Fig.4 shows the block diagram of the proposed encoder which involves countering, controller, comparator, and three 3- bit registers. In the advanced sector, each compound of the encoding method is described. By reducing the 7-bit lines into 4-bit lines the worst-case crosstalk is reduced or eliminated by the encoder which transforms the bus line signals. It identifies the number of 1's which are equal or greater than 4 in counter and controller compound. According to the higher number of 1's in the output line of the controller is placed to locate the flips in the line. First, the counter counts the number of 1's. If the number of 1's is equal or greater than 4 then the output of the comparator is a high state, which is denoted as 1. Due to the counter and controller, there are 3 flips possible in the comparator. In three registers, the flips positions are stored.

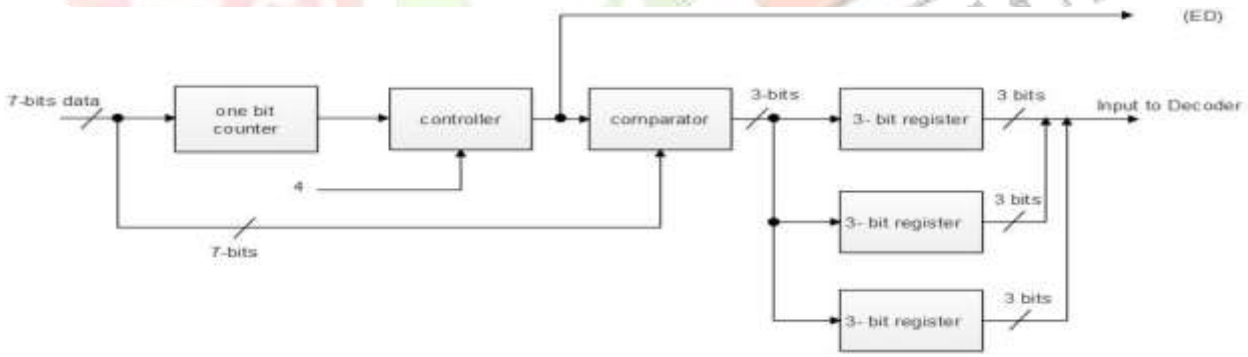

Fig. 4. Block diagram of encoding model

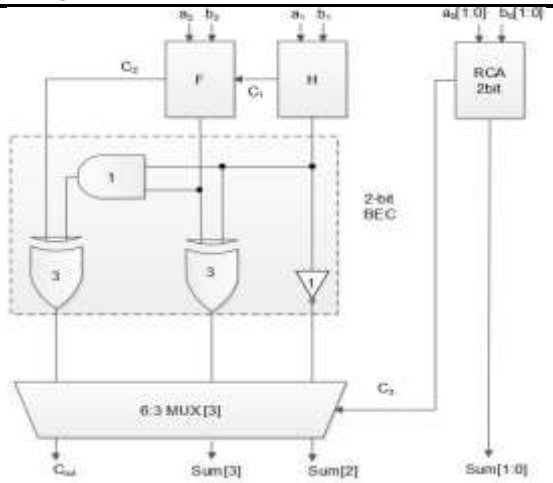

Fig. 5. Low area carry selectadder

The output of the comparator is EX-OR with the initial 7- bit input line and stored from the flipped position in the 3-bit register. The best as well as worst cases the number of the register is chosen as three. The crosstalk is reduced if all the register having the value as null or the value of the register can vary from zero to maximum 3. The encoder takes the input as 7-bit data lines from that 3-bit are taken to indicate the flip bit position. Table.1 shows the 8 combinations for all the equivalent position. By three different clock cycles, each register value is sent. The decoder the content of one register is sent for each clock cycle. In the next clock cycle, the next register contents are sent and so on.

TABLE I. REGISTER VALUES INDICATING THE POSITIONS OF FLIPPING

Register value	Flipped I/P line position
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

A. Counter

The input of the counter is 7-bit input. The number of 1's is determined in the input sequence of 7-bit lines. The number of 1's is fed as input to the controller. The counter has adder, this normal adder is replaced by low area carry select adder for reduction of the area and is shown in the fig.5.

B. Controller

The output line of the counter means the number of 1's as shown in fig 4. From the input of the controller, the output of the counter is fed. From the controller, a decision is used which is the number of 1's is greater than or equal to 4. If the number of 1's is equal to or greater than 4 then the output of the controller is high state i.e.1. If the number of 1's is less than 4 then the output of the controller is low state i.e.0.

C. Comparator

The comparator the single output line is fed along with the initial 7-bit input. Each of the initial 7-bit is compared with the single output line. The single line it is compared whether the value of the bit is same or different. To identify the flipping the output of the controller is EX-OR with the seven input lines. For decoding purpose, it identifies the flipped position and stored in the 3-bit register.

D. Register

The position of flipped bit which is identified by the comparator is used to store in the register. It finds the proper clarification of the input bits as showed in table 1. Where the 0th bit position in the register has 000 value, 001 has 1st bit position and likewise, 111 has 5th bit position. For the storage of the flipped bit position, the three registers are used simultaneously. Along with three register output, the controller output line also transmitted, which is denoted as equivalent line. For the decoding purpose, the encoder provides four output lines i.e. one of the controllers and the other three from the register. In complete decoding of the input sequence, it needs three clock cycles.

E. Crosstalk analytical

The equivalent circuit model of pseudo- 2π RC model is shown in fig.6. This model is used to model the structure, which is different from a standard 2π RC model by shifting the coupling capacitances at the receiver ends to the middle nodes. To understand the coupling noise, the coupling capacitance at the receiver ends are shorted to ground. The encoder output is connected to this circuit, which creates the noise from the incoming signal. Then this RC model output is fed to the decoder, which helps to remove the crosstalk noise.

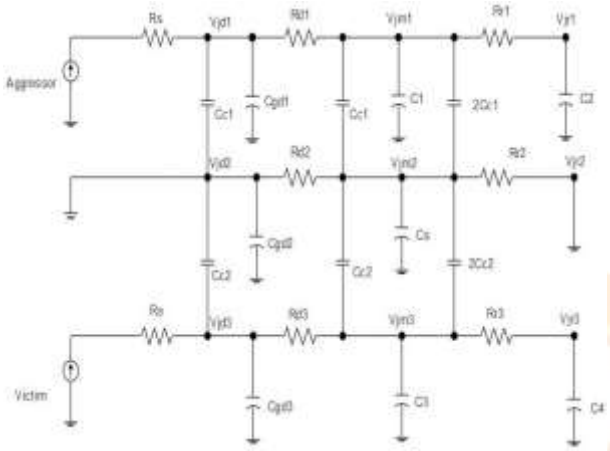

Fig. 6. Equivalent circuit model of pseudo- 2π RC model

V. DECODER TECHNIQUE

Fig.7 shows the proposed encoding method of the decoder. It consists of three 3-bit registers, inversion module, and line identifier. The four output lines from the encoder are given as a input to the decoder. In the first register of the decoder, the content of the first register from the encoder is stored for the first clock cycle and so on. There are three maximum flips are possible. So, to complete decoding of the 7-bit data three clock cycles are required. Instead of three 3-bit registers, we can use the single 3-bit register in the encoder and decoder side, for the transmission of flipped bit position to decoder side the delay is generated by the clock cycle.

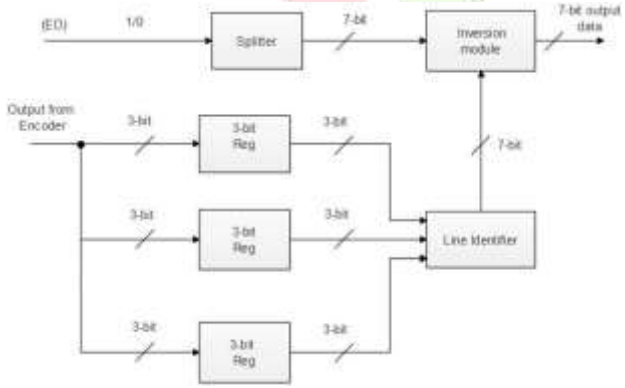

Fig. 7. Block diagram of decoding model

The input is fed from the output of the comparator of encoder side to the splitter module of the decoder. It breaks 1- bit input into 7-bit of output lines. All the output has the same value as the input i.e. if the input is 1 then all the seven output lines has the output as 1. When the input is 0 then all the seven output lines has the output as 0. The input to the identifier is taken from the 3-bit register sequentially. The clock cycle directs the sequence. As per table.1, it gets the content of the 3- bit register and identifies the line to be flipped. The identification indication is fed to the inversion module. The identified line is inverted by the inversion module. The final decoded data of 7-bits is taken as the output of the decoder after three iterations. The overall crosstalk analysis block diagram is shown in fig.8.

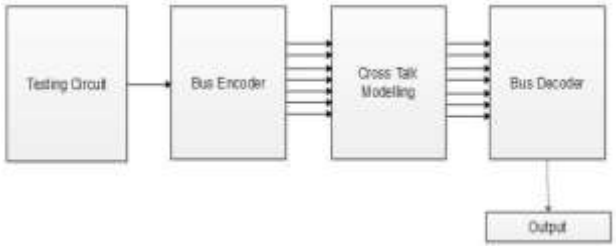

Fig. 8. Crosstalk analysis

VI. EXPERIMENTAL SETUP

The proposed method using 18 transistors to implement area as well as power efficient FA circuit by using Low area carry select adder. The complete method is implemented on cadence 45nm technology and RTL compiler. Bus encoding RTL is compiled in cadence encounter tool. From this area, Power, crosstalk noise, and delay can be minimized effectively.

. VII. RESULT AND DISCUSSION

Fig. 9. Comparison of area performance for existing and proposed encode

Fig. 10. Comparison of power performance for existing and proposed encoderer

From this graph we can understand, those two parameters such as area and power is reduced in proposed method than existing method.

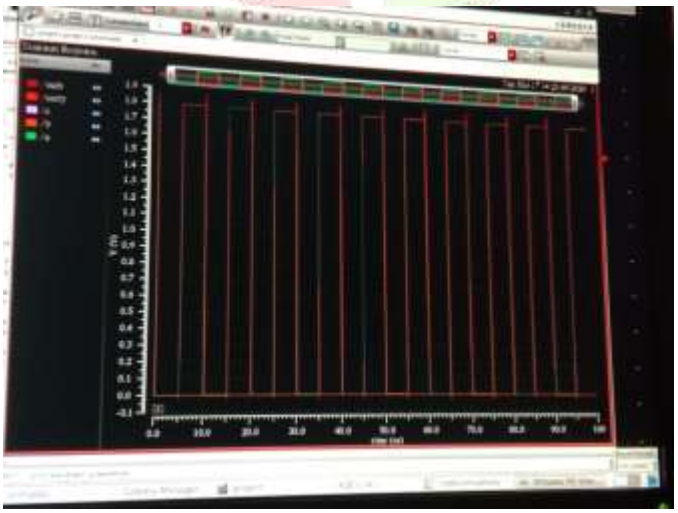

Fig. 11. Testing circuit output

The testing circuit output is shown in fig.11, which is taken from cadence software. From this result, we can understand counter, controller, and comparator of the encoding techniques are working properly.

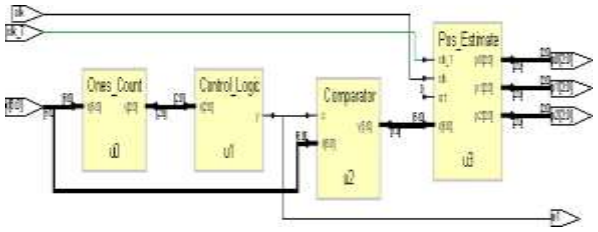

Fig. 12. RTL schematic diagram of encoding process

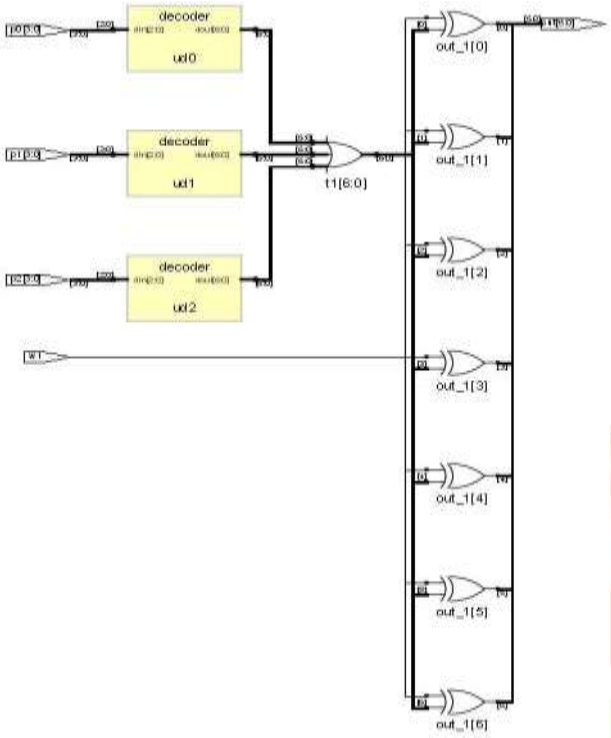

Fig. 13. RTL schematic diagram of decoding process

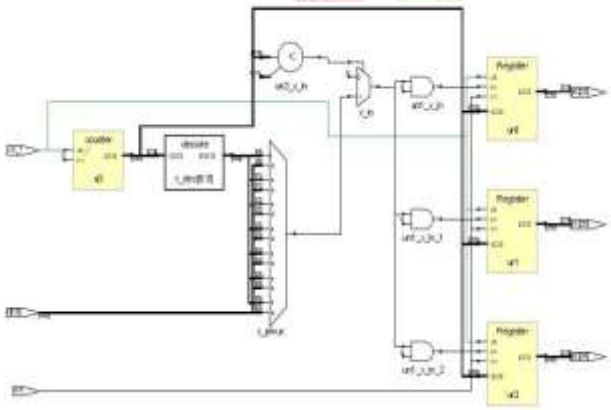

Fig. 14. RTL schematic diagram of the POS estimation

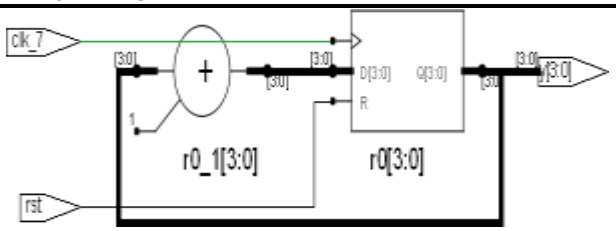

Fig. 15. RTL schematic diagram of the counter

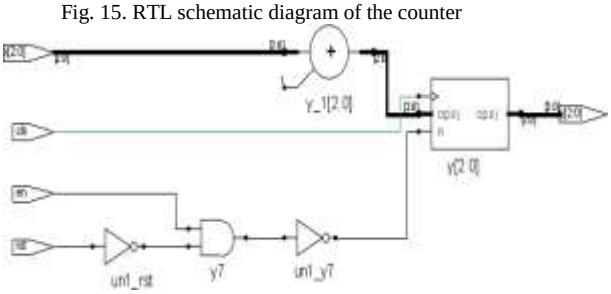

Fig. 16. RTL schematic diagram of the register

The RTL schematic of encoding process, decoding process, POS (Position) estimation, counter and the registers are shown in fig.12, fig.13, fig.14, fig.15, fig.16. This all schematics are obtained from a Synplify pro by using Verilog code. We have a separate code for each block such as encoding process, decoding process, POS estimation, counter and the register.

VII. CONCLUSION

In this paper, the proposed method BEM is eliminating the crosstalk noise, which is present in the 18T full adder circuit as testing sequence. This reduction of crosstalk is because of the reduction of lines from7 bits to 4 bits as an output of the encoder. We have done upto simulation and further we improve our results. Finally, the area, and power are minimized with the help of bus encoding scheme.

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