Comparative Study of Dual Material Asymmetric Double Gate Junctionless and Junction Transistor

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Abstract : In this paper, we present the features of asymmetric DMDG Junctionless transistor and compared it with a similar junction transistor. This comparison has been carried out using 2D models of the transistors. The parameters we have calculated are threshold voltage, drain induced barrier lowering (DIBL), Ion/ Ioff ratio and sub-threshold slope (SS). We observed that when the channel length is lesser, the junctionless transistor has better results for DIBL (34.61% improvement) and Ion/Ioff ratio (by 10^3). The results of SS for both the transistors were the same. These results varied when the channel lengths of the transistors were changed between 20 nm, 30 nm and 40 nm. All the device parameters are simulated in 2D environment using the device simulator Cogenda Visual TCAD.

IndexTerms **- dual material dual gate (DMDG) Junctionless transistor, two-dimensional (2D) model, drain induced barrier lowering (DIBL), sub-threshold slope (SS), Cogenda Visual technology computer aided design (TCAD).**

I. INTRODUCTION

In order to realize high speed and high packaging density in MOS integrated circuits, the dimensions of MOSFET's have shrunk in accordance with Moore's law. However, the power consumption of modern VLSI's is become significant as a result of extremely large integration. Reducing this power is necessary and one of the approaches is to lower down the supply, but this degrades MOSFET's current driving capability. Consequently, scaling of MOS dimensions is important in order to improve the driving ability and achieve higher performance and higher functional VLSI. The conventional Metal Oxide Semiconductor Field Effect Transistors has challenges, such as enlarged gate leakage and added serious short channel effects with continuous miniaturization of device sizes at Nano-scale regime [1]. Multiple gate FETs have better scalability due to the superior controllability of the gates on the channel region. According to International Technology Roadmap for Semiconductors (ITRS), the gate length of MOSFETs is forecasted to reach sub-20 nm regime in a couple of years. As a response to several problems resulted from the scaling gate in Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), junction less transistors have been reported as alternative device. Among all the MOSFETs, junction less MOSFET has recently attracted the attention of the researchers due to its unique electrical properties. The properties include 1) improved electrostatic characteristics such as low leakage current 2) high trans-conductance 3) very low Drain induced barrier lowering and 4) less sensitive to thermal budget issues than regular CMOS devices [3].

Double-Gate(DG)MOSFETs layers seem to be a very promising option for ultimate scaling of CMOS technology. Excellent short-channel effect (SCE) immunity, high transconductance, and ideal subthreshold factor have been reported by many theoretical and experimental studies on this device. Lack of Source & Drain induced depletion regions in the channel of Junctionless devices enlarges the potential barrier and thus reduces short channel effect [3].These properties can further be improved by using dual material gates. Hence to combine all these properties, we have proposed a Dual Material Double Gate asymmetric Junctionless Transistor. We have carried out a simulation study of the same. The characteristics are compared with conventional device that is Dual material gate JT. All the device parameters are simulated in 2-D environment using the device simulator Cogenda Visual TCAD [1].

II. DEVICE STRUCTURE AND SIMULATION

A cross section of the DMGJLT is shown in Fig. 1. The DMGJLT has two asymmetric metal gates with three different work functions denoted by *m*1, *m*2, m3 which are assigned to be 5.1 eV, 4.1 eV and 4.1 eV respectively corresponding to the values of some common metals (e.g., PPolySi for m1 and NPolySi for m2, m3) [4]. The channel length initially is 20 nm for both the devices. The detailed parameters of both DMGJLT and DMDGT used in the simulations are shown in Table 1. The lengths and work functions of the two metal gates can be varied in the simulations.

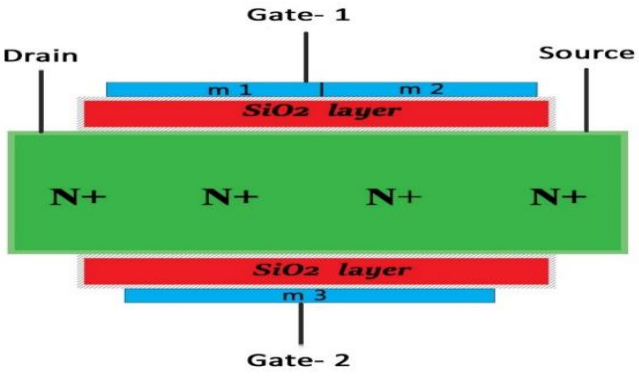

Fig.1 Cross section of DMDGJLT

Table 1 gives the description of the values used for the simulations.All the simulations were done in 2D environment using Cogenda TCAD.

Table 1 Dimensions used for both DMDGJLT DMDGT devices

Parameter	DMDGJLT value	DMDGT value
Channel Length	20 nm	20 nm
Channel Width	1 um	1 um
Channel doping density	0.4 x 10 ^ 17 / cm^3	1 x 10 ^ 16 /cm^3
Source doping density	-	1 x 10 ^ 19 /cm^3
Drain doping density	-	1 x 10 ^ 19 /cm^3
SiO2 layer thickness	1 nm	1 nm
Gate m1 affinity	5.1 eV	5.1 eV
Gate m2 affinity	4.1 eV	4.1 eV
Gate m3 affinity	4.1 eV	4.1 eV

III. RESULTS AND DISCUSSION

The parameters of the DMGJLT are calculated and compared with a corresponding DMDGT. Some of the key parameters are analyzed in this section.

3.1 DIBL

In long channel MOSFET's voltage applied to gate acts as a controller to drain-source current flow as we reduce the channel length, drain current (I_D) is not only controlled by the gate voltage but also controlled by the drain voltage this behaviour of the transistor is called DIBL. This behaviour of the MOSFET where drain acts as a second gate degrades the performance of MOSFET. Thus, the drain current is controlled not only by the gate voltage, but also by the drain voltage. For device modeling purposes this parasitic effect can be accounted for by a threshold voltage reduction depending on the drain voltage. In Fig. 2, the DIBL characteristics of the DMGJLT and the corresponding DMDGT for different channel lengths is shown.

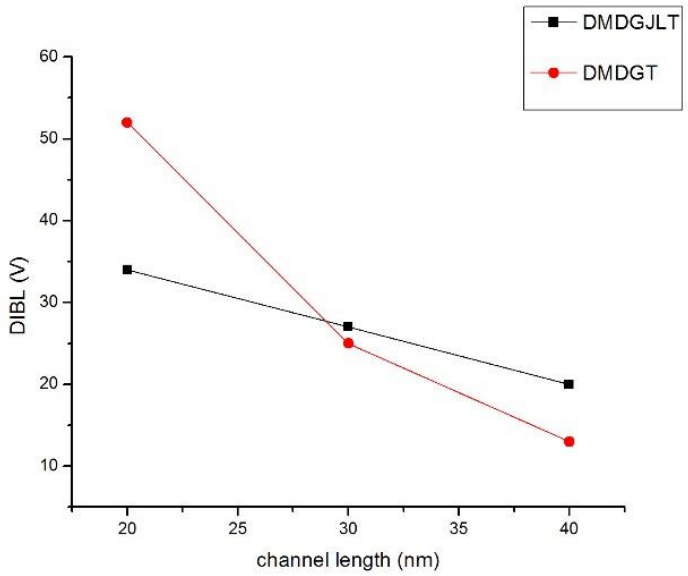

Fig.2 DIBL characteristics for DMDGJLT and DMDGT for 20,30 and 40 nm channel lengths.

The simulation results of the DIBL effect for junctionless and junction transistor are summarized in Table 2. DIBL effect in junctionless transistor is lesser than in junction transistor for a channel length of 20 nm. As channel length increases to 30 nm and 40 nm DIBL effect is lesser in the junction transistor.

Table 2 DIBL Readings

Type	Channel Length (nm)	Vth for Vds = 1 V (V)	Vth for Vds = 0.5 V (V)	DIBL (V)
DMDGJLT	20	0.091	0.125	0.034
	30	0.171	0.198	0.027
	40	0.17	0.19	0.02
DMDGT	20	-0.307	-0.255	0.052
	30	-0.113	-0.088	0.025
	40	-0.019	-0.006	0.013

3.2 Ion/I off Ratio

By using different materials in the gate, due to work function differences, the electric field increases. This increases the ON current. Due to use of Junctionless transistor, the leakage current i.e. off current is low. Hence the Ion/I off ratio increases significantly. Figure. 3 shows the characteristics of current ratio for both the devices.

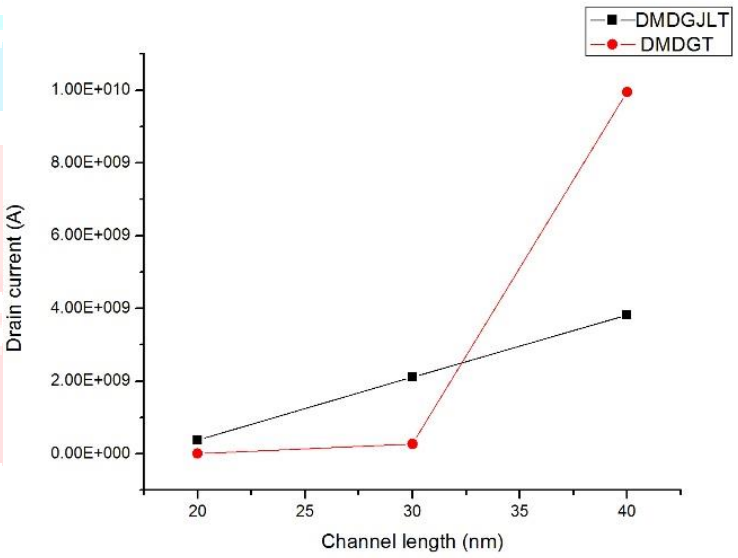

Fig.3 I on/ I off ratio characteristics for DMDGJLT and DMDGT for 20,30 and 40 nm channel lengths.

Table 3 shows that for 20nm and 30nm, the Ion/I off ratio is much greater in DMDGJLT than in DMDGT while for 40nm, it is slightly higher in DMDGT.

Table 3 I on/ I off Ratio Readings

Type	Channel Length (nm)	Ion/Ioff Ratio
DMDGJLT	20	3.79E+08
	30	2.11E+09
	40	3.81E+09
DMDGT	20	1.17E+05
	30	2.73E+08

	40	9.95E+09

3.3 S. S (Sub-threshold slope)

Sub-threshold Swing is defined as the variation in the gate voltage required to have a decade variation in drain current. Higher SS means that the device can have a fewer orders of change in drain current from the off state to the V_T, which in turn means a higher off current for a given V_T. SS can be made smaller close to 60mV/decade by using thinner gate oxide thickness or lower substrate doping concentration. S slope deceases when the gate oxide thickness and or silicon film thickness are increased. Figure. 4 indicates the slope for both DMDGJLT and DMDGT devices.

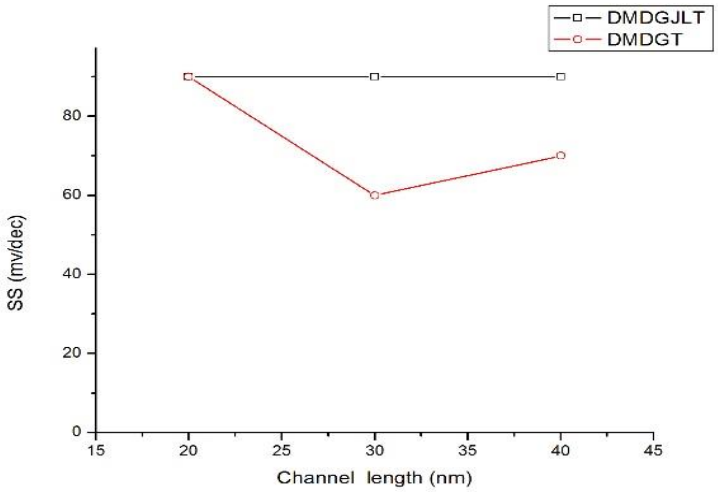

Fig.4 Sub-threshold slope for DMDGJLT and DMDGT for 20,30 and 40 nm channel lengths.

The simulation results of the SS for junctionless and junction transistor are summarized in Table 4. It is linear for DMDGJLT whereas for DMDGT it is varying according to the channel length. The values of SS for 20 nm length DMDGJLT and DMDGT are equivalent. As channel length is increased SS for DMDGT is less.

Table 4 Sub-threshold slope Readings

Type	**Channel Length** (nm)	**SS** (mV/ decade)
DMDGJLT	20	90
	30	90
	40	90
DMDGT	20	90
	30	60
	40	70

IV. CONCLUSION

A detailed study of DMDGJLT has been performed by developing a simulation model. The parameters like DIBL, SS, Ion/I off ratio have been examined and compared with DMDGT. We observed that when the channel length is lesser, the Junctionless transistor has better results for DIBL (34.61% improvement) and Ion/I off ratio (by 10^3). These results varied when the channel lengths of the transistors were changed between 20 nm, 30 nm and 40 nm.

Hence, DMDGJLT performed satisfactorily for some of the parameters and can be used in low voltage and high frequency applications.

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