Power Management for Low Power VLSI design

[1]Diwakar Tiwary, [2]Mohd Javeed
[1]Assistant Professor, [2]Assistant Professor
[1]Department of Electronics and Communication Engineering,
[1]Sree Dattha Institute of Engineering and Science, Ibrahimpatnam, R.R District, Telangana, India

Abstract: Low power is the major challenge for today's electronics industries. Power dissipation is an important consideration in terms of performance and space for VLSI Chip design. Power management techniques are generally used to designing low power circuits and systems. This paper discuss about the various methodologies and power management techniques for low power VLSI design that can meet future challenges to designs low power high performance circuits. It also describes the many issues regarding circuits design at architectural, logic and device levels and presents various techniques to overcome difficulties.

Index Terms **- VLSI, Power consumption, Dynamic power, Clock gating.**

I. INTRODUCTION

In the past decades, the major challenge for the VLSI designer was area, performance, cost and power consumption. In recent years, however, this has begun to change and, increasingly power consumption is being given comparable weight to area and speed considerations. Now a day's power is the primary factor for the remarkable growth and success in the field of personal computing devices, telecommunication system which demand high speed computation and complex functionality with low power consumption. The motivations for reducing power consumption differ application to application and circuits to circuits. In the area of micro powered battery operated portable applications such as cell phones, the aim is to keep the battery lifetime and weight reasonable and packaging cost low. For high performance portable computers such as laptop and mobiles, the objective is to reduce the power dissipation of the electronics circuits of the system to a point which is about half of the total power dissipation. Finally for the high performance non battery operated system such as workstations the overall goal of power minimization is to reduce the system cost while ensuring long term device reliability. For such high performance systems, process technology has driven power to the fore front toallfactorsinsuchdesigns.Atprocessnodesbelow100 nm technology, power consumption due to leakage has joined switching activity as a primary power management concern. The motivations for reducing power consumption differ from application to application. In the class of micro-powered battery- operated, portable applications, such as cellular phones and personal digital assistants, the goal is to keep the battery lifetime and weight reasonable and the packaging cost low. Power levels below 1-2 W, for instance, enable the use of inexpensive plastic packages. For high performance, portable computers, such as laptop and notebook computers, the goal is to reduce the power dissipation of the electronics portion of the system to a point which is about half of the total power dissipation (including that of display and hard disk). Finally, for high performance, non battery operated systems, such as workstations, set-top computers and multimedia digital signal processors, the overall goal of power minimization is to reduce system cost (cooling, packaging and energy bill) while ensuring long-term device reliability. These different requirements impact how power optimization is addressed and how much the designer is willing to sacrifice in cost or performance to obtain lower power dissipation.

2. SOURCES OF POWER CONSUMPTION

When we recognized power consumption as a design constraint, Power per MHz is commonly used representation of a component. With a closer look at power dissipation, it becomes obvious that the subject is not that simple. Electric current is not constant during operation and peak power is an important concern. The device will malfunction due to electro- migration and voltage drops even if the average power consumption is low. The equation for the average power consumption is given as

$$P_{avg} = P_{dynamic} + P_{short} + P_{leakage} + P_{static} \quad [1]$$

So the total average power consumption is depends on Dynamic power consumption, Short-circuit power consumption Leakage power consumption and static power consumption. The leakage current which is primarily determined by the fabrication technology consists of reverse bias current in the parasitic diodes formed between source and drain diffusions and the bulk region in a MOS transistor as well as the sub threshold current that arises from the inversion charge that exists at the gate voltages below the threshold voltage. The short-circuit current which is due to the DC path between the supply rails during output transitions and the charging and discharging of capacitive loads during logic changes. The short- circuit and leakage currents in CMOS circuits can be made small with proper circuit and device design techniques. The main source of power dissipation is the charging and discharging of the junction capacitances. Switching activity is a measure for the number of gates and their outputs that change their bit value during a clock cycle. To toggle between logic zero and logic one can discharged and charged the junction capacitor. The electric current that flows during this process causes dynamic power dissipation *Pdynamic*. The dynamic power is depend upon the capacitive output load Cout and the supply voltage Vdd and frequency of clock signal.

$$P_{dynamic} = K\ Cout\ Vdd^2\ f \quad [2]$$

K is the average number of positive transitions during one clock cycle and f the clock frequency. By reducing power supply will therefore have the greatest effect on saving power, taking into consideration that typically $P_{dynamic}$ is responsible for 80% of P_{avg}.

3. LOW POWER DESIGN STRATEGIES

There are different strategies available at different level in VLSI design process for optimizing the power consumption.

Table 3.1 different strategies for optimizing power consumption.

Design Level	**Strategies**
Operating System Level	Portioning, Power down
Software level	Regularity, locality, concurrency
Architecture level	Pipelining, Redundancy, data encoding
Circuit / Logic level	Logic styles, transistor sizing and energy recovery
Technology Level	Threshold reduction, multi threshold devices

4. LOW POWER TECHNIQUES FOR VLSI

There are many techniques that have been developed over the past decade to address the continuously aggressive power reduction requirements of most of the high performance. The basic low-power design techniques, such as clock gating for reducing dynamic power, or multiple voltage thresholds (multi-Vt) to decrease leakage current, are well-established and supported by existing tools.

Table 4.1 Techniques for power Consumption

Techniques	**Dynamic Power Reduction**	**Leakage power reduction**	**Other Power reduction Techniques**
Clock Gating	Clock Gating	Minimize usage of low Vt cells	Multi Oxide devices
Power Gating	Power Efficient Techniques	Power Gating	Minimize capacitance by custom design
Variable Frequency	Variable Frequency	Back Biasing	Power efficient circuits
Variable Voltage Supply	Variable Voltage Supply	Reduce Oxide Thickness	----------
Variable Device Threshold	Variable Island	Use Fin FET	----------

It is an overview of known techniques which gives an idea of what methodology is applicable. Optimizing for power entails an attempt to reduce one or more of these factors. To address the challenge to reduce power, the semiconductor industry has adopted a multifaceted approach, attacking the problem on four fronts:

1. *Reducing chip and package capacitance*: It can be achieved by process development like SOI with partially or fully depleted wells of semiconductors, CMOS scaling to submicron device areas, and advanced interconnect substrates such as Multi-Chip Modules (MCM). This process is very effective but very expensive and has its own pace of development and introduction to the market.
2. *Scaling the supply voltage:* This technique can be very effective in reducing the power dissipation in circuit, but requires new IC fabrication process. Supply voltage scaling also requires support circuitry for low-voltage operation including level-converters and DC/DC converters.
3. *Employing better design techniques:* This approach promises to be very successful because the investment to reduce power by design is relatively small in comparison to the other three approaches and because it is relatively untapped in potential.
4. *Using power management strategies*: The power savings that can be achieved by various static and dynamic power management techniques are very application dependent, but can be significant. Dynamic power consumption depends linearly on the physical capacitance being switched. So, in addition to operating at low voltages, minimizing capacitances offers another technique for minimizing power consumption. Interconnect plays an increasing role in determining the total chip area, delay and power dissipation, and hence, must be accounted for as early as possible during the design process.

REDUCING SWITCHING ACTIVITY

In addition to voltage and physical capacitance, switching activity also affect dynamic power consumption. A chip may contain an enormous amount of physical capacitance, but without any switching then there will be no dynamic power consumption.

Minimization of Glitches

Gates' delays are often assumed zero to simplify estimation. In this way an important aspect of reality, glitch power, is left out. In a static logic gate, the output or internal nodes can switch before the correct logical value is being stable. Imagine an AND-gate with two inputs of different delay time and the transition 01 and 10. At a zero delay gate the output would be a stable logic zero but in our example the first port has a lower delay, which forces the output to a temporary logic one, after which it stabilizes on zero again. The power lost during this unnecessary switching activity is called glitching power loss.

Minimization of the Number of Operations Minimizing the number of operations to perform a given function is critical to reducing the overall switching activity. To illustrate the power trade-offs that can be made at the algorithmic level, consider the problem of compressing a video data stream using the vector quantization (VQ) algorithm.

Low Power Bus

Busses are known for their heavy loads, long interconnects and therefore their large capacitances. This is due to their connections to large cores spread across the die of a SoC. Reducing the capacitance is normally not possible and reducing the switching activity is the only chance of reducing power loss.

Therefore, coding the transmitted data for minimum switching activity is the methodology of the choice

POWER DOWN MODES

Systems have to be designed to meet certain constraints in which they have to operate. Since these limits normally show worst case situations, the system typically is not working at maximum possible performance. Parts of the chip are idle, do not add any functionality to the design at the time, but still consume power. The reasons are unnecessary changes on the inputs of the unused devices and the load they add to the clock-signal, which continuously toggles whether the devices are processing or not. Reasonably these parts should be turned off.

Power Supply Shutdown

Shutting down power supply reduces power dissipation to zero. This is the most effective way to save power in idle modules. Several conditions have to be fulfilled to employ this methodology.

1. The power switch will have to be well designed. A resistance and delay value is tied to a real switch. A straight forward implementation would be a transistor with a low ON resistance. Therefore, its width has to be increased, which results in a large capacitance. Buffering circuitry is needed to operate the switch at a satisfactory performance.
2. It takes a delay time of DT before supply voltage stabilizes in a switched back on module. This makes the methodology applicable for components with an idle time greater then DT only.
3. The design must not contain any storage units like registers or memory because their values would be lost during power down. It is possible to add extra logic to save and later restore the data, but the logic and power overhead for this proceeding has to be well examined.
4. Powering down and up will result in transient noise and voltage drops in a carefully designed power supply grid. These effects must be adequately shielded to avoid functional failures.

The numerated points suggest that power supply shutdown is applicable for a very coarse level of granularity only and one has to realize that it is very invasive and disturbing to a design.

Clock Gating

Instead of switching off power supply, the clock signal may be halted in idle devices. This reduces switching activity and therefore dynamic power consumption to zero. Inserting clock gates is not as great of an interference to the design as power supply shutdown and can be used on components with lower granularity. This makes clock gating applicable for applications where power shut down is no alternative. Clock gating won't lessen power dissipation to zero since leakage power is unaffected.

Enabled Flip-Flops

As clock gating can be seen as a softer alternative to power supply shut down, enabled flip flops are the next less aggressive (and less effective) strategy. Registers are replaced by a representative with an enable signal. By enabling these representatives, they behave like general registers. Disabled, the flip-flops' outputs are not changing, which reduces switching activity in the circuit. The most active signal, the clock, is still active though, ensuing a great deal of power dissipation.

SYSTEM DESIGN

System level low power design techniques should be most promising for reducing energy consumption. Two methodologies are denoted in this section. Chapter 3.4.1 focuses on low power hardware- software partitioning and shows possible power savings of approximately 77%. chip's I/O communication, which is responsible for up to 33% of overall system power consumption in typical designs. *HW/SW Partitioning*

The Micro PP Plus will be an embedded system with two processor cores, a controller and a DSP. Services can be implemented either in software running on these cores, or in dedicated hardware. In our design flow this will be decided during the step of hardware- software partitioning. This process has great influence on system power. This is illustrated in the following example:

Specific hardware is generally more efficient. 330mW are consumed to perform an addition using a SPARC lite processor core in an exemplary technology (0.32mm / 1.8V / 16.8 MHz).

A custom adder in the same technology consumes only 2mW plus additional communication overhead. *Integration of Chip Components*

Implementing systems using present day technology results in third or more of total power being consumed at the chip's input/output (I/O) ports. The larger capacitances of chip's boundaries compared to internal gates and higher voltages are the reason for this observation. Typical values for internal capacitances reside around 10's of femto farads, where I/O pins reach dimensions of 10's of pico farads. Nowadays supply voltages for chip- cores tend to be lower then 2.0V. In industrial systems not all components of a design might be state of the art and require higher voltages or technical constraints require them. Still, these different components have to communicate over their I/O. This makes dual voltage systems (lower voltage for the cores – higher voltage for I/O) quite common.

5. CONCLUSION & FUTURE SCOPE

In this paper, various strategies and methodologies for power consumptions are discus and reviewed. The need for lower power systems is being driven by many market segments. Unfortunately designing for low power adds another dimension to the already complex design problem and the design has to be optimized for power as well as Performance and Area. Over all system power dissipation can roughly be divided into three parts: 33% I/O, 33% cores/memory and 33% control logic. Energy consumption breaks down into dynamic, static, leakage and short circuit power dissipation. Dynamic power, with a share of 80% is the starting-point for most of the introduced methodologies.

A low voltage/low threshold technology and circuit design approach, targeting supply voltages around 1 Volt and operating with reduced thresholds.

- Low power interconnect, using advanced technology, reduced swing or reduced activity approaches.
- Dynamic power management techniques, varying supply voltage and execution speed according to activity measurements.

This can be achieved by partitioning the design into sub-circuits whose energy levels can be independently controlled and by powering down sub-circuits which are not inuse.

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