A Novel 65 Level Asymmetric Multi-Cell Cascaded Multilevel Inverter

[1]N.Bala Lakshmi , [2]P.Ram Vasanth Reddy, [3]P.Manasvi, [4]B.Sonia,[5]D.Satyanath,[6]K.Lakshmi Ganesh
[1]UG Student, [2] UG Student, [3] UG Student, [4] UG Student, [5]UG Student, [6]Assistant Professor
[1]Department of EEE, PSCMR Engineering and Technology, JNTUK, Vijayawada, Andhra Pradesh, India.
[2]Department of EEE, PSCMR Engineering and Technology, JNTUK, Vijayawada, Andhra Pradesh, India.
[3]Department of EEE, PSCMR Engineering and Technology, JNTUK, Vijayawada, Andhra Pradesh, India.
[4]Department of EEE, PSCMR Engineering and Technology, JNTUK, Vijayawada, Andhra Pradesh, India.
[5]Department of EEE, PSCMR Engineering and Technology, JNTUK, Vijayawada, Andhra Pradesh, India.
[6]Department of EEE, PSCMR Engineering and Technology, JNTUK, Vijayawada, Andhra Pradesh, India.

Abstract *:* In earlier, many multilevel structures are came into exist. Among that cascaded multilevel inverters are mostly popular. On the base of series connection of dc voltage sources in which its uses standard low voltage configurations, this type of multilevel inverters integrates the medium voltage output. This peculiar allows one to attain high quality output voltage and current waveforms by using different topologies. So the main theme of this paper is to attain higher output voltage level with less number of switches, less weight, less place, less cost and lower THD values. It is only possible when by using asymmetric multi-cell topology. Hence this paper inaugurates newly proposing 65 level asymmetric multi-cell cascaded multilevel inverter. The main reason behind this paper is to improve the fundamental component and to reduce the THD value. In order to verify the a novel 65 level Asymmetric multi-cell cascaded MLI, MATLAB/SIMULINK software is used and the results were presented.

IndexTerms **- Cascaded H-Bridge Multi-level Inverter, multi-cell Configuration, total harmonic distortion (THD).**

I. INTRODUCTION

Converter or Inverter means, which converts fixed DC voltage to variable AC voltage. Then converting due to the switching action and infinite number of odd harmonics present in it hence it doesn't produce a pure sinusoidal waveform. Then it gives a square wave. If a square wave is used for electrical equipment's life span of the equipment's is diminishes. This drawback is retrieved by using multilevel inverters which produces a staircase voltage waveform which is equal to approximate sinusoidal waveform [1], [2].

Multilevel inverters are nothing but the various voltage values in a cycle. It is the best solution for medium voltage and high power applications. The basic reason of the multilevel inverter is to use a number of power semiconductor switches in order to combine a staircase voltage waveform with a peak value of sum of all multiple input DC sources. Here the inputs used as batteries, PV cells, fuel cells etc. The sum of these multiple DC sources are controlled by power semiconductor switches to attain high output voltage. The most usual semiconductor switching devices are MOSFET, IGBT. The power inverter circuits require a relatively stable DC power source capable of supplying enough current to meet the power demands of the system. There are mainly three types of multilevel inverters which are diode clamped, flying capacitor, Cascaded multilevel inverters [3], [4]. Among all CMLI is mostly used. If diode clamped and flying capacitor is used to increase the output voltage level according to level the components like diodes and capacitors are also increased. Hence the main drawback for using these topologies is complexity, due to the capacitor imbalance, real power flow is different and needs high voltage rating diodes to block reverse voltages and also switching utilization and efficiency are poor for real power transmission. Hence these topologies are not used to get higher output level. In that case multilevel inverters are used to get higher output voltage level.

In fact, CMLI are also divided into two types 1. Symmetric CMLI 2. Asymmetric CMLI. Symmetric cascaded multilevel means equal DC voltages with equal magnitude which is given to the input. In this symmetric topology the relation between levels and bridges is L=2N+1, where L is the level and N is the number of bridges. Asymmetric cascaded multilevel inverter means DC voltage sources with unequal magnitudes are given to the input. Hence in symmetric CMLI topology number of switching components along with level increases. This disadvantage will be reduced by using asymmetric CMLI topology. Hence a newly proposed Asymmetric multi-cell topology was implemented to attain the higher quality output voltage waveform with less number of switches. In this present paper, existing system of 7 level symmetric CMLI, proposed system of 25 level asymmetric multi-cell cascaded multilevel inverter and newly proposed a novel 65 level asymmetric multi-cell CMLI are presented and also to reduce the THD value and to smoothen the waveform LC filter is used.

II. EXISTING SYSTEM

In this existing system, 7 level symmetrical cascaded multilevel inverter is discussed. Actually the series H-bridge inverter was discovered in 1975, but a number of patents have been obtained for this topology as well. The voltage and power level may be easily scaled due to this topology consists series of power conversion cells. Hence the output phase voltage can be expressed as V=V1+V2+V3+--------- Vn. In this topology no need of extra clamping diodes and balancing capacitors.

In order to construct 7 level symmetric CMLI, three bridges are to be used based on formula. Hence total 12 switches are utilised to build three bridges and these three full bridges are arranged in cascaded connection as the first arm of the first bridge is taken as a positive terminal, the second limb of the first bridge is connected to the first arm of the second bridge. The second limb of the second bridge is connected to the first arm of the third bridge and as well as the second arm of the third bridge is considered as negative terminal. Here the inputs given to each bridge is 100V, 100V, 100V because the existing system is a symmetric CMLI topology. The block diagram of the seven level symmetric CMLI is as shown in the Fig. 1.

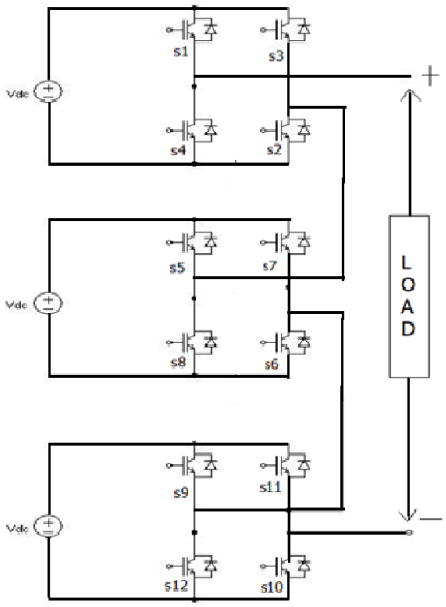


Fig. 1 block diagram of Existing system

TABLE I

SWITCHING TABLE FOR EXISTING SYSTEM

voltages	switches
0V	S1, S3, S5, S7, S9, S11
100V	S1, S2, S5, S7, S9, S11
200V	S1, S2, S5, S6, S9, S11
300V	S1, S2, S5, S6, S9, S10
-100V	S3, S4, S5, S7, S9, S11
-200V	S3, S4, S7, S8, S9, S11
-300V	S3, S4, S7, S8, S11, S12

Here Vdc=100V, the switches are named as S1, S2, S3, S4, S5, S6, S7, S8, S9, S10, S11, S12. These switches are supervised to get seven levels in the output as 0V, 100V, 200V, 300V, -100V, -200V, -300V due to the bridges are connected in series. To trigger the switches gate pulses are given in which switching configuration table is used to study the switches on and off period. Hence the switching configuration table for the seven level symmetric cascaded multilevel inverter is as shown in the table 1. Here clearly given the switches on and off for obtained levels. For example, to get 200V i.e., 100V the switches like S1, S2, S5, S7, S9, S11 are trigged. The output can obtain seven levels which is shown in simulation results.

III. PROPOSED SYSTEM

The main disadvantage for the existing system is require more number of switching components to attain higher output. This may increase the complexity and increases the switching losses. Hence this symmetric topology is not efficient to get higher output. Now asymmetric multi-cell cascaded multilevel inverter is currently used topology to get high quality voltage output with less number of switches. Hence this method is used in this paper.

In this present paper 25 level is implemented by using asymmetric multi-cell CMLI topology. In the existing to get the seven level total 12 switches are used. But here the same switches are supervised to get 25 levels in the output. Hence this topology is adorable solution to get higher output with less number of switches. In this multi-cell topology, the switching components are also connected in series and across of the DC voltage sources other than the full bridges. In the proposed system total two bridges are used as 12 switches are used. For each bridge two DC voltage sources are used then the inputs given to the first bridge is 26V, 26V and for the second bridge the inputs given as 130V, 130V. Hence the output voltage attains as 312V which forms a 25 levels in the output. This topology can give a better quality waveform of output voltage, reduces a voltage stress due to fundamental frequency. Hence this topology is used for the high power applications. To trigger the switches gate pulses are given for that switching table is used. The block diagram of the proposed system is as shown in Fig.2 and the switching table is shown in table 2 for clear understand of switches on and off periods. Here LC filter is used to reduce the THD values and also to smoothen the waveform. The values taken are L=90mH C=55µF and R=70Ω.

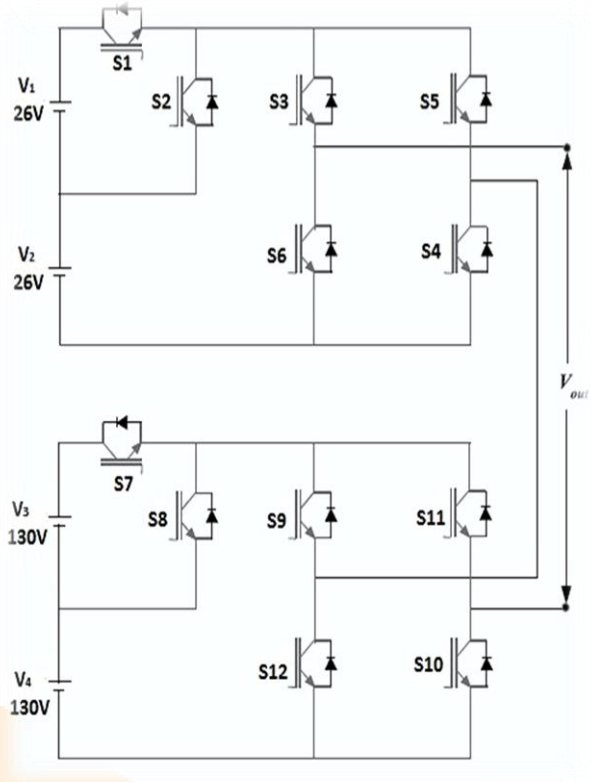


Fig. 2 Block diagram of the proposed system

TABLE II

SWITCHING TABLE FOR PROPOSED SYSTEM

Voltage	Switches
0V	S1, S3, S5, S7
26V	S1, S2, S5, S7, S10
52V	S1, S2, S5, S7, S9
78V	S3, S4, S5, S6, S9, S12
104V	S3, S4, S5, S6, S10, S12
130V	S1, S3, S5, S6, S12
156V	S1, S2, S5, S6, S10, S12
182V	S1, S2, S5, S6, S9, S12
208V	S3, S4, S5, S6, S9, S11
234V	S3, S4, S5, S6, S10, S11
260V	S1, S3, S5, S6, S11
286V	S1, S2, S5, S6, S10, S11
312V	S1, S2, S5, S6, S9, S11
-26V	S3, S4, S5, S7, S10
-52V	S3, S4, S5, S7, S9
-78V	S1, S2, S7, S8, S9, S12
-104V	S1, S2, S7, S8, S10, S12
-130V	S1, S3, S8, S7, S12
-156V	S3, S4, S7, S8, S10, S12
-182V	S3, S4, S7, S8, S9, S12
-208V	S1, S2, S7, S8, S9, S11
-234V	S1, S2, S7, S8, S10, S11
-260V	S1, S3, S7, S8, S11
-286V	S3, S4, S7, S8, S10, S11
-312V	S3, S4, S7, S8, S9, S11

From the table, it is clearly given as to get the 26V the switches like S1, S2, S5, 57, S10 are triggered then current path for this level is26V→S2→S3→LOAD→S11→S9→S4→-26V. The proposed system is operated in 25 modes and these modes are controlled by changing the switching period of the switching devices(IGBT). Each switch is designed to operate at particular time intervals.

IV. NEWLY PROPOSED SYSTEM

In this newly proposed system, 65 level asymmetric multi-cell cascaded multilevel inverter is implemented. By using this topology THD value is decreases by increasing the output levels. The main theme of this paper is to design 65 level asymmetric multi-cell CMLI with less number of switches. Suppose in symmetric topology to get 65 level total 128 switches are used which may increase the switching losses and also the complexity. If in this asymmetric multi-cell topology, just 18 switches are needed to attain 65 level. Hence this topology is very promising topology to attain higher output level with less number of switches.

For 65 level asymmetric multi-cell topology three bridges are used which are arranged in cascaded connection. The first limb of the first bridge is considered as a positive terminal hence it is connected to positive terminal of the load and at the same way the second limb of the third bridge is considered as a negative terminal then it is connected to the negative terminal of the load. Here the inputs given to the first bridge as 10.16V, 10.16V. Second bridge has the input voltages as 50.81V, 50.81V and the inputs given to the third bridge is 101.63V, 101.63V. The block diagram of 65 level asymmetric multi-cell cascaded multilevel inverter is as shown in the Fig. 3

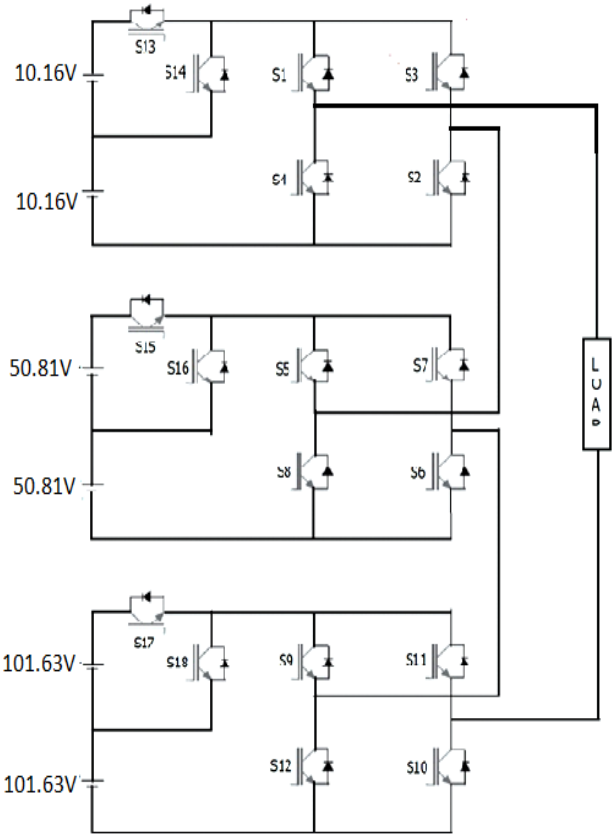


Fig. 3 Block diagram of the newly proposed system

Here the desired inputs are given to meet the grid voltage which is 325.25V and also to meet the power demands. These 18 switches are supervised to get higher quality output voltage. To understand the gate pulses of the switches, switching configuration table is given below

This newly proposed system is operated in 65 modes and all these 65 modes are controlled by changing the switching periods. Table 3 shows in which switches are on for the desired level for example to get the 2nd level of 10.16V the switches like S1, S2, S5, S7, S9, S11, S14 are turned on with the help of gate pulses given to the switches. Hence by this method THD will be reduced in easier way. These levels are build up to form a 65 level output waveform. In order to get grid voltage the inputs are taken according to attain the peak of grid voltage. Here fundamental frequency is used hence the problems of switching losses and voltage stress is reduced. The resultant outputs are shown in Simulink results. The switching table for newly proposed system is as shown in the Table 3.

TABLE III

SWITCHING TABLE FOR NEWLY PROPOSED SYSTEM

Voltages	Switches
0V	S1,S3,S5,S7,S9,S11
10.16V	S1,S2,S5,S7,S9,S11,S14
20.32V	S1,S2,S5,S7,S9,S11,S13
30.48V	S3,S4,S5,S6,S9,S11,S13,S16
40.64V	S3,S4,S5,S6,S9,S11,S14,S16
50.8V	S1,S3,S5,S6,S9,S11,S16
60.96V	S1,S2,S5,S6,S9S,S11,S14,S16
71.12V	S1,S2,S5,S6,S9,S11,S13,S16
81.28V	S3,S4,S5,S6,S9,S11,S13,S15
91.44V	S3,S4,S5,S6,S9,S11,S14,S15
101.6V	S1,S3,S5,S6,S9,S11,S15
111.76V	S1,S2,S5,S6,S9,S11,S14,S15
121.92V	S1,S2,S5,S6,S9,S11,S13,S15
132.08V	S3,S4,S5,S6,S9,S10,S13,S16,S18
142.24V	S3,S4,S5,S6,S9,S10,S14,S16,S18
152.4V	S1,S3,S5,S6,S9,S10,S16,S18
162.56V	S1,S2,S5,S6,S9,S10,S14,S16,S18
172.72V	S1,S2,S5,S6,S9,S10,S13,S16,S18
182.88V	S3,S4,S5,S7,S9,S10,S13,S17
193.04V	S3,S4,S5,S7,S9,S10,S14,S17
203.2V	S1,S3,S5,S7,S9,S10,S17
213.36V	S1,S2,S5,S7,S9,S10,S14,S17
223.52V	S1,S2,S5,S7,S9,S10,S13,S17
233.68V	S3,S4,S5,S6,S9,S10,S13,S16,S17
243.84V	S3,S4,S5,S6,S9,S10,S14,S16,S17
254V	S1,S3,S5,S6,S9,S10,S16,S17
264.16V	S1,S2,S5,S6,S9.,S10,S14,S16,S17
274.32V	S1,S2,S5,S6,S9,S10,S13,S16,S17
284.48V	S3,S4,S5,S6,S9,S10,S13,S15,S17
294.64V	S3,S4,S5,S6,S9,S10,S14,S15,S17
304.8V	S1,S3,S5,S6,S9,S10,S15,S17
314.96V	S1,S2,S5,S6,S9,S10,S14,S15,S17
325.22V	S1,S2,S5,S6,S9,S10,S13,S15,S17

V. SIMULATION RESULTS

A. Existing System

The Simulink result output voltage waveform is as shown in the Fig. 4. Here in the output seven levels are obtained with a peak of 300V because the maximum input given the circuit is 300V.

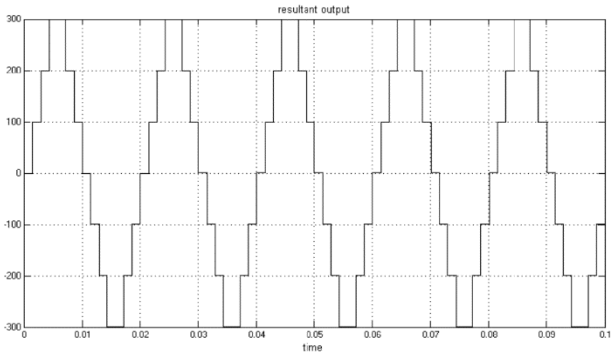


Fig. 4 Seven level output voltage waveform of existing system

B. Proposed System

In this proposed system two bridges are used namely inverter 1 and inverter 2 for the inverter 1 the voltages given is 26V, 26V hence the inverter 1 output voltage waveform with a peak of 52V is as shown in the Fig. 5.

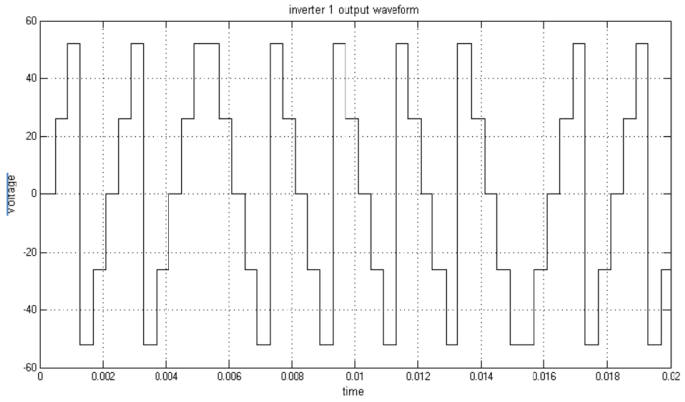


Fig. 5 Inverter 1 resultant output voltage waveform of proposed system

The input voltage which is given to the 2nd inverter is 130V, 130V hence the resultant voltage of second inverter is as shown in the Fig. 6

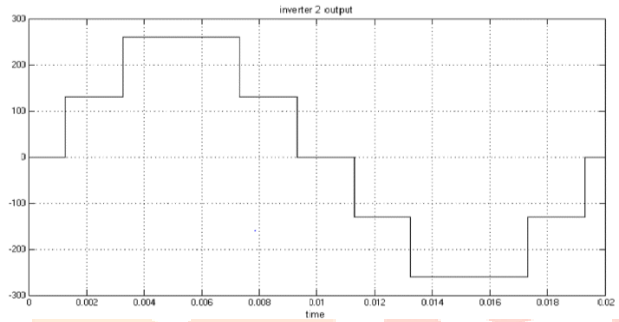


Fig. 6 Inverter 2 resultant output voltage waveform of proposed system

Hence the resultant output voltage of 25 level Asymmetric multi-cell cascaded multilevel inverter is as shown in the Fig. 7.

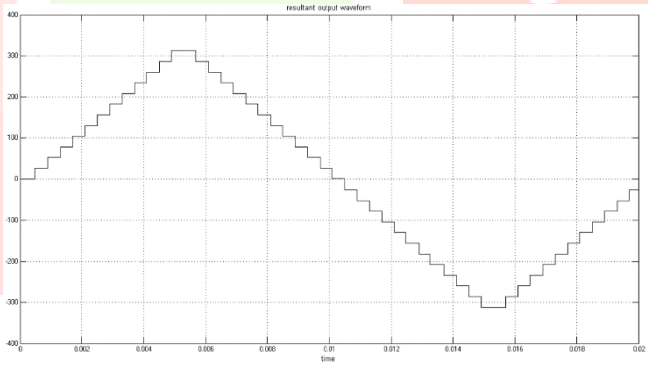


Fig. 7 Twenty five level resultant output waveform of the proposed system

C. Newly Proposed System

In newly proposed 65 level asymmetric multi-cell CMLI, the output can consists 65 levels in which positive half cycle have 32 steps and also negative half cycle have 32 steps and this is integrated by the three inverters hence the inverter 1 output voltage waveform with a peak of 20.32V is shown in Fig.8

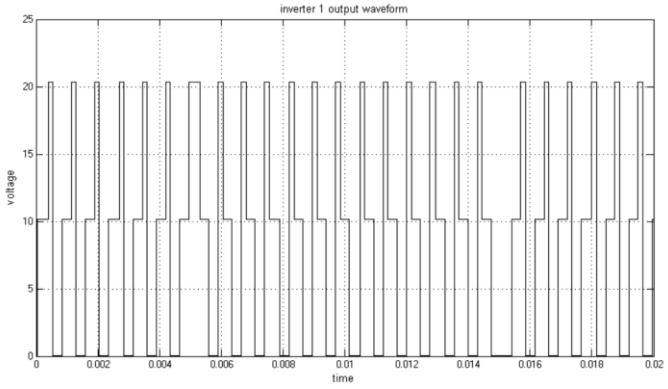


Fig. 8 Inverter 1 output voltge waveform of newly proposed system

Inverter 2 has the input voltage of 101.64V hence the inveter 2 ouput voltage with a peak of 101.64V ia as shown in the Fig. 9

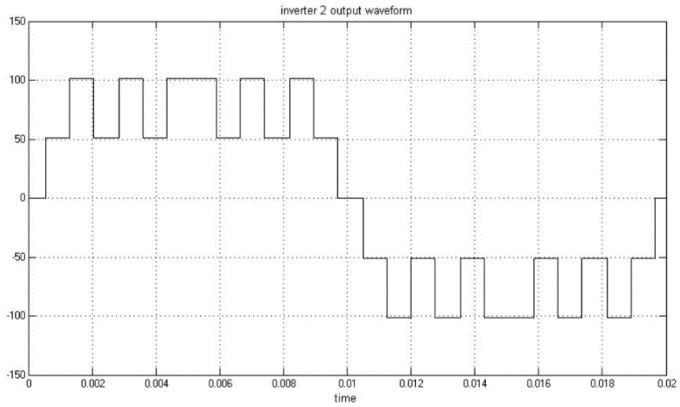


Fig. 9 Inverter 2 output voltage waveform of newly proposed system

Inverter 3 has the input voltage of 203.6V. Hence the inverter 3 output voltage waveform with a peak of 203.6V is as shown in the Fig. 10

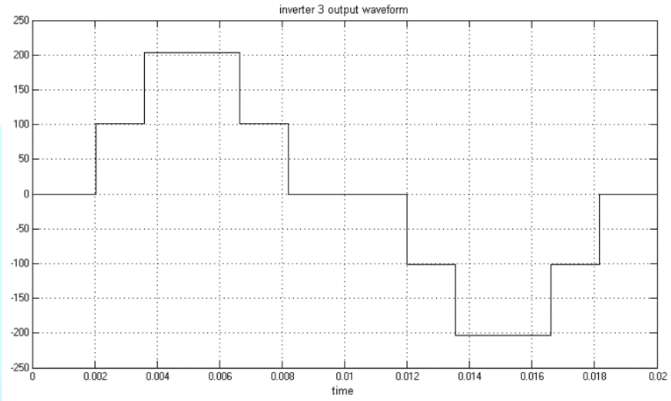


Fig. 10 Inverter 3 output voltage waveform of newly proposed system

The integration of the three inverters outputs will form the resultant output voltage waveform with a peak of 325.22. Hence the result output of the 65 level asymmetric multi-cell cascaded multilevel inverter is shown in the Fig. 11

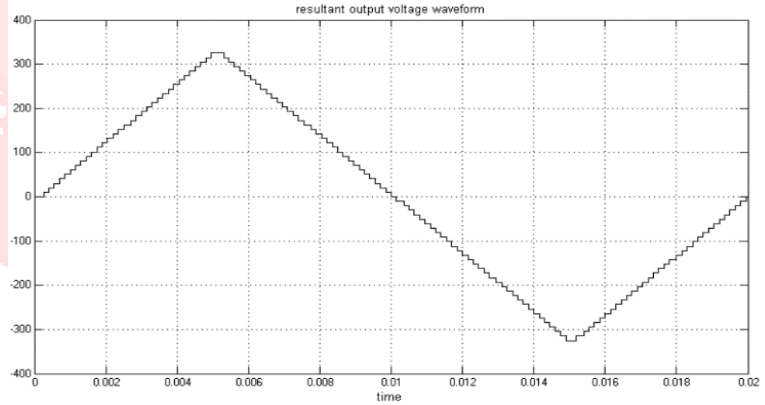


Fig. 11 Sixty five level resultant output voltage waveform of newly proposed system

VI. FFT ANALYSIS

A. Existing System

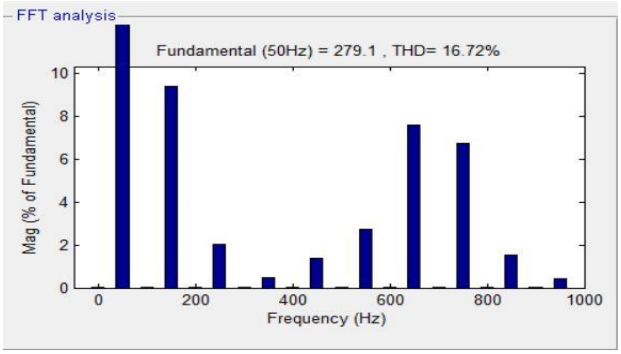


Fig. 12 Existing System of THD without LC filter

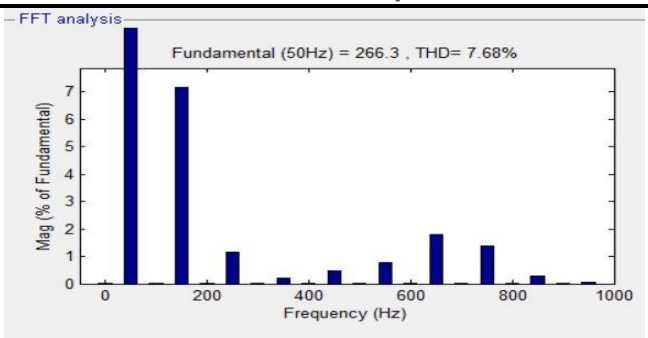


Fig. 13 Existing System of THD with LC filter

B. Proposed System

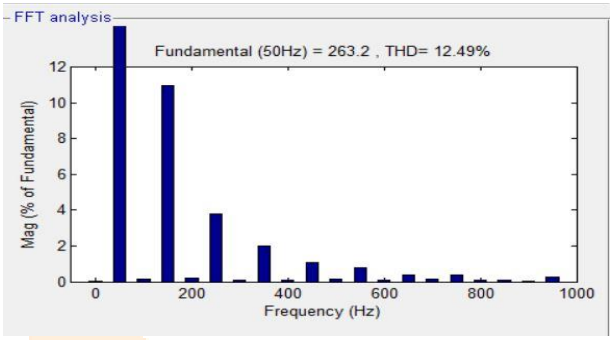


Fig. 14 Proposed System of THD without LC filter

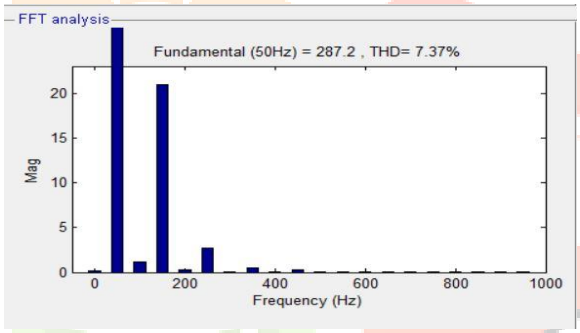


Fig. 15 Proposed System of THD with LC filter

C. Newly Proposed System

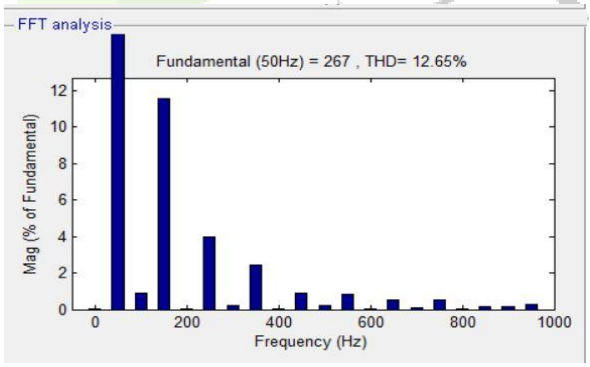
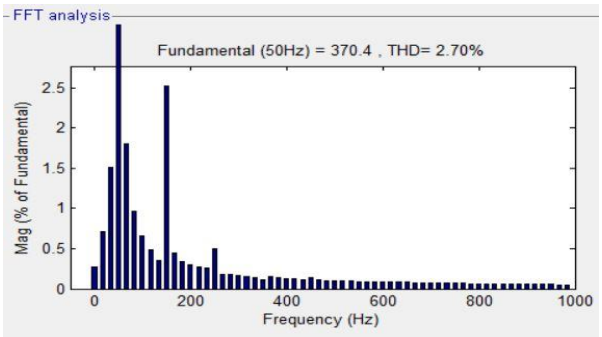


Fig. 16 Newly Proposed System of THD without LC filter



VII. CONCLUSION

Hence the existing system of seven level symmetric CMLI, proposed system of 25 level asymmetric multi-cell CMLI and also newly proposed 65 level asymmetric multi-cell CMLI are deeply discussed. Here the output of the newly proposed system 65 level cascaded multilevel inverter is connected the grid. Hence THD value is decreased to get the approximate sine wave in order to reduce the disadvantages. And the for the existing system the THD values are 16.72% and 7.68% for without and with LC filter, for the proposed system the obtained THD's are 12.49% and 7.37% and also for newly proposed system 12.65% and 2.70% are attained. Hence this new topology is the best topology to achieve the low THD value with less number of switches.

REFERENCES

[1]. Babaei E, Alilu S. "A new general topology for cascaded multilevel inverters with reduced number of components based on developed H-bridge". *IEEE Trans Ind Electron* 204;61(8):3932-9.

[2]. Malinowski Mariusz, Gopalkumar K, Rodriguez Jose, Pe'rez Marcelo A. "A survey on cascaded multilevel inverters". *IEE Trans Ind Electron* 2010;57(7):2197-205.

[3]. Wu JC, Wu KD, Jou HL, Xiao ST. "Diode-clamped multi-level power converter with azero-sequence current loop for three-phase three-wire hybrid power filter". *Elsevier J Electrical power systems Res* 2011;81(2):263-70.

[4]. Khoucha Farid, Laguon Mouna Soumia, Kheloui Abdelaziz, Benbouzid Mohamed El Hachemi. "A comparision of symmetrical and asymmetrical three-phase H-bridge multilevel inverter for DTC induction motor drives".*IEE Trans Energy convers* 2011;26(1):64-72.

[5]. Ebrahimi J, Babaei E Gharehpetian GB. "A new topology of cascaded multilevel converters with reduced components for high-voltage applications". *IEE Trans Power Electron* 2011;26(11):3119-30.

[6]. Esfandiari Ehsan, Marium Norman Bin. "Experimental results of 47-level switch-ladder". *IEE Trans Ind Electron*2013;60(11);4960-7.