Low Power VLSI design of 4-Bit CEPAL adder using Cadence 0.18µM CMOS Full adder

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Abstract : Full adder is the basic block of all arithmetical and logical circuits found in microcontroller and microprocessor inside arithmetic and logic unit (ALU). This paper presents the of design of 4-Bit adder using both 28 transistor full adder and CEPAL full adder also gives the comparative analysis of these two designs with the conventional CMOS Full adder circuit. The proposed and conventional designs have been simulated using CADENCE Virtuoso Simulator with gpdk 0.18µM CMOS technology.

IndexTerms **- Adder, CEPAL adder, Full-Adder, Low-Power Adder.**

I. INTRODUCTION

With the continuously increasing chips complexity and number of transistors, circuits' power consumption is growing as well. Technology trends shows that circuit delay is scaling down by 30%, performance and transistor density are doubled approximately every two years, and the transistor's threshold voltage is reduced by almost 15% every generation. All of these technology trend leads to higher and higher power consumption in circuits[2]. The battery technology does not advance at the same rate as the microelectronics technology and there is a limited amount of power available for the mobile systems. The goal of extending the battery life span of portable electronics is to reduce the energy consumed per arithmetic operation, but low power consumption does not necessarily imply low energy[2].

Full adders have been utilized as a base circuit in various arithmetic circuits to carry out arithmetic operations like addition, subtraction, multiplication, address calculation and MAC unit etc..Apart from arithmetic operations, adders are utilized to generate memory locations in different architectures of microprocessors and cache memories. Thus improvement in the full adder would prove more beneficial for all the circuits where its application has a significant effect in the performance of the circuit where it has been employed. The most important parameters to be kept in consideration are compactness and power which affects the performance and usefulness of any VLSI circuit[1].

The most basic arithmetic operation is the addition of two binary digits. This simple addition consists of four possible elementary operations such as:

0 + 0 = 0,
0 + 1 = 1,
1 + 0 = 1,
and 1 + 1 = 10.

In above addition first three will generate only sum bit but when both 1's are added the it produces carry bit also. So a typical adder takes the inputs and generates the sum and carry as the outputs.

This paper aims at the analysis and improvement of power efficiency of the full adder using 28 transistor full adder and CEPAL full adder. The CEPAL (Complementary Energy Path Adiabatic Logic) full adder is a low power full adder which utilizes very low power comparing with the other full adder architectures.

This paper is organized as fallows. Section I gives the Introduction, Section II describes about Full-Adder circuit. Section III shows the 4-Bit adder using full adder circuit, Section IV gives the simulation results of the three types of full adders and using them in 4-bit adder circuit. Section V Shows the Comparative analysis In section V concludes the paper.

II. FULL ADDER

The Full-Adder is a combinational circuit that performs the addition operation of 2 input bits and 1Previous carry bit and produces 2 output bits.

Let the input variables are A, B and C_{in}. and the two output variables are sum (S) and carry (C_{out}). Then the Truth-Table for the sum and carry is given by

Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Figure 1:Truth Table

K-Map for the above truth-Table are

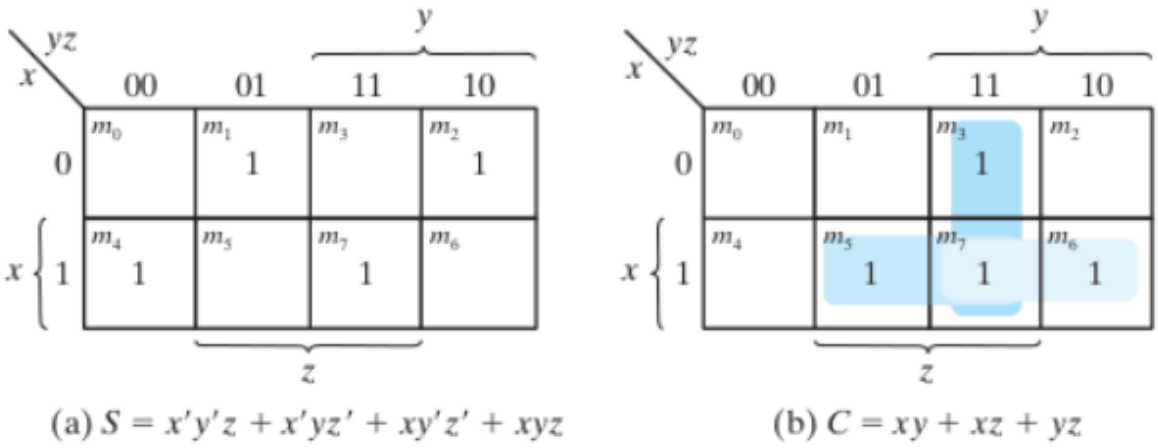


Figure 2:K-Map for the above truth table

The Boolean expression for full adder outputs are given by

$$SUM = A \oplus B \oplus C_{in} \quad (1)$$

$$C_{out} = AB + (A \oplus B)C_{in} \quad (2)$$

If we observe the above Boolean expressions the basic element used is the XOR gate which generates basic addition operation in the adder circuits. A single XOR generates simple two bit addition i.e. it behalves like a single half adder, for generating sum in a full adder we need 2 XOR gates. The XOR gate conventionally uses 14 transistors.

The schematics of NAND,NOR,XOR,XNOR are given by

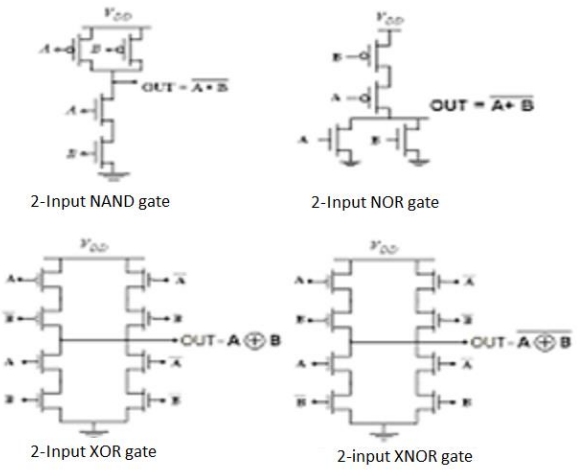


Figure 3: Schematics of 2-input NAND, NOR, XOR, XNOR

The logic diagram of the conventional CMOS full adder using logic gates is given by

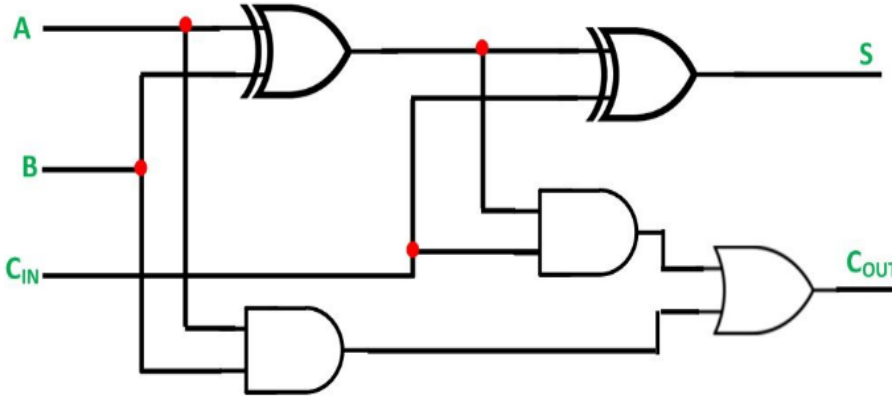


Figure 4:Conventional full adder using logic gates

III. 4-BIT ADDER USING FULL ADDER

The 4-Bit adder using full adder is given by

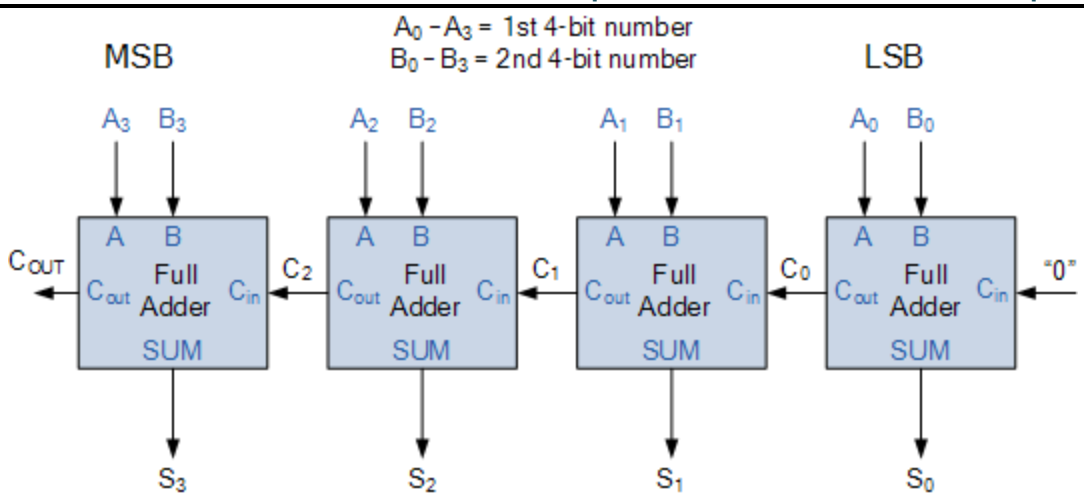


Figure 5: 4-Bit adder using full adders

IV. SIMULATION RESULTS

One bit adder using logic gates in cadence virtuoso schematic editor is given by

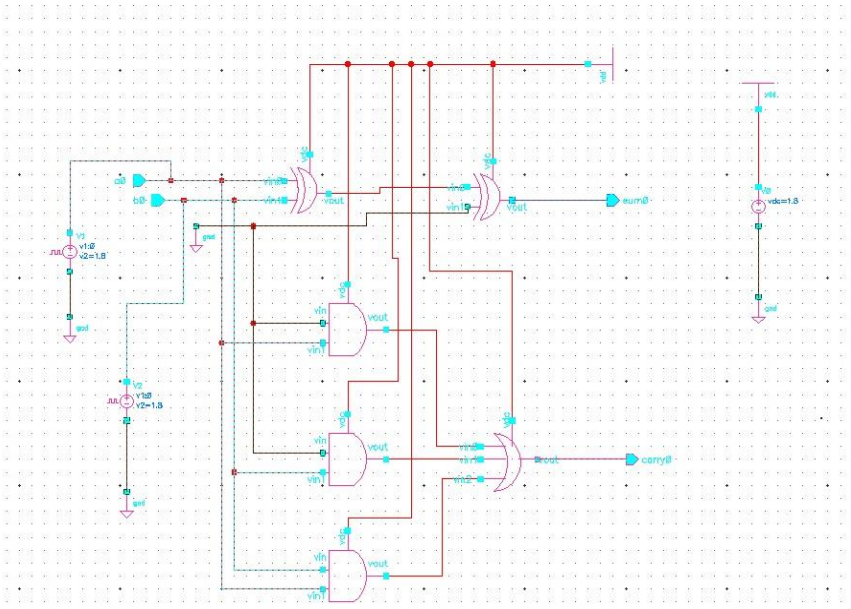


Figure 5: Schematic of 1-Bit adder using full logic gates

The one bit adder using 28 transistors in cadence virtuoso schematic editor is

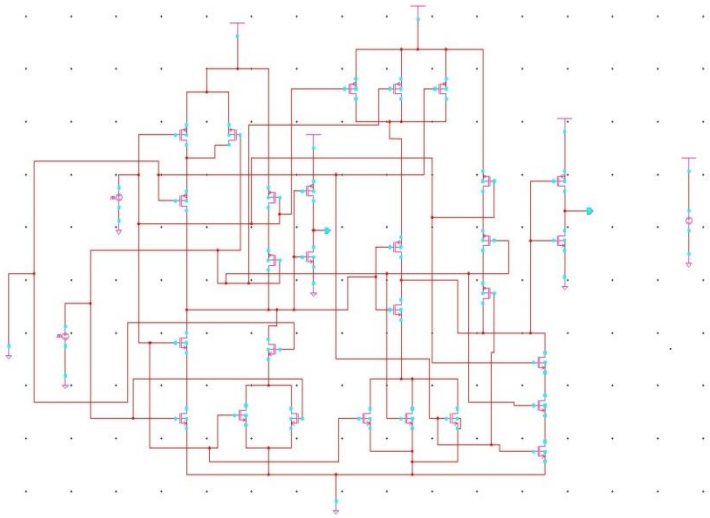


Figure 6: Schematic of 1-Bit adder using 28 transistors

2-bit adder using CMOS Complementary Energy Path Adiabatic Logic

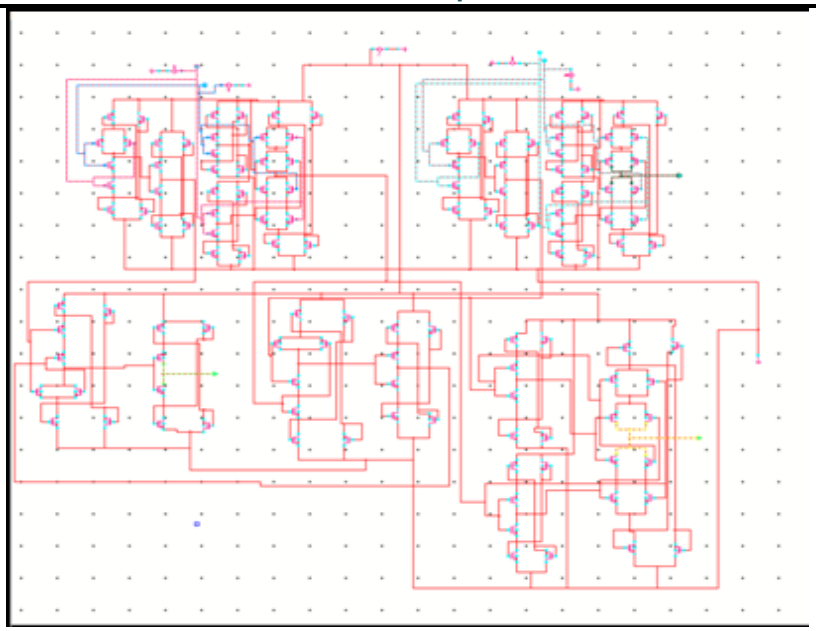


Figure 7: Schematic of 2-Bit adder using CEPAL technique

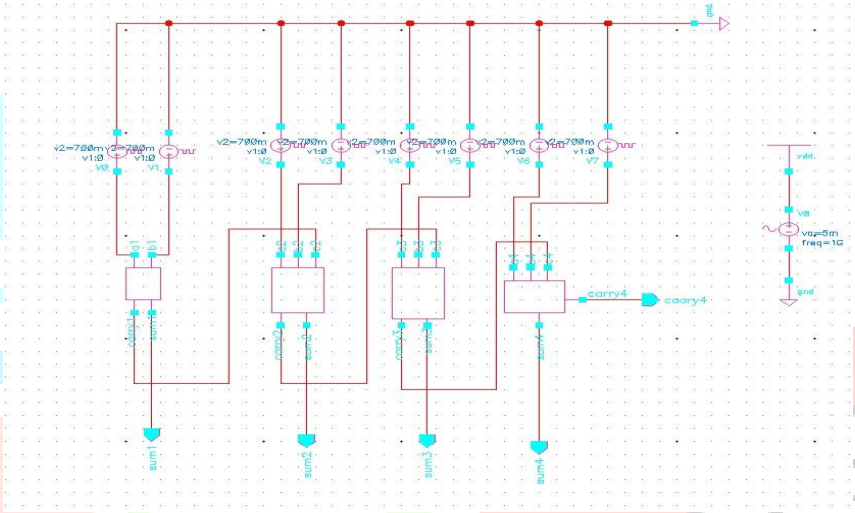


Figure 8: 4-Bit Adder using CEPAL full adders

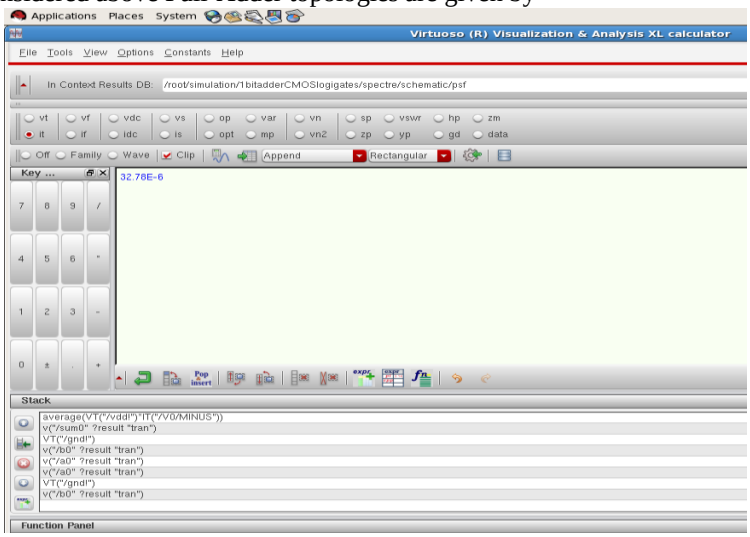
V. POWER CONSUMPTION OF VARIOUS FULL ADDERS

There are three types of power consumption in VLSI circuits namely short circuit power, static power and dynamic power. The short circuit power dissipation is due to the short circuit current generated when both NMOS and PMOS transistors are simultaneously active for a small duration. The static power dissipation varies with process technology.

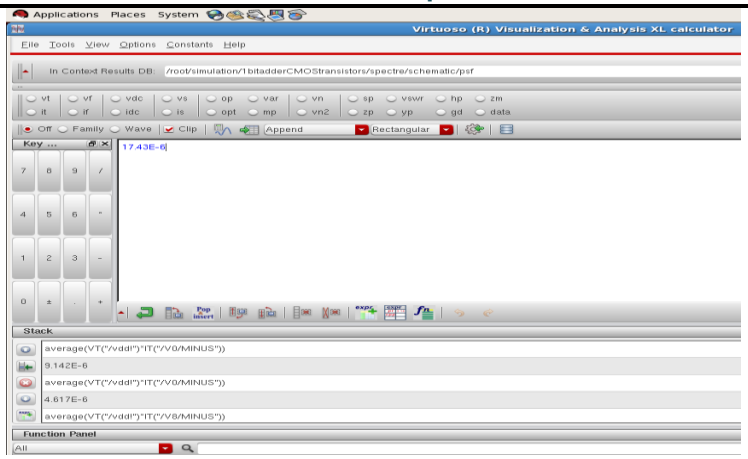
$$P_{average} = P_{Leakage} + P_{Short\text{-}circuit} + P_{Dynamic} \quad (3)$$

The Complementary Energy Path Adiabatic Logic uses double the number of transistor but consumes very low power than the other full adder architectures the main advantage with the CEPAL is the power loss due to short circuit is extremely low.

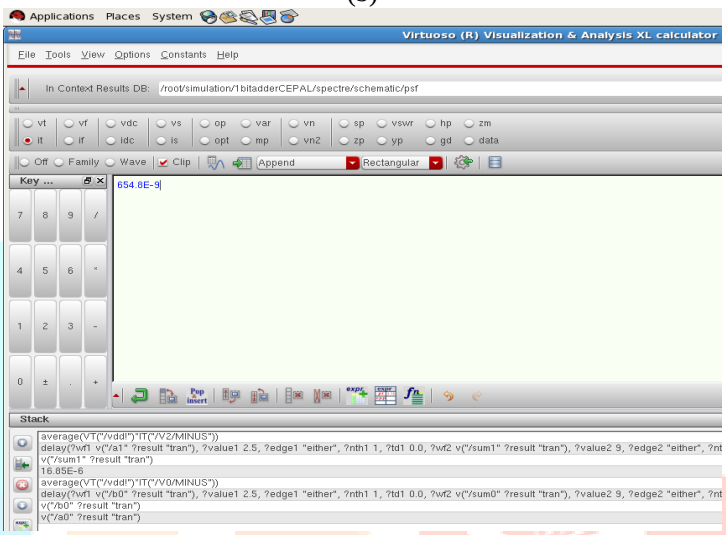
The power consumptions of the considered above Full-Adder topologies are given by



(a)



(b)



(c)

Figure 9: Power Consumptions of (a) CMOS Logic gates Full adder (b) 28T CMOS full adder (c) CEPAL Full adder

Table 1:Comparison Table

	1-Bit Full adder		
	Using logic gates	**Using 28T**	**Using CEPAL**
Power consumption	32.7µWatts	17.4µWatts	654.8nWatts

Power consumption of CEPAL 4-Bit adder is shown in below figure

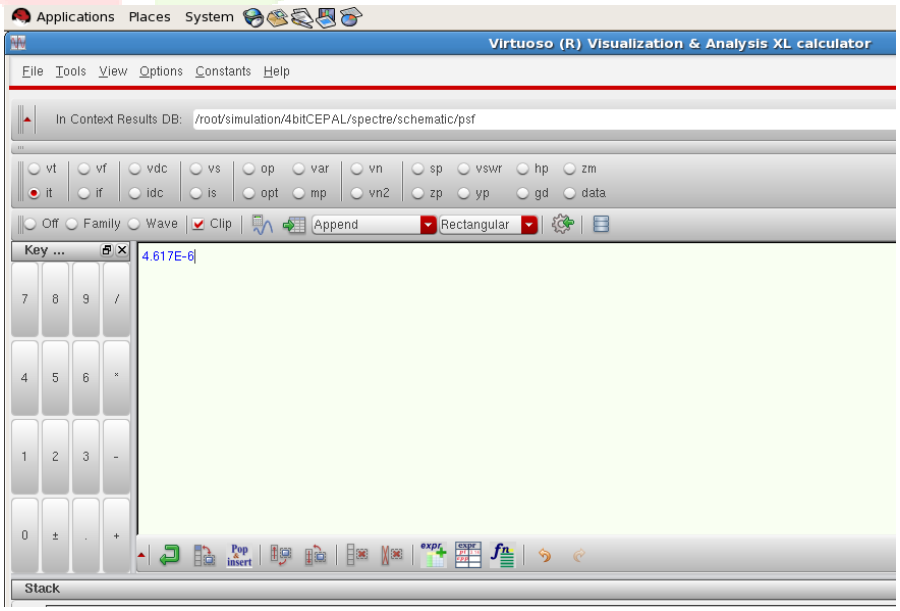


Figure 10: Power Consumption of a 4-Bit CEPAL adder

VI. CONCLUSION

In this paper we have presented the Low power CMOS full adder design using both the 28 transistors full adder and Complementary Energy Path Adiabatic Logic Full adder, even though the CEPAL full adder uses double the number of transistor but consumes very low power than

the other full adder architectures the main advantage with the CEPAL is the power loss due to short circuit is extremely low. The power consumption of a 28 transistor full adder is having 17.4µWatts where 2-bit CEPAL adder utilizes only 654.8nWatts, the overall power consumption of 4-Bit adder using CEPAL is 4.617µWatts comparingly very low power than the other design styles.

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