ANALYSIS OF OPTIMIZATION TECHNIQUES PURSUINGFOR LOW POWER VLSI CIRCUIT

ADILAKSHMAMMA T, Dr S.Venkatanarayanan
[1]Research Scholar
SSSUTMS, Sehore
[2]Research Guide
SSSUTMS, Sehore

ABSTRACT

The main objective of this work is to study the various optimization techniques for reducing power consumption in VLSIcircuit systems without any tradeoff with the desired and necessary tasks it has to perform. As VLSI circuit systems are used in a wide range of applications, there is a need to meet the design metrics of embedded systems like power, time to market, flexibility, robustness, cost, performance and many more. Power consumption is particularly an important design metric for battery powered embedded systems (small sized batteries can have very limited lifetime). Power optimization can be implemented using various techniques like Dynamic Voltage scaling, Dynamic Frequency Scaling, Software Optimization, Power down mode and Sleep mode. However, power consumption is also very important in systems running from power supplies, since the IC chips can become hot very quickly when their clock speeds are increased. Minimizing power consumption in such circumstances is very much desirable to improve reliability and system cost.

Key words: Low power, Optimization, VLSI Circuits, Power Consumption

INTRODUCTION

In the previous decades, the principle focal point of VLSI designers were execution, area and design cost. Power consumption was for the most part of just auxiliary significance moderately. Notwithstanding, this pattern has started to change and, with significant need, power consumption is given equivalent significance to speed and area. The upside of using blend of low-power design methods in conjunction with low-power parts is more important at this point. Warmth age in top of the line PC items constrains the doable IC bundling and execution of circuits and in this manner builds the bundling and cooling costs. Warmth drew into the room, the power expended and the workplace clamor reduces with low power VLSI chipset. Necessities for lower power consumption keep on increasing altogether as segments move toward becoming battery-powered, minimal and require complex usefulness. At sub micro meter process hubs, spillage power consumption has joined exchanging action as an essential power administration concern.

RELATED CONCEPTS

A. Power Dissipation Basics

Total power consumption by a CMOS device is given by,

Pdissipation = Pstatic + Pdynamic + Pshort circuit..... (a)

Dynamic power or switching power is power dissipated during charging or discharging of capacitors and is described below [1] [2].

Pdyn = CL* Vdd2 *α * f..... (b)

Where CL: Load Capacitance is a function of fan-out, wirelength, and transistor size,

Vdd: Supply Voltage, which has been dropping with successive process nodes,

α: Activity Factor

f :Clock Frequency, which is increasing at each successive process node.

Short-circuit power dissipation occurs due to short circuit current(Isc) that flows when both the NMOS and PMOS devices are simultaneously 'on' for a short time duration and is given by the below equation,

Pshort-circuit = Isc * Vdd * f..... (c)

Static power dissipation is due to reverse saturation, sub-threshold and leakage current and occurs especially when the device is in idle mode. It is given by the below equation.

Pstatic = f(Vdd , Vth, W/L) .....(d)

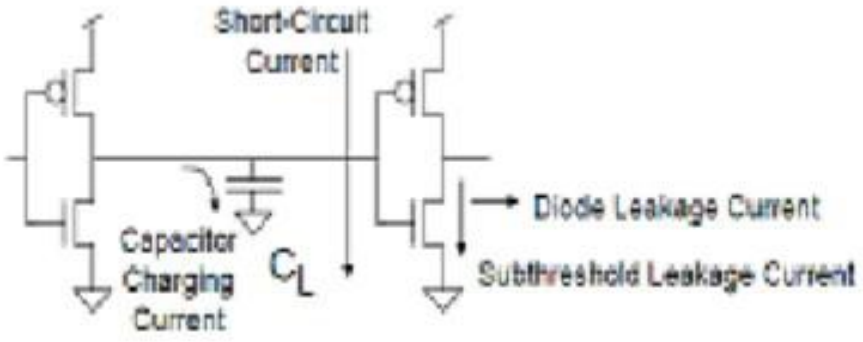


Figure 1: Power Dissipation in CMOS

whereVth is threshold voltage, 'W' is transistor width and 'L' is transistor length

Figure-1 shows the various components responsible for power dissipation in CMOS.

B. Low Power Strategies

Low power designs strategies at various abstraction levels are listed in table 1.

Design level	Strategies
Operating system level	Portioning, power down
Software level	Regularity,locality,concurrency
Architecture level	Pipelining, Redundancy, data encoding
Circuit / logical level	Logic styles, transistor sizing and energy recovery
Technology level	Threshold reduction, multi threshold devices

Table 1: strategies for low power designs

Effective power management is possible by using the different strategies at various levels in VLSI Design process. So designers need an intelligent approach for optimizing power consumptions in designs.

C. Power Optimization Techniques

Table-2 describes low power techniques used at different levels [3][4].

Traditional techniques	Dynamic power deduction	Leakage power reduction	Other power reduction techniques
Clock gating	Clock gating	Minimize usage of low vt cells	Multi oxide devices
power gating	Power efficient techniques	Power gating	Minimize capacitance by custom design
Variable frequency	Variable frequency	Back baising	Power efficient circuits
Variable voltage supply	Variable voltage supply	Reduce oxide thickness	

Variable device threshold	Variable Island	Use fit FET	

Table 2: Few low power techniques used today

CIRCUIT LEVEL

We study optimizations that decrease switching activity power of individual logic-gates and transistor-level combinational circuits in this section.

A. Complex Gate Design

In the design of complex gates, e.g., $f = \overline{(a + b) \cdot c}$, choices regarding the placement of individual transistors in the gate can be made. For example, in the N part of the CMOS gate implementing the above function f, the parallel transistor pair a + b can be connected to the gate output or the transistor driven by c can be connected to thegate output. Similarly, given $g = a \cdot b \cdot c$, any serial requesting of a, b and c can be picked in the N part of a CMOS gate executing g. It is notable that late arriving signs ought to be set nearer to the yield to limit gate proliferation delay. In any case, the normal power scattered is subject to the progress probabilities of the gate inputs and the inward hub capacitances. (Inward hub capacitance is because of parasitic deplete and source capacitance and interconnect capacitance.) Requesting of gate data sources will influence both power and deferral. In [5] and [6] techniques to streamline the power as well as postponement of rationale gates in light of transistor reordering are given. Direct upgrades in power and postponement can be gotten by a sensible requesting of transistors inside individual complex gates.

B. Transistor Sizing

Transistor estimating in a combinational gate circuit can have critical effect on circuit deferral and power dissemination. In the event that the transistors in a given gate are expanded in estimate, at that point the postponement of the gate diminishes, nonetheless, power scattered in the gate increments. Further, the postponement of the fanin gates builds in view of expanded load capacitance. Given a postpone limitation, finding a proper measuring of transistors that limits power scattering is a computationally troublesome issue. A run of the mill way to deal with the issue is to process the slack at each gate in the circuit, where the slack of a gate relates to how much the gate can be slowed down immediately of the circuit. Sub circuits with slacks more noteworthy than zero are prepared, and the sizes of the transistors decreased until the point that the slack ends up plainly zero, or the transistors are generally least size. Variations of the above approach are introduced in [6] and [7].

LOGIC LEVEL

We survey optimizations that reduce switching activity power of logic-level combinational and sequential circuits in this section.

A. Combinational

Combinational rationale streamlining has generally been disintegrated into two stages: innovation autonomous advancement and innovation subordinate enhancement. In the primary stage rationale conditions are controlled to decrease area, postponement or power dispersal. In the second stage the conditions are mapped to a specific innovation library utilizing innovation mapping calculations, again advancing for area, deferral or power. For an extensive treatment of combinational rationale union techniques focusing on area and deferral, see [8]. In this segment we will review as of late proposed strategies to improve combinational circuits for low power dispersal.

A.1 Don’t-care Optimization

Any gate in a combinational circuit has a related controllability and recognizability couldn't care less set. The controllability couldn't care less set relates to the information blends that never happen at the gate inputs. The discernibleness couldn't care less set compares to accumulations of info blends that deliver similar esteems at the circuit yields. Strategies to lessen circuit area and enhance delay abusing couldn't care less sets have been exhibited (e.g., [9]). The power dissemination of a gate is reliant on the likelihood of the gate assessing to a 1 or a 0. This likelihood can be changed by using the couldn't care less sets. A strategy for couldn't care less enhancement to diminish exchanging movement and in this manner power scattering was displayed in [10]. This strategy was enhanced in [11] where the impact of couldn't care less advancement of a specific gate on the gates in its transitive fanout is considered.

A.2 Path Balancing

Misleading advances represent in the vicinity of 10% and 40% of the exchanging movement power in run of the mill combinational rationale circuits. So as to diminish deceptive exchanging movement, the postponements of ways that join at each door in the circuit ought to be generally equivalent. By specifically adding unit-postpone supports to the contributions of doors in a circuit, the deferrals of all ways in the circuit can be made equivalent. This expansion won't expand the basic deferral of the circuit, and will viably dispense with misleading changes. In any case, the expansion of cushions expands capacitance which may counterbalance the diminishment in exchanging movement. Strategies to diminish instead of totally take out fake exchanging action, while including a negligible number of unit-postpone cushions have been proposed. The design of a multiplier with progress decrease circuitry that achieves glitch diminishment by way adjusting is depicted in [12].

A.3 Factorization

A primary means of technology-independent optimization is the factoring of logical expressions. For example, the expression a · c + a · d + b · c + b · d can be factored into (a + b) · (c + d) reducingtransistor count considerably. Common sub expressions can be foundacross multiple functions and reused. Kernel extraction is a commonly used algorithm to perform multilevel logic optimization for area. In this algorithm, the kernels of the given expressions are generated and kernels that maximally reduce literal count are selected. When targeting power dissipation, the cost function is not literal count but switching activity. Modified kernel extraction methods that target switching activity power are described in [13].

B. Technology Mapping

Once advanced rationale conditions have been acquired, the undertaking remains tomap the conditions into an objective library that contains upgraded rationale doors in the picked innovation. A run of the mill library will contain many GATEs with various transistor sizes. Current innovation mapping strategies utilize a chart covering plan, initially displayed in [14], to target area and postpone cost capacities. The diagram covering detailing of [14] has been stretched out to the power cost work. Under the zero postpone show, the ideal mapping of a tree can be resolved in polynomial time, by broadening the calculation of [14]. Different ways to deal with innovation mapping that expect distinctive defer models and target insignificant power scattering have been portrayed [15].

C. Sequential

We survey methods to optimize sequential circuits for low power in this section. Sequential logic optimization methods work at two levels of abstraction; 1) at the State Transition Graph level and 2) at the logic-gate and flip-flop level.

C.1 Encoding

State encoding for insignificant area is an all-around inquired about issue [2]. These strategies must be adjusted to focus on a power cost work, to be specific, weighted exchanging movement. Naturally, if a states has an extensive number of advances to state q, at that point the two states ought to be given uni-removed codes, to limit exchanging movement at the flip-flounder yields. Be that as it may, the intricacy of the combinational rationale coming about because of a state task ought not to be overlooked. Techniques to encode State Transition Graphs to deliver two-level and multilevel executions with insignificant power are portrayed in [15] and [14]. A technique to re-encode rationale level successive circuits to limit power dissemination is introduced in [14]. Encoding to diminish exchanging action in datapath rationale has additionally been the subject of consideration.

A strategy to limit the exchanging on transports is proposed in [13]. In this strategy, an additional lineE is added to the transport which implies if the esteem being exchanged is the genuine esteem or should be

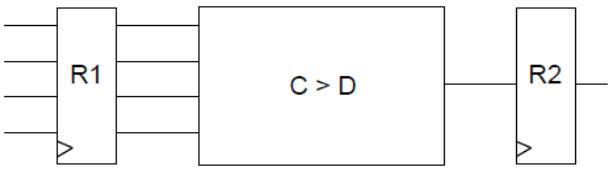
bitwise supplemented upon receipt. Contingent upon the esteem moved in the past cycle, a choice is made to either exchange the genuine current esteem or the supplemented current esteem, in order to limit the quantity of advances on the transport lines. For instance, if the past esteem exchanged was 0000, and the present esteem is 1011, at that point the esteem 0100 is exchanged rather, and the lineE is stated to imply that the esteem 0100 must be supplemented at the opposite end. Different strategies for transport coding are likewise proposed in [39]. Strategies to actualize math units other than in standard two's supplement number juggling are additionally being researched. A strategy for onehot deposit coding to limit exchanging movement of number juggling rationale is introduced in [11].

C.2 Retiming

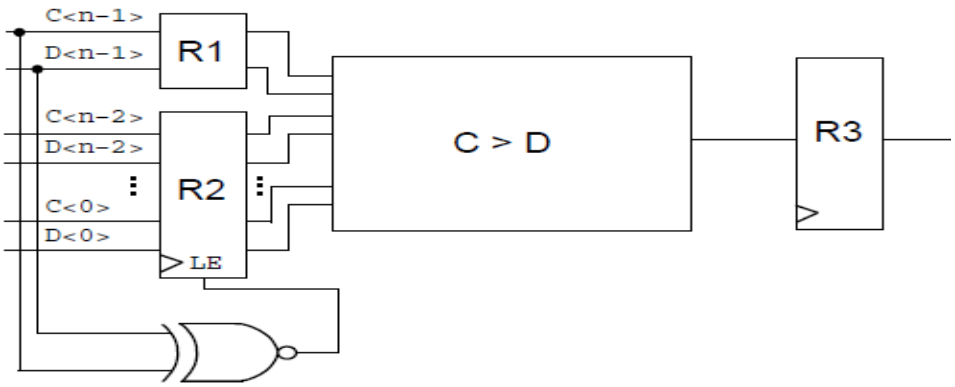
Retiming [12] is an outstanding enhancement technique that repositions the flip-flounders in a synchronous consecutive circuit to limit the required clock time frame. Polynomial-time calculations for least defer retiming and least enroll retiming have been produced. It has been watched that the exchanging action at flip-slump yields in a synchronous successive circuit can be altogether not as much as the action at the flip-tumble inputs. This is on account of there might be numerous misleading changes at the contributions to the flip-flops which are sifted through by the clock. A retiming technique that endeavors the above perception and focuses on the power dispersal of a successive circuit is depicted in [12].

C.3 Gated Clocks

Huge VLSI circuits, for example, processors contain enlist documents, math units and control rationale. The enlist document is normally not gotten to in each clock cycle. So also, in a discretionary consecutive circuit, the estimations of specific registers require not be refreshed in each clock cycle. On the off chance that basic conditions that decide the inaction of specific registers can be resolved, at that point power lessening can be acquired by gating the tickers of these registers [9]. At the point when these conditions are fulfilled, the exchanging movement inside the registers is decreased to insignificant levels. A similar technique can be connected to "kill" or "power down" math units when these units are not being used in a specific clock cycle. For instance, when a branch direction is being executed by a CPU, an increase unit may not be utilized. The info registers to the multiplier are kept up at their past qualities, guaranteeing that exchanging movement power in the multiplier is zero for this clock cycle.



(a)



(b)

C.4 Precomputation

The gated clock worldview of the past segment can be conveyed substantially further. Given a rationale level circuit and a specific information boost, if lingering subcircuits can be identified which don't add to the calculation of the yield reaction for this info jolt, power lessening can be gotten by "killing" the sitting subcircuits. A strategy called precomputation, initially displayed in [1], accomplishes information subordinate power down at the consecutive rationale or combinational rationale level. In a successive precomputation design, the yield rationale estimations of a circuit are specifically precomputed one clock cycle before they are required, and these precomputed esteems are utilized to diminish interior exchanging action in the succeeding clock cycle. A case of one such design connected to a comparator circuit is appeared in Figure 1, taken from [1]. The circuit of Figure 1(a) is a n-bit comparator that analyzes two n-bit numbers C and D and registers the capacity C >D. The circuit with extra precomputation rationale is appeared in Figure 1(b). The precomputation rationale is the rationale that is associated with the heap empower flag of the registers stamped LE.

$$LE = C < n - \otimes > \quad \otimes \quad D < n - 1 >$$

Where stands for the exclusive-nor operator. When the XNOR gate evaluates to a 0, the load enable signal for the registers connected to C< n – 2 : 0 > and D< n – 2 : 0 >is turned off. This means that the outputs of these registers do not switch in the next cycle. The correct value for the output is computed even though these input hold possibly erroneous values because either:

- C < n – 1 > = 1 and D < n – 1 > = 0 in which case the output is a 1 regardless of C < n – 2 : 0 > and D < n – 2 : 0 > , or
- C < n – 1 > = 0 and D < n – 1 > = 1 in which case the output is a 0 regardless of C < n – 2 : 0 > and D < n – 2 : 0 > .

The decrease in power scattering is a component of the likelihood that the XNOR door assesses to a 0. Different information sources can be added to the precomputation rationale to build power diminishment. On the off chance that straightforward locks are utilized as a part of the place of flip-tumbles, the change of Figure 1(b) is material to combinational circuits. Different successive and combinational models depicted in [1] have been produced further. Given a combinational circuit, calculations to decide the sub circuits to be killed, and the rationale required to play out the handicapping are exhibited in [13] and [14]. The strategies of [13] utilize all inclusive measurement to decide the subcircuits and those of [14] utilize recognizability couldn't care less sets to decide the subcircuits. A strategy to diminish exchanging movement in limited state machines by checking for circle edges in the State Transition Graph of the machine, and incapacitating the calculation of the following state for these edges is displayed in [4].

CONCLUSION

We have measured power optimizations applicableat different levels of abstraction, namely the circuit and logic levels. This survey is not comprehensive, rather we have focused a few typical optimizations at each level of abstraction. Further, devicelevel and layout level optimizations to reduce power have not been presented. Lowering power dissipation at altogetherabstraction levels is anemphasis of intense academic and industrial exploration. These methods are being incorporated into state-of-the-art Computer-Aided Design frameworks.

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