Robust Literature Review on Decoders and Sense Amplifier for SRAM based memory systems

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Abstract: Address decoder and sense amplifier is important component of SRAM memory. Selection of storage cell and read operation is depends on decoder and sense amplifier respectively. Hence, performance of SRAM is depends on these components. This work survey the address decoder and sense amplifier for SRAM memory, concentrating on delay optimization and power efficient circuit techniques

Index Terms **– Amplifier, decoder, power efficient, SRAM, storage cell.**

I. INTRODUCTION

In computers data (information) and program (sequence of commands) are store in some physical devices on permanent or temporary basis. This stored content is used in other computing or on time computing depends on the application. For large data which may need to access in future on permanent basis for that magnetic storage is used. Run time data is stored in semiconductor memories. Computer memories are mainly divided into two parts: Primary memory and Secondary Memory. Semiconductor memories come under primary storage. SRAM is random access memory that means its content can be access from anywhere of storage memory. Data are stored in cells and to access data randomly, fix address is assign to all locations of storage cell. SRAMs are volatile in nature that means their storage data will loss after power shutdown. Therefore they can be used to store run time data in computer systems. SRAM is used as register and cache memory to make faster program execution in computer system. SRAMs are made by using same sources as for process made therefore they are compatible with processor in all extent and their speed is matched with current processor speed. SRAM cell are made up with cross couple inverter latch having positive feedback loop therefore during write operation it store data rapidly. For reading it uses Sense Amplifier circuit which amplifies small voltage difference of lines. Semiconductors memories are faster compare to other type of memories and SRAM has highest read and write speed. Power dissipation of SRAM can be reduced by using efficient circuit techniques.

II. LITERATURE REVIEW

Michael A. Turi and José G. Delgado-Frias [1]. Dynamic decoders are always having advantages over static decoders because of their speed and power consumption. in this paper dynamic decoding schemes are discovered. Address decoder using selective pre-charging schemes are presented and analysed here. These schemes are having advantage on simple decoder and the AND-NOR decoders. Results are also compared with conventional one and giving satisfactory performance.

Shivkaran Jain, Arun kr. Chatterjee [2], in their paper has given some NAND gate design styles which when used in decoder educes energy consumption and delay. Basically conventional, NOR style NAND, source coupled NAND is discussed. The three designs conventional, nor style NAND, source coupled NAND, ranges in area, speed and power. In nor style NAND transistors are added in parallel so high fan -in is obtained and logical effort is reduced. In source coupled NAND gate number of transistors is reduced it give speed of operation compared to an inverter.

Ireneusz B., Łukasz Z., [3], in this paper universal decoding scheme is proposed. Universal decoders are made by alternate stage of NAND and NOR gate which avoid unnecessary use of inverters. This paper overcomes problem on simple decoders. AND gate are not available naturally, they are made up by using NOR and NOT gate.

B. S. Amrutur and M. A. Horowitz, [4][5] in this paper low power SRAM techniques are explained. Decoder with different logic style is explained here. Modelling of decoder is also explained here. Logical effort of circuits is calculated and according to that transistors are sized.

Kevin Zhang [6], in this book/literature basic structure of SRAM along with component are explained. Basic design techniques of components are given and sizing issues are discussed. All SRAMs basic parts are covered along with their role in memory optimization.

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