Common Mode Voltage reduction in Diode Clamped MLI using Alternative Phase Opposition Disposition SPWM Technique

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Abstract: The main objective of this paper is to reduce the Common Mode Voltage (CMV) in the Diode Clamped Multilevel Inverter (DCMLI).Three phase Y-connected RL load is connected to DCMLI. The common mode voltage exists between neutral point of Y-connected load and system ground.CMV causes premature failure of bearings of induction motor and is essential to reduce. In this paper, Alternative Phase Opposition Disposition SPWM technique is used to reduce common mode voltage. Two level, five level, seven level and nine level DCMLI are compared in terms of THD and CMV.The effect of a passive LC filter on THD was studied. The simulation of circuit is carried out by using MATLAB/Simulink. Simulation result portrays reduction in THD and CMV by using APOD-SPWM controlled higher level Inverters.

IndexTerms **- CMV, THD, APOD SPWM, DCMLI**

I. INTRODUCTION

CMV is define as voltage between neutral point of the load and the dc midpoint or the voltage between neutral point of load and the system ground or the common mode voltage is defined as the potential of the star point of the load with respect to the center of the D.C. bus of the inverter (or) the common mode voltage (CMV) of the 3-phase system is defined as the voltage potential difference between the star point of the load network and the mid-point of the D.C. link capacitors[1].

$$CMV=\frac{1}{3}\sum_{x=a}^{c} V_{xg} \quad (1)$$

Where V_{ag}, V_{bg}, V_{cg} are the voltages between ground to phase.CMV is zero in purely sinusoidal three phase system but VSI is non-pure sinusoidal system thus it develops CMV. CMV results in high leakage current and premature failure of motor bearing so it is required to reduce [2], [3]. Some modulation techniques based approaches to reduce CMV are MLI using SPWM technique, MLI using Space Vector PWM technique, MLI using Modified space vector modulation technique, predictive current control method, on zero state modulation techniques. In this paper, APOD- SPWM is used to reduce common mode voltage.

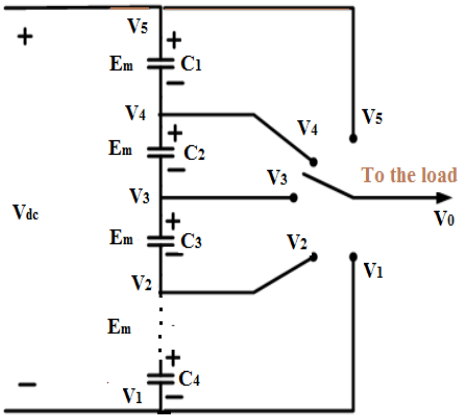

Fig.1.Schematic of single pole of MLI by a switch [5]

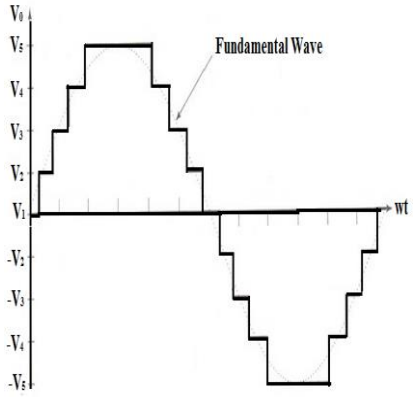

Fig.2.Typical output voltage of 5 level MLI [5]

The idea of multilevel inverters has been introduced in 1975 with invention of cascaded H-Bridge MLI.The term multilevel began with 3- level inverter. Afterwards numerous multilevel inverter topologies have been developed .Three different MLI topologies that have been proposed are diode clamped or neutral point clamped, flying capacitor and cascaded H-Bridge or multicell MLI [4]. In addition, several control strategies have been developed. The series connected capacitors constitute the energy tank for the inverter, providing some nodes to which MLI can be connected. Each capacitor has the same voltage E_m ,which is given by

$$E_m = \frac{E_{dc}}{m-1} \quad (2)$$

Where m denotes the number of levels. The term level refers to number of nodes to which the inverter can be accessible. An m-level inverter needs m-1 capacitors. Figure 2 shows the schematic of a pole in MLI.Pole is regarded as a single-pole, multi-throw switch. Desired output can be obtained by connecting the switch to one node at a time.

Different modulation techniques exist to trigger switches of inverter circuit. The commonly used modulation techniques are as follows

- Sinusoidal pulse width modulation (SPWM) [6]
- Third harmonic PWM (THPWM)
- Space vector PWM (SVPWM) [7]
- Modified Space vector PWM (MSVPWM)

The most popular method of controlling inverter's output voltage is SPWM technique.SPWM is a carrier based pulse width modulation method in which predefined modulation signal is used to determine output voltages. Sinusoidal modulation signal is used in SPWM technique. The gating signal in SPWM is generated by comparing a reference signal of sine shape with a triangular carrier wave.

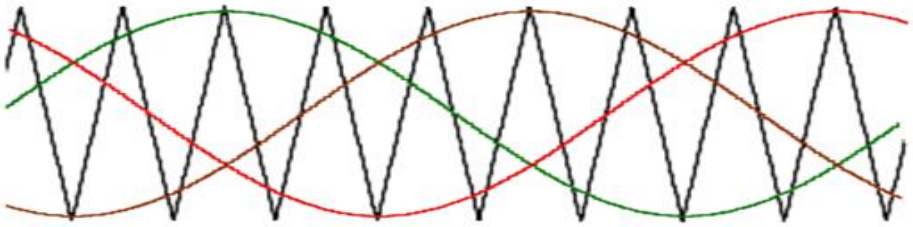

Fig.3.Comparision of reference and carrier signal in SPWM generation

The width of each pulse varied proportionally to amplitude of a sine wave. The output frequency of a inverter can be found by using the frequency of reference signal. The rms output voltage can be controlled by modulation index and intern modulation index is controlled by peak amplitude.SPWM method results in reduction of THD for output voltage.SPWM technique is effective modulation technique and it does not require any additional components and eliminates lower order harmonics easily. Carrier based SPWM techniques are classified as follows

- Single carrier based SPWM technique
- Multi carrier based SPWM technique

Single carrier SPWM technique is used for 2-level inverter whereas multi carrier SPWM technique is used in Multi-level inverters. Multi carrier SPWM technique is further classified as follows

- Phase shift SPWM technique
- Level shifted SPWM technique
- Hybrid SPWM technique

Level shifted SPWM technique is further classified as follows

- Phase Disposition (PD)
- Phase Opposition Disposition (POD)
- Alterative Phase Opposition Disposition (APOD)

Alternative phase opposition disposition SPWM is used to reduce common mode voltage in Diode clamped MLI.

II. Diode Clamped Multilevel Inverter

Diode clamped Inverter (DC-MLI) is also known as neutral point clamped inverter (NPC-MLI). A m level diode clamped inverter typically consists of (m-1) capacitors on the D.C. bus and produces m levels on the phase voltage. The m- level inverter leg requires (m-1) capacitors, 2× (m-1) switching devices and (m-1) × (m-2) clamping diodes [8].

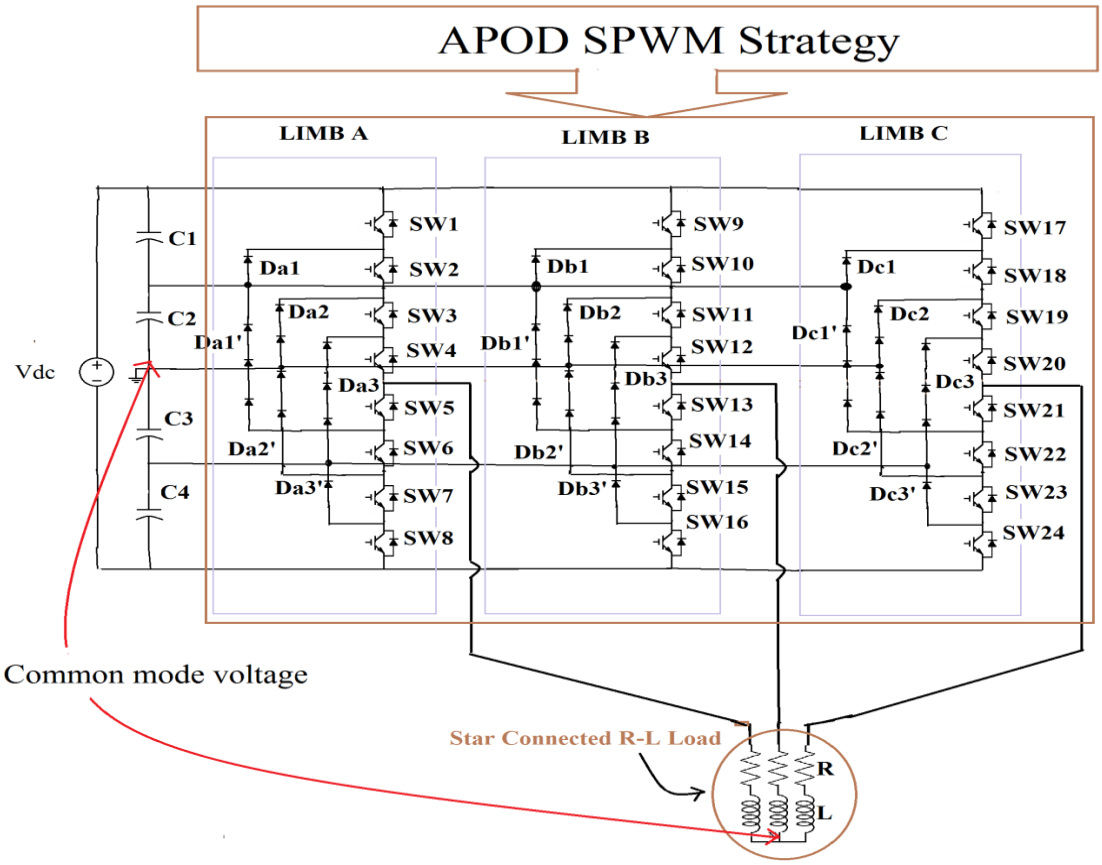

Fig.4.Three phase 5 level DCMLI

For one phase, steps to synthesize the five level voltages are as follows.

1. Turn on all upper half switches of Limb-A i.e., from SW1 to SW4 for an output voltage level $V_{a0} = V_{dc}/2$.
2. Turn on three upper switches of Limb-A i.e., SW2 to SW4 and one lower switch of Limb-A i.e., SW5 for an output voltage level $V_{a0} = V_{dc}/4$.
3. For an output voltage level $V_{a0} = 0$,turn on two upper switches SW3 and SW4 of Limb-A and two lower switches SW5 and SW6 of Limb-A.
4. Turn on one upper switch SW4 of Limb-A and three lower switches SW5 to SW7 of Limb-A for an output voltage level $V_{a0} = -V_{dc}/4$.
5. Turn on all lower half switches from SW5 to SW8 of Limb-A for an output voltage level $V_{a0} = -V_{dc}/2$

Table 1: Switching states of five level diode clamped inverter for phase A

Switching States								Output voltage
SW1	*SW2*	*SW3*	*SW4*	*SW5*	*SW6*	*SW7*	*SW8*	
High	High	High	High	Low	Low	Low	Low	Vdc/2
Low	High	High	High	High	Low	Low	Low	Vdc/4
Low	Low	High	High	High	High	Low	Low	0
Low	Low	Low	High	High	High	High	Low	-Vdc/4
Low	Low	Low	Low	High	High	High	High	-Vdc/2

Seven level and nine level diode clamped inverters can also be presented in same manner as five level DCMLI

III. Alternative Phase Opposition Disposition SPWM Strategy

In APOD-SPWM technique the carrier signal of same amplitude are phase displaced from each other by 180° from its neighboring carrier signals, This carriers are compared with sinusoidal signal for producing pulse signals to trigger gates of switches used in DCMLI.For m-level output, (m-1) carrier signals are phase disposed by 180 degrees to its neighboring carrier waveform [9]. Fig. 6(a), 6(b), and 6(c) shows the carrier arrangement for APOD SPWM controlled 5, 7 and 9 level DCMLI respectively

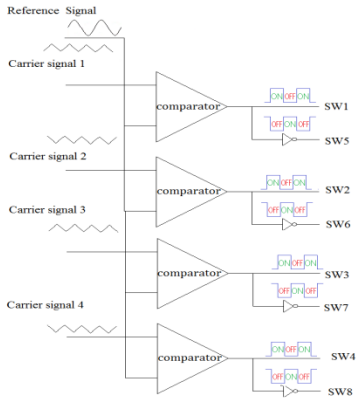

Fig. 5. APOD-SPWM technique for triggering switches of five level diode clamped inverter (Phase A)

The amplitude modulation index m_a and frequency ratio m_f are mathematically shown in equations (3) and (4) respectively.

$$m_a = \frac{A_m}{(m-1)A_{cr}} \tag{3}$$

Where A_m is peak to peak amplitude of reference waveform or modulating signal,A_{cr} is peak to peak amplitude of individual carrier frequency, m is output level of inverter.

$$m_f = \frac{f_{cr}}{f_m} \tag{4}$$

Where f_{cr} is frequency of carrier signal & f_m is frequency of modulating signal.

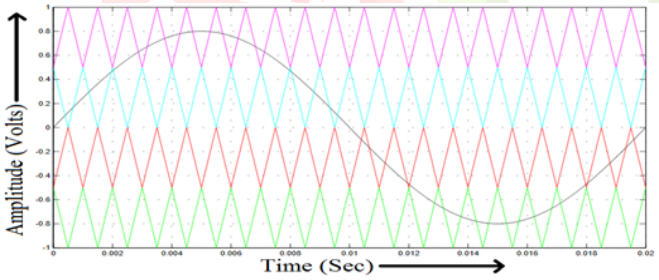

Fig. 6(a).Carrier arrangement for APOD SPWM controlled 5-level DCMLI ($m_a = 0.8$ and m_f=20).

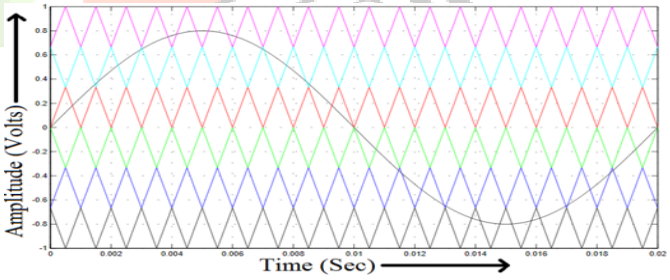

Fig. 6(b).Carrier arrangement for APOD SPWM controlled 7-level DCMLI ($m_a = 0.8$ and m_f=20).

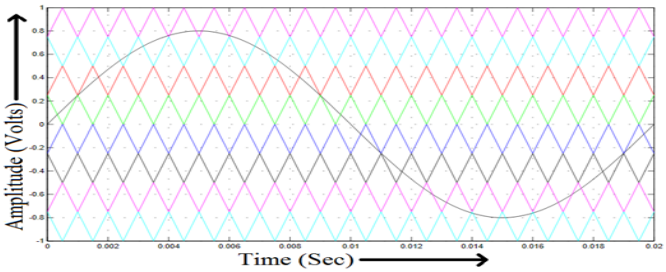

Fig. 6(c).Carrier arrangement for APOD SPWM controlled 9-level DCMLI ($m_a = 0.8$ and m_f=20).

IV. Simulation Results

The Simulation of APOD-SPWM controlled DCMLI for five, seven and nine level is carried out in Matlab/Simulink software. Figures 7(a), 7(b), 7(c), 7(d) presents phase voltage for 2-level, 5-level, 7-level, 9-level inverter respectively and figures 8(a), 8(b), 8(c), 8(d) presents line voltage without filter for 2-level, 5-level, 7-level, 9-level inverter respectively.

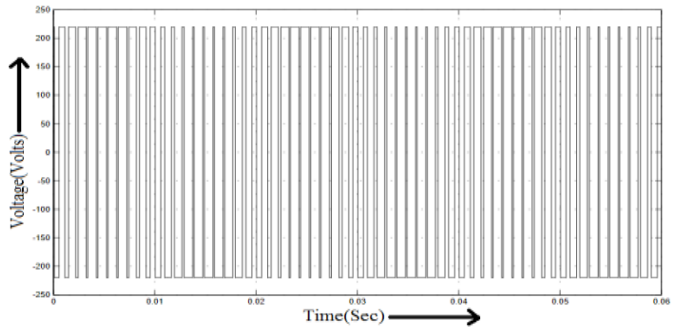

Fig. 7(a).2- Level Inverter Phase voltage

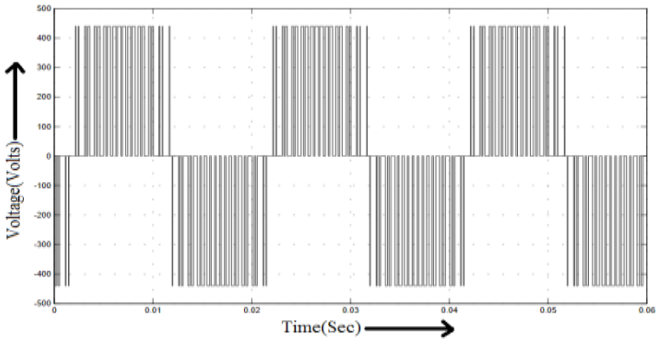

Fig. 8(a).2- Level Inverter line voltage without filter

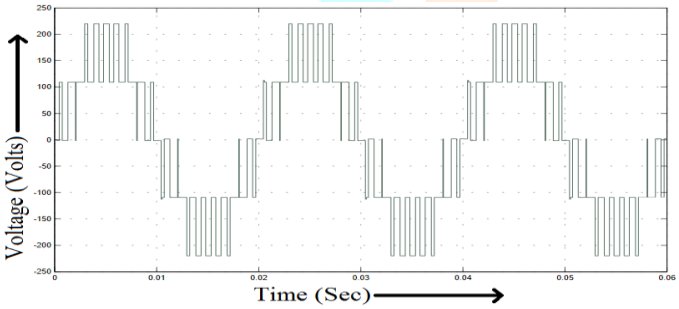

Fig. 7(b).5- Level DCMLI Phase Voltage

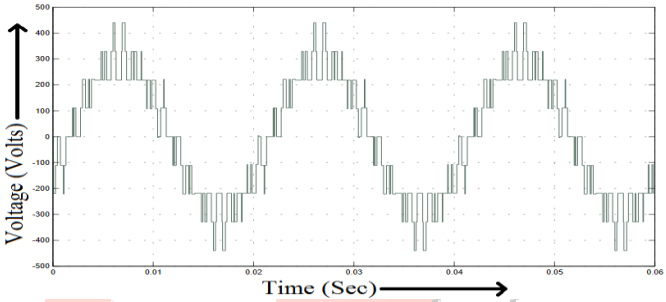

Fig. 8(b).5- Level Inverter line voltage without filter

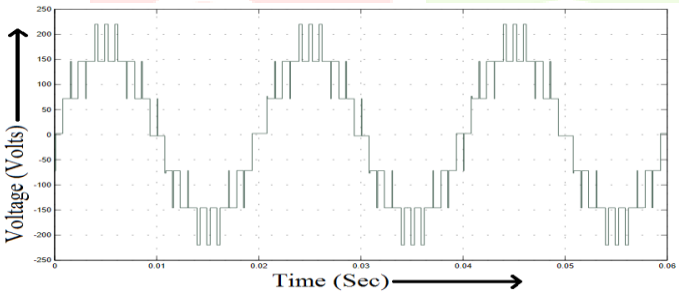

Fig.7 (c).7-Level DCMLI Phase Voltage

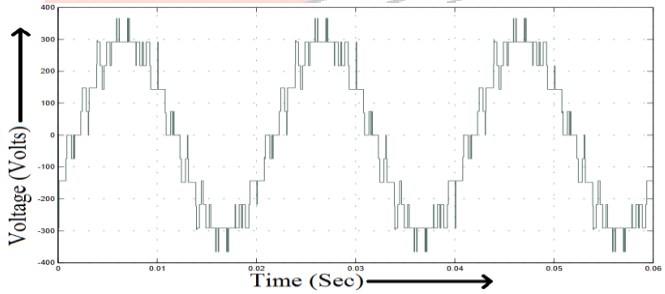

Fig. 8(c).7- Level Inverter line voltage without filter

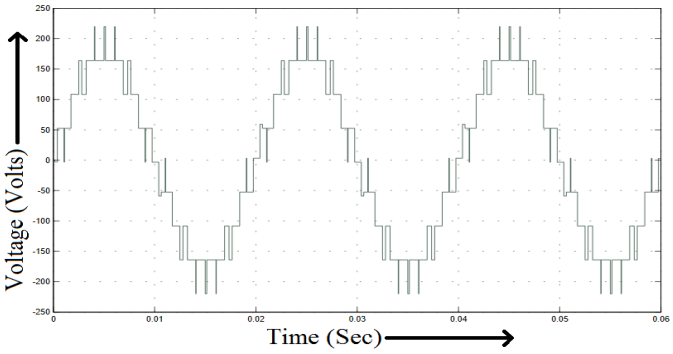

Fig. 7(d).9- Level DCMLI Phase Voltage

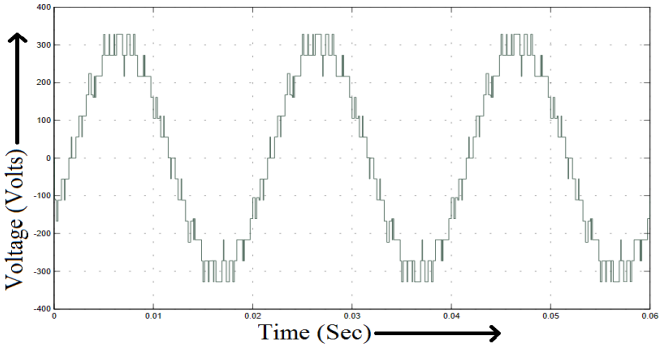

Fig. 8(d).9- Level Inverter line voltage without filter

Figures 9(a), 9(b), 9(c), 9(d) presents line voltage with filter for 2-level, 5-level, 7-level, 9-level inverter respectively and figure 10(a), 10(b), 10(c), 10(d) presents CMV waveform for 2-level, 5-level, 7-level, 9-level inverter respectively.

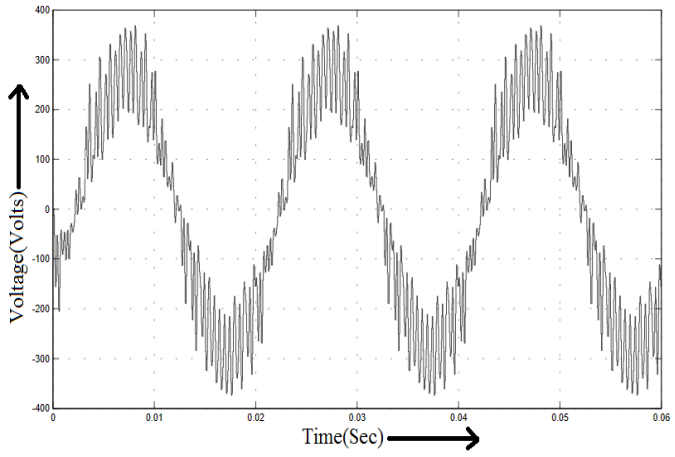

Fig. 9(a).2- Level Inverter line with LC filter

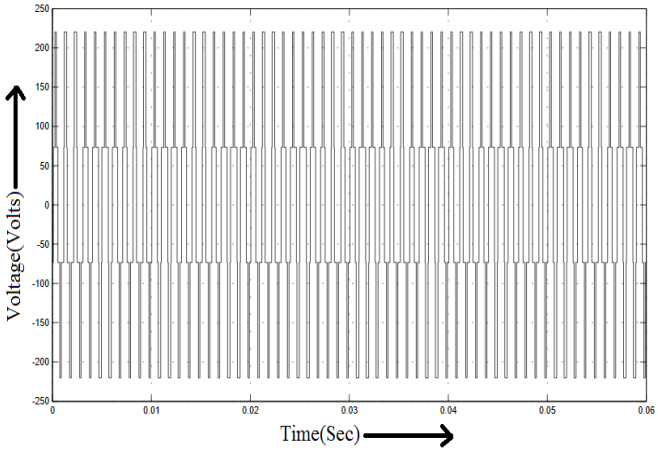

Fig. 10(a).2- Level Inverter CMV waveform

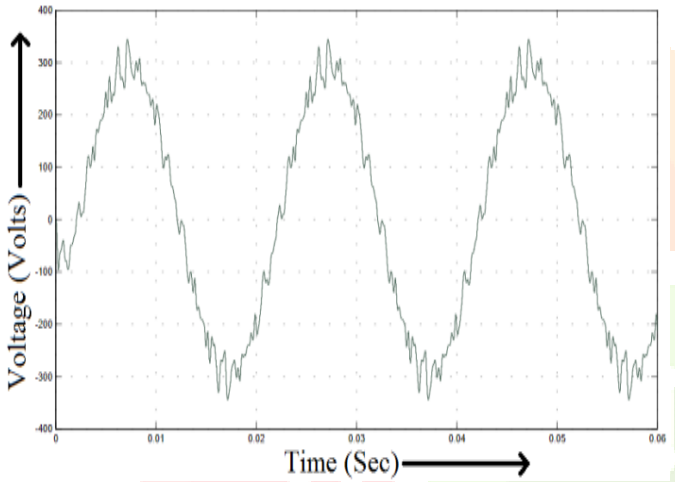

Fig. 9(b).5- Level Inverter line voltage with LC filter

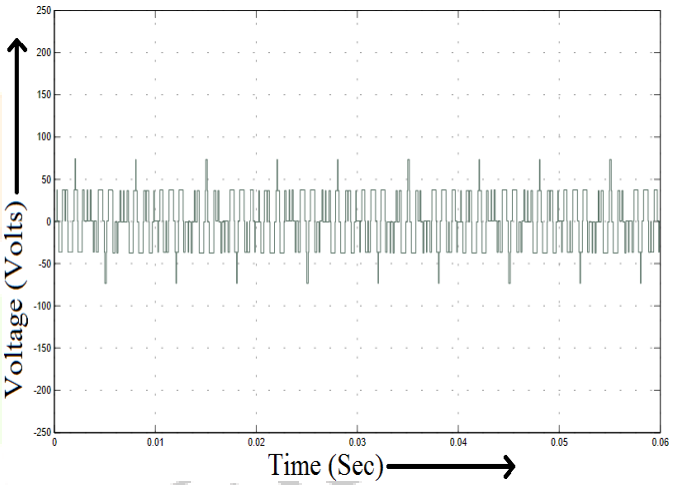

Fig. 10(b).5- Level DCMLI CMV Waveform

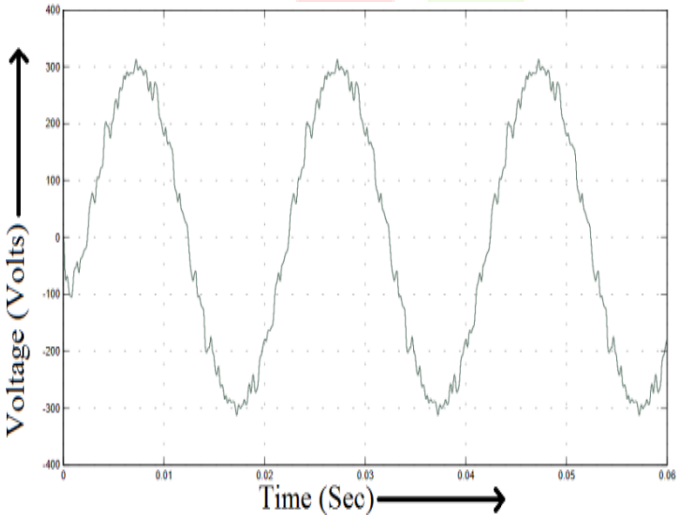

Fig. 9(c).7- Level Inverter line voltage with LC filter

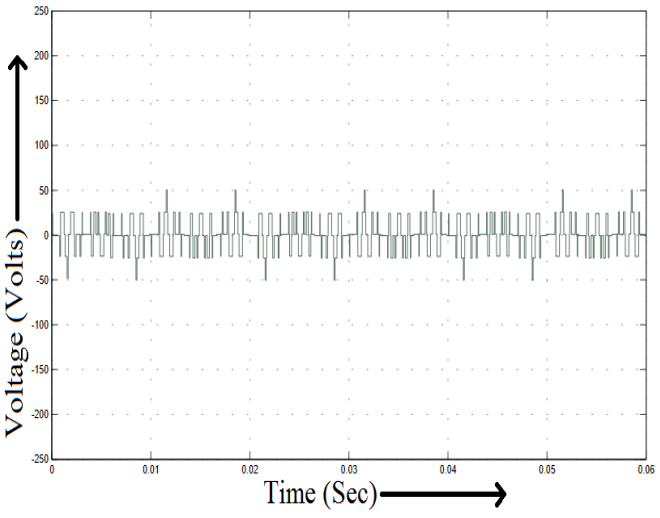

Fig. 10(c).7-Level DCMLI CMV Waveform

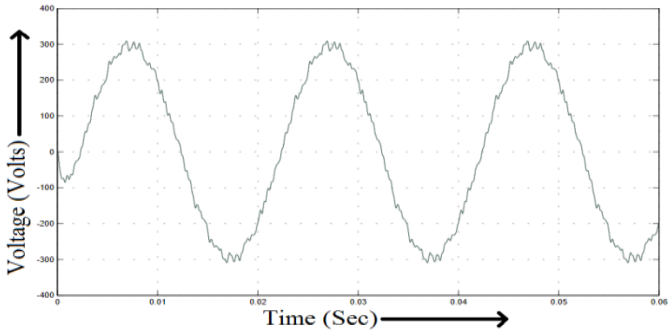

Fig. 9(d).9- Level Inverter line voltage with LC filter

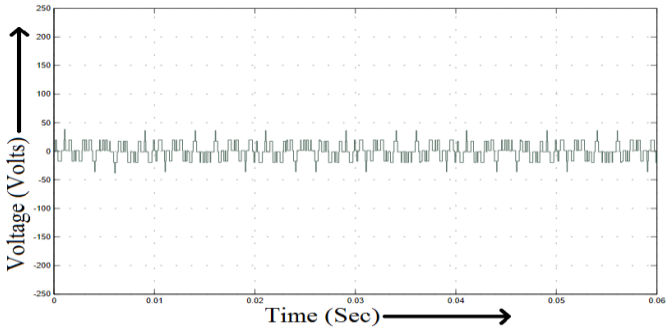

Fig. 10(d).9-Level DCMLI CMV waveform

Figure 11(a), 11(b), 11(c), 11(d) presents THD analysis without filter for 2-level, 5-level, 7-level, 9-level inverter respectively and figure 11(e), 11(f), 11(g), 11(h) presents THD analysis with LC filter for 2-level, 5-level, 7-level, 9-level inverter respectively.

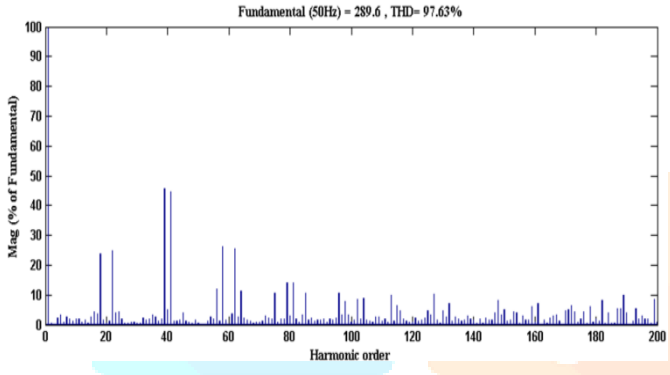

Fig. 11(a).Line voltage THD Analysis of 2-level inverter without filter

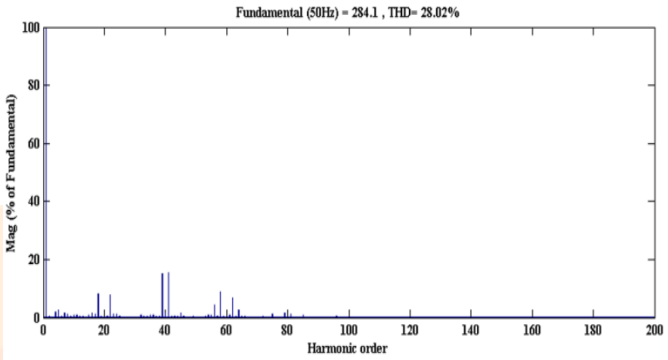

Fig. 11(e).Line voltage THD Analysis of 2-level inverter with filter

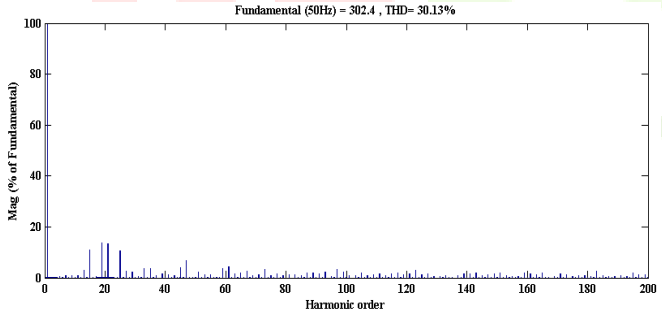

Fig. 11(b). Line voltage THD Analysis of 5-level inverter without filter

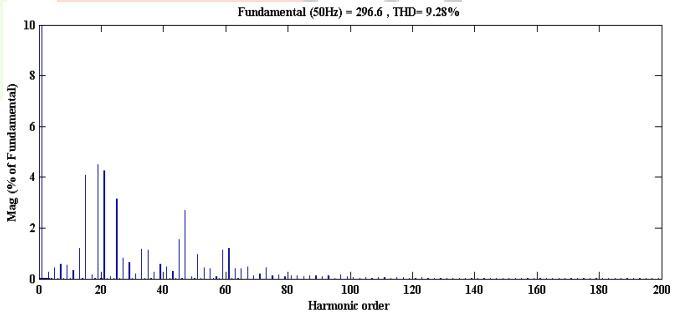

Fig. 11(f).Line voltage THD Analysis of 5-level inverter with filter

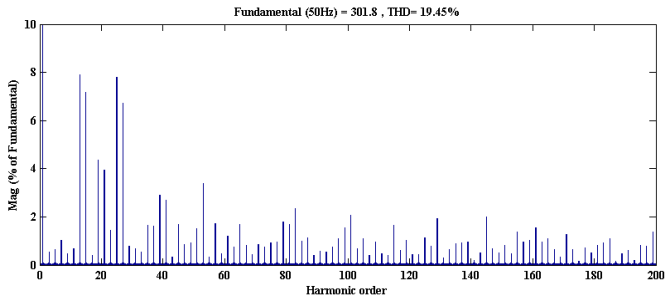

Fig. 11(c). Line voltage THD Analysis of 7-level inverter without filter

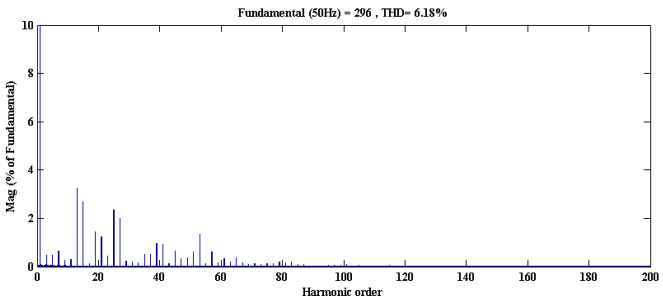

Fig. 11(g).Line voltage THD Analysis of 7-level inverter with filter

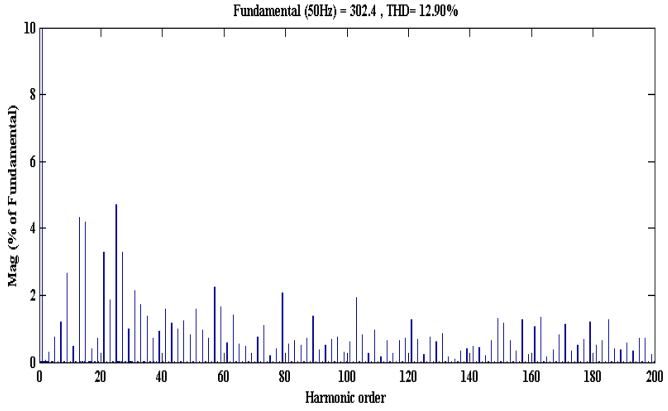

Fig. 11(d).Line voltage THD Analysis of 9-level inverter without filter

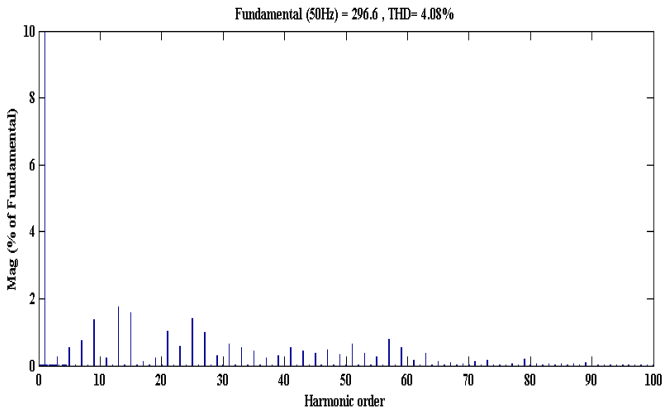

Fig. 11(h).Line voltage THD Analysis of 9-level inverter with filter

Table 2 shows the CMV and %THD for two level VSI, 5, 7 and 9 level Diode clamped Inverter using Alternative Phase Opposition Disposition SPWM technique with and without LC filter.

Table 2: CMV and %THD values for APOD SPWM controlled DCMLI

		2-level VSI	3-Phase APOD SPWM Controlled DCMLI		
			5-level	7-level	9-level
CMV (V)		145.2	31.14	17.44	14.09
THD (%)	Without filter	97.63	30.13	19.45	12.90
	With filter	28.02	9.28	6.18	4.08

Variation of CMV and % THD with level of Inverter is shown in fig. 12

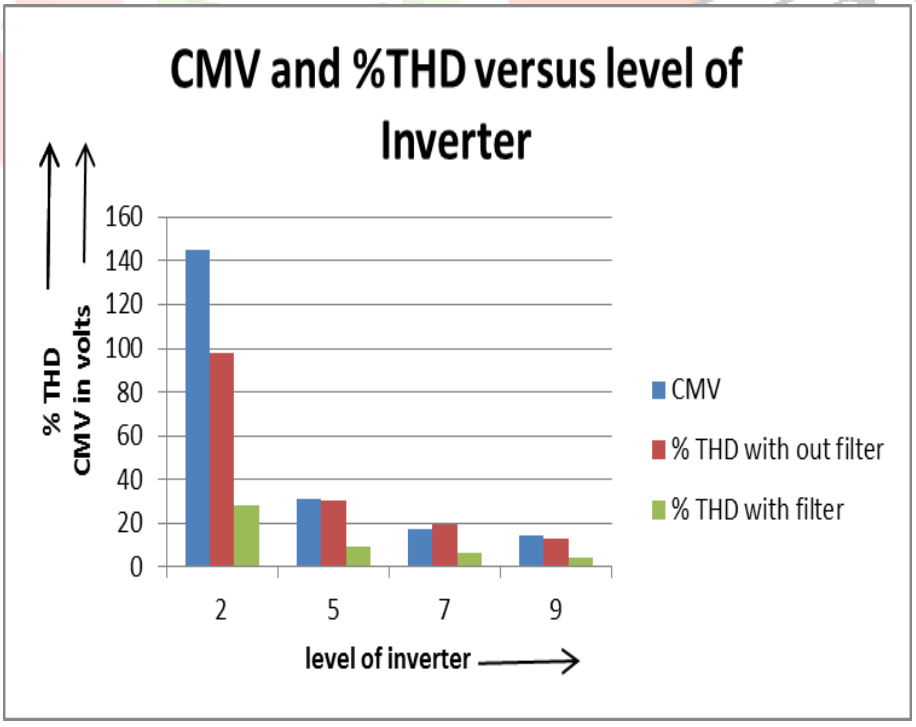

Fig.12.CMV and %THD versus level of Inverter

V.CONCLUSION

APOD SPWM controlled DCMLI for five, seven & nine level is simulated in Matlab/Simulink software. It is cleared from fig. 12 that CMV and %THD decreases with increase in level of the inverter. Increase in level improves the nature of output voltage waveform, approaching to sine shape which in turn lessens lower order harmonics. The number of steps in the output voltage increases as the level increases which reduces rate of rise of voltage.CMV and %THD reduces as size of step reduces.

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