Analysis of Double Tail Comparator with Low Power & High Speed Design

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Abstract : Comparators are most probably second most widely used electronic components after operational amplifiers in this world. Comparators are known as 1-bit analog-to digital converter and for that reason they are mostly used in large abundance in A/D converter. In the analog-to-digital conversion process, it is necessary to first sample the input. This sampled signal is then applied to a combination of comparators to determine the digital equivalent of the analog signal. The conversion speed of comparator is limited by the decision making response time of the comparator. Apart from that, comparators are also can be found in many other applications like zero-crossing detectors, peak detectors, switching power regulators, BLDC operating motors, data transmission, and others. The basic functionality of a CMOS comparator is used to find out whether a signal is greater or smaller than zero or to compare an input signal with a reference signal and outputs a binary signal based on comparison. Comparator is a circuit used to detect whether a signal is greater or smaller than zero, or to compare the size of one signal with another. Designing high-speed comparators is more challenging when the supply voltage is smaller. High-speed comparators in ultra-deep sub-micrometer (UDSM).CMOS technologies suffer from low supply voltages. In this paper we are going to study and analyze the dynamic double tail comparator and implement the same for high speed analysis and will observe the power consumption.

IndexTerms – CMOS, double tail comparator, Comparator

I. INTRODUCTION

The high speed, area efficient and low power analog to digital converter requires dynamic regenerative comparators to maximize speed and power efficiency. These dynamic comparators have no static power consumption. That means to minimize power consumption of dynamic comparator we need to reduce dynamic power of comparator. Dynamic power mainly dependent on supply voltage Vdd, transitions of the MOS due to clock and load capacitance, where capacitance is due to transistors and interconnects. The clock drives the comparator continuously whether the input is present or not. Thus when the comparator is in idle state, the clock drives the comparator continuously which causes switching of some of the MOSFET's. This causes more dynamic power dissipation. This problem can be overcome by using clock gating technique which disables clock at the idle states of comparator. The circuit may also suffer various types of process variation while fabrication or when subjected to various temperature and supply voltages. In such conditions the circuit must work properly, hence four corner analysis must be done before IC fabrication. By literature review, we find that there are various types of comparator architectures available in our today's electronic world. Among these comparators, we analyzed the static and dynamic characteristics & advantages and disadvantages of Preamplifier Based Comparator i.e. comparators having a preamplifier followed by a regenerative latch stage which is again followed by an output buffer (which is basically a self-biased differential amplifier) and fully dynamic latched comparators i.e. comparators having positive feedback based back-to-back latch stage that determines output of the circuit.

II. Comparator with a Modified Latch

The circuit is proposed with a new latch for low-supply-voltage operation, where the advantages of a high-impedance input, a rail-to-rail output swing, no static power consumption, and the indirect influence of the parasitic capacitances of the input transistors (larger gate area for lower offset) to the output nodes and, therefore, to the switching speed have been kept [2].

The circuit diagram for *proposed comparator with a modified latch is shown in figure 3·1·* A clock period is divided into two phases: The reset phase (CLK = 0) is used to establish the initial condition Out = Out_bar =VDD and the following comparison phase (CLK =VDD, VDD is the positive supply voltage of the comparator). During reset, transistor N6 is switched off, and transistors P2, P3, N4, and N5 are on. Consequently, the output nodes Out and Out_bar are pulled toward VDD by P2 and P3, which causes transistors P4 and P5 to be switched off. N4 and N5 pull both nodes FB and FB/ to GND. Hence, transistors P0 and P1 are turned on and help in pulling Out and Out_bar to the final voltage level VDD. Comparison of the voltage at input CINP with the voltage at CINN is started when CLK switches to voltage level VDD (comparison phase). Hence, transistor N6 is turned on, and P2, P3, N4, and N5 are switched off. At the very beginning, transistors P4 and P5 are switched off, and transistors P0 and P1 work in the linear region and build the load for an amplifier with N2 and N3. Transistors N0 and N1 are initially on. (The comparison phase starts

with Out = Out_bar =VDD and FB = FB/ =GND.) If, for the input voltage, CINP > CINN is assumed, transistor N3 pulls the voltage level at node Out_bar down faster than N2 does at node Out. Hence, transistor P4 begins to conduct. In this initial time period, a small amount of positive feedback is also contributed by transistors N0 and N1. When P4 begins to conduct, node FB is charged toward VDD (N4 and N5 are off), and complete positive feedback is started. Transistor P1 is turned off, and P0 keeps conducting, because node Out is pulled to VDD.

Thus, P5 remains off, and FB/ remains near GND (Sufficient input voltage difference CINP-CINN is assumed). Finally, N1, P4, and P0 are switched on, and N0, P1, and P5 are turned off. Thus, Out is at voltage level VDD, Out_bar is at GND, and no static current can flow after the decision.

III. Proposed Double-Tail Dynamic Comparator

In the proposed comparator the voltage difference at the first stage outputs (fn and fp) at initial time (i.e. ΔVfn/fp) is increased so as the latch regeneration speed should be increased [1]. This proposed dynamic comparator increases the speed of the double-tail comparator by altering two important factors like the first one is that it increases the initial output difference voltage (ΔV_0) at the starting of the regeneration ($t = t_0$); and the second one is that the effective transconductace (g_{meff}) of the latch is increased.

In the proposed double–tail dynamic comparator, only one node (fn or fp) gets charged during the reset phase. This happens because during the previous decision making phase, only one of the nodes (fn or fp) was not discharged and thus less power is required. The operation of the proposed comparator shown in figure 3.5 isas follows. When CLK = 0, in the reset phase, both the tail transistors Ntail1 and Ntail2 are in off to avoid static power dissipation. Transistor N3 and N4 are in on state. N3 and N4 pulls both fn and fp nodes to VDD, hence transistor NC1 andNC2 are cut off. The circuit has two intermediate stage transistors NR1 and NR2. These transistors reset both latch outputs to ground. When CLK = VDD, both the tail transistors are on, N3 and N4 transistors are off. Suppose InP > InN, thusfn drops faster than fp, the corresponding PMOS control transistor (NC1 in this case) starts to turn on, pulling fp node back to the VDD, so another control transistor remains off, allowing fn to be discharged completely.

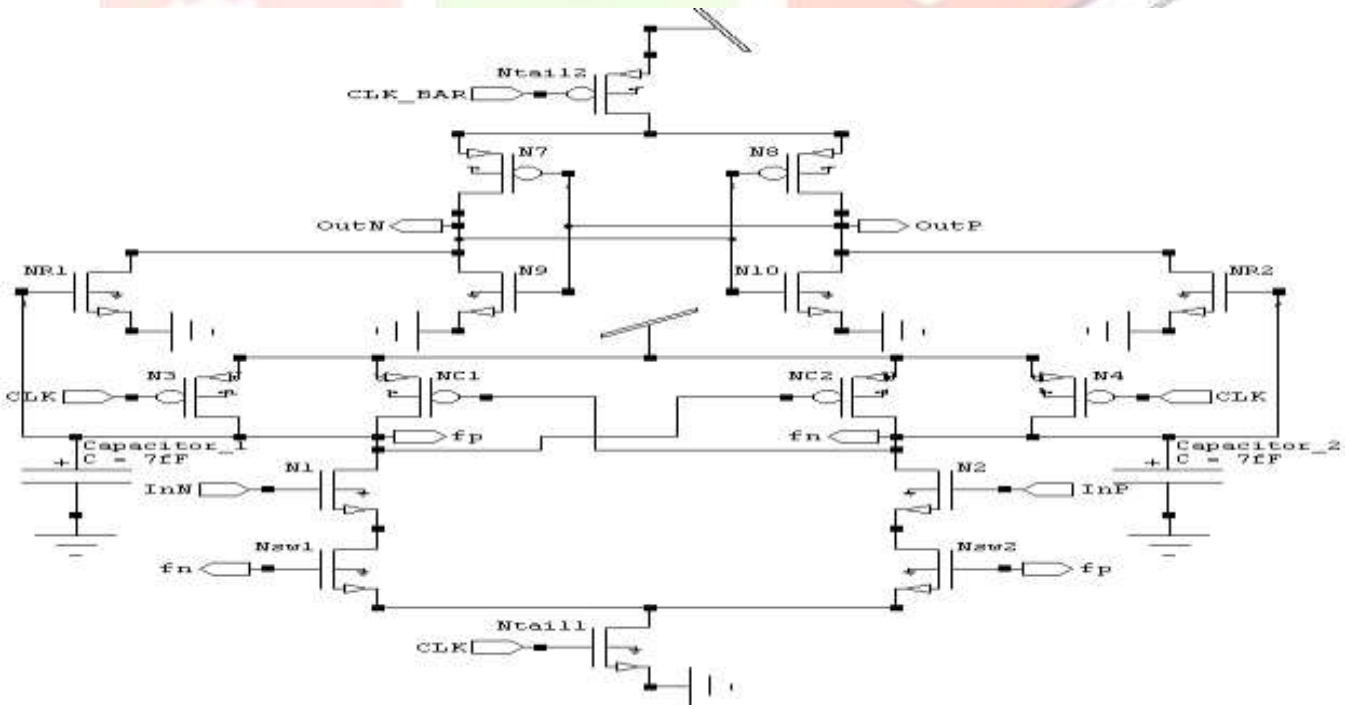

Figure 3.1: Schematic diagram of the proposed dynamic double-tail comparator

IV. RESULTS AND DISCUSSION

Previous Methodology Result

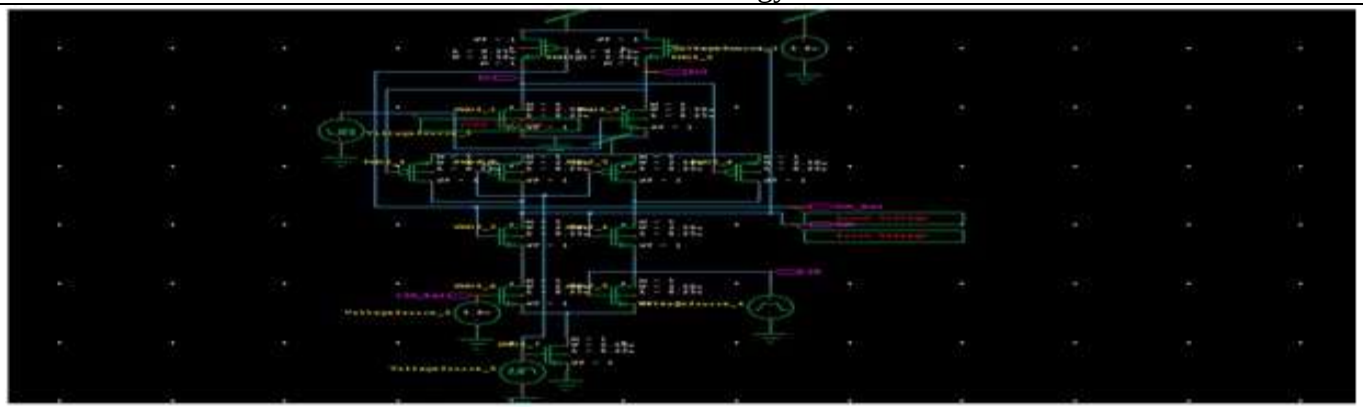

Fig:- 5.1 Comparator with a modified latch

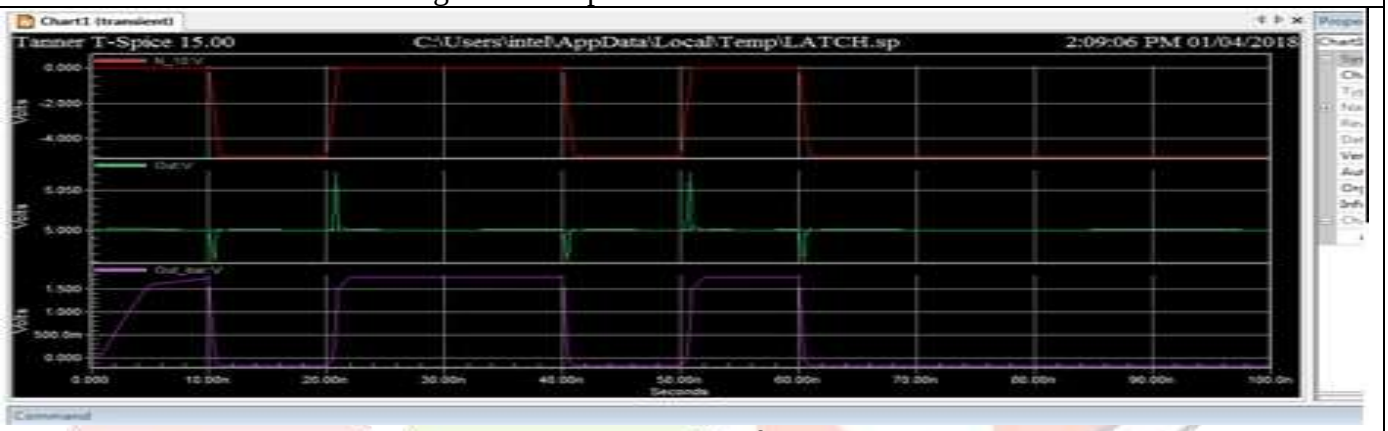

Fig:- 5.2 Wave form

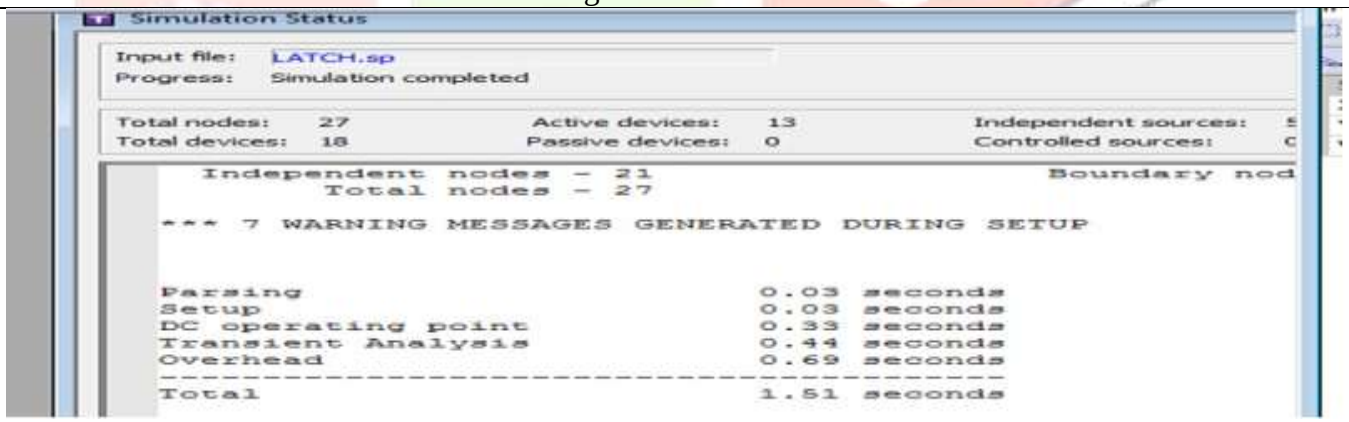

Fig:- 5.3 Time analysis

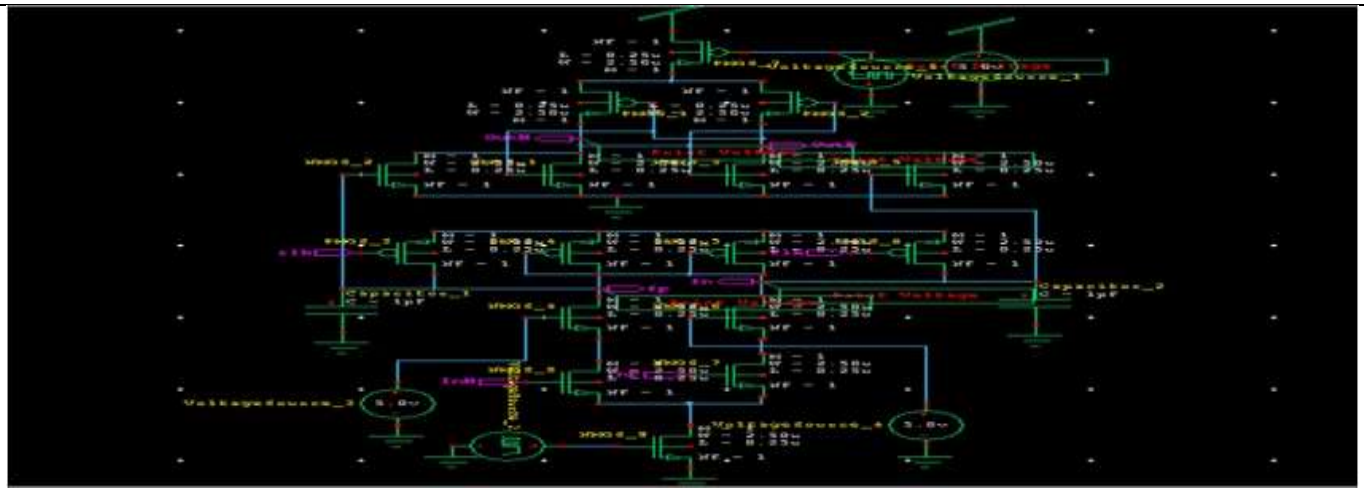

Fig:- 5.4 Proposed Double-Tail dynamic Comparator

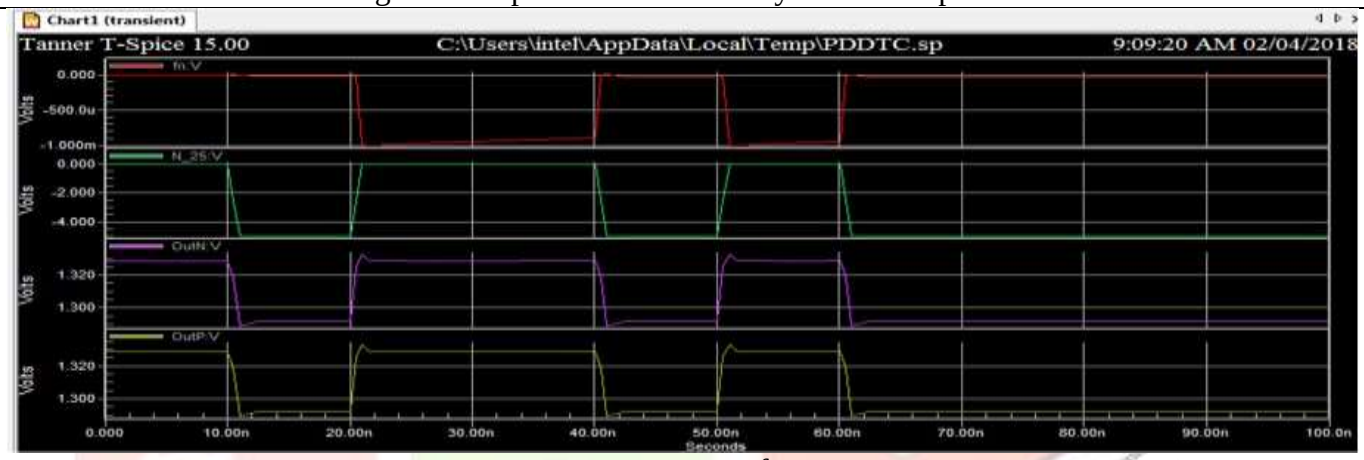

Fig:- 5.5 Wave form

Fig:- 5.6 Time analysis

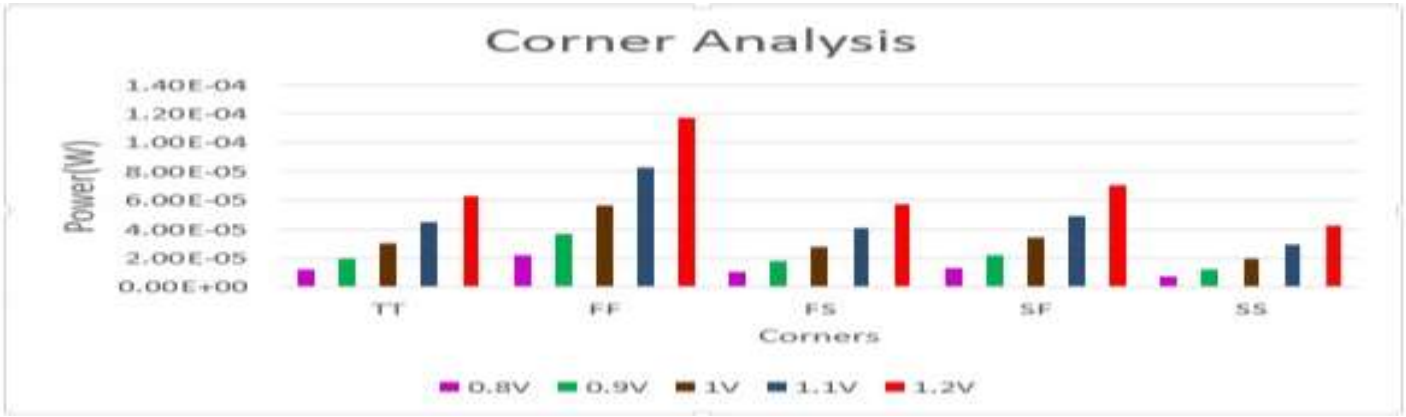

Figure 5.7 shows the power variation along with different process variation at different supply voltages of the dynamic double-tail comparator circuit

V. Conclusion:

A new dynamic comparator using positive feedback which shows better noise response, lower dynamic power dissipation than the double-tail comparator and proposed double tail comparator has been proposed & can be targeted for ADC application. The transistor count in the modified comparator is higher to an extent among all the comparators analyzed. The performance of the modified clock gated comparator, the double tail comparator and proposed double tail comparator comparators have been compared. The pre-layout simulation using 0.18 µm technology shows that the dynamic power for the modified clock gated comparator has been reduced significantly by using gating technology. The corner analysis at different corner specifies that the circuit may fail at certain process corners which requires some modification in MOSFET's parameters.

VI. Future scope and applications

From simulation results, we can see that power dissipation is reduced by more than half and speed is also maintained as compared to the previous design, then the optimization in the circuit as well as the layout of the proposed comparator with some other technologies with reduced transistor feature size and with some other different parameters can be one topic. Furthermore by knowing the unused states of comparator we can reduce the dynamic power profoundly which can be another topic. Offset voltage optimization can be another topic of interest.

Clocked regenerative comparator provides fast decision by means of using strong positive feedback in latch therefore it is most widely used in high speed ADC. The conversion speed of comparator is limited by the decision making response time of the comparator. Therefore for low power, high speed and area efficient analog-to digital converter dynamic regenerative comparators are used. Apart from that, comparators are also can be found in many other applications like zero-crossing detectors, peak detectors, switching power regulators, BLDC operating motors, data transmission, and others.

VII. References

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