

COMPARISON OF THD REDUCTION FOR ASYMMETRICAL CASCADED H-BRIDGE INVERTER

¹G. Jegadeeswari, ² Dr. Saravanan. S.V

¹Assistant Professor, ²Assistant Professor

Department of Electrical & Electronics Engineering

¹AMET Deemed to be University, Chennai, India

Abstract:

This paper proposes the performance of single phase seven, nine and fifteen level asymmetrical H-bridge multilevel inverter. Sinusoidal pulse width modulation technique is used for pulse generation. By comparing reference and carrier signal, we can generate the SPWM for H-bridge inverter. This proposed inverter widely used in industrial applications such as speed control of induction motor, brushless dc motor etc. This switching scheme reduces the total harmonic distortion, switching losses and increases the output level. FFT analysis and output result of inverter with R-load is discussed in this paper.

Keywords: Multilevel inverter, THD, cascaded H-bridge inverter, R-load, simulation results.

1. INTRODUCTION

Multilevel inverter is used to convert uncontrolled D.C to controlled A.C. In recent years, asymmetric multilevel inverters have received increasing attention because it is possible to synthesize voltage waveforms with reduced harmonic content, even using a few series- connected cells. In this paper seven, nine, fifteen level inverter with it results has been discussed. For pulse generation sinusoidal pulse width modulation technique is used. This technique is most widely used in industrial application. FFT is used to determine the harmonic analysis for seven, nine and fifteen level inverter.

The paper can be ordered as follows: Section 2 explains the proposed cascaded H-bridge inverter. Section 3 discusses the modulation techniques. Section 4 explains the circuit model of single phase seven level, nine levels and fifteen level inverter. Section 5 discusses the simulation results. In section 6 discusses the comparison of total harmonic distortion for all three types of inverter.

2. PROPOSED CASCADED H-BRIDGE INVERTER

Multilevel inverter owns a separate DC source to form a single phase full bridge or H-bridge inverter. By different combination of four switches S1, S2, S3 and S4, it can generate the three-different output voltage +Vdc, 0, -Vdc.

The switches S1 and S4 turned on to obtain a +Vdc, for -Vdc the switches S2 and S3 gets turn on. The output voltage is 0 when the switches S1 and S4 or S2 and S3 are turn on. Here, the final output voltage levels becomes the sum of each terminal voltage of H-bridge, and it is given as

$$V_{out} = V_{HB1} + V_{HB2} \quad (1)$$

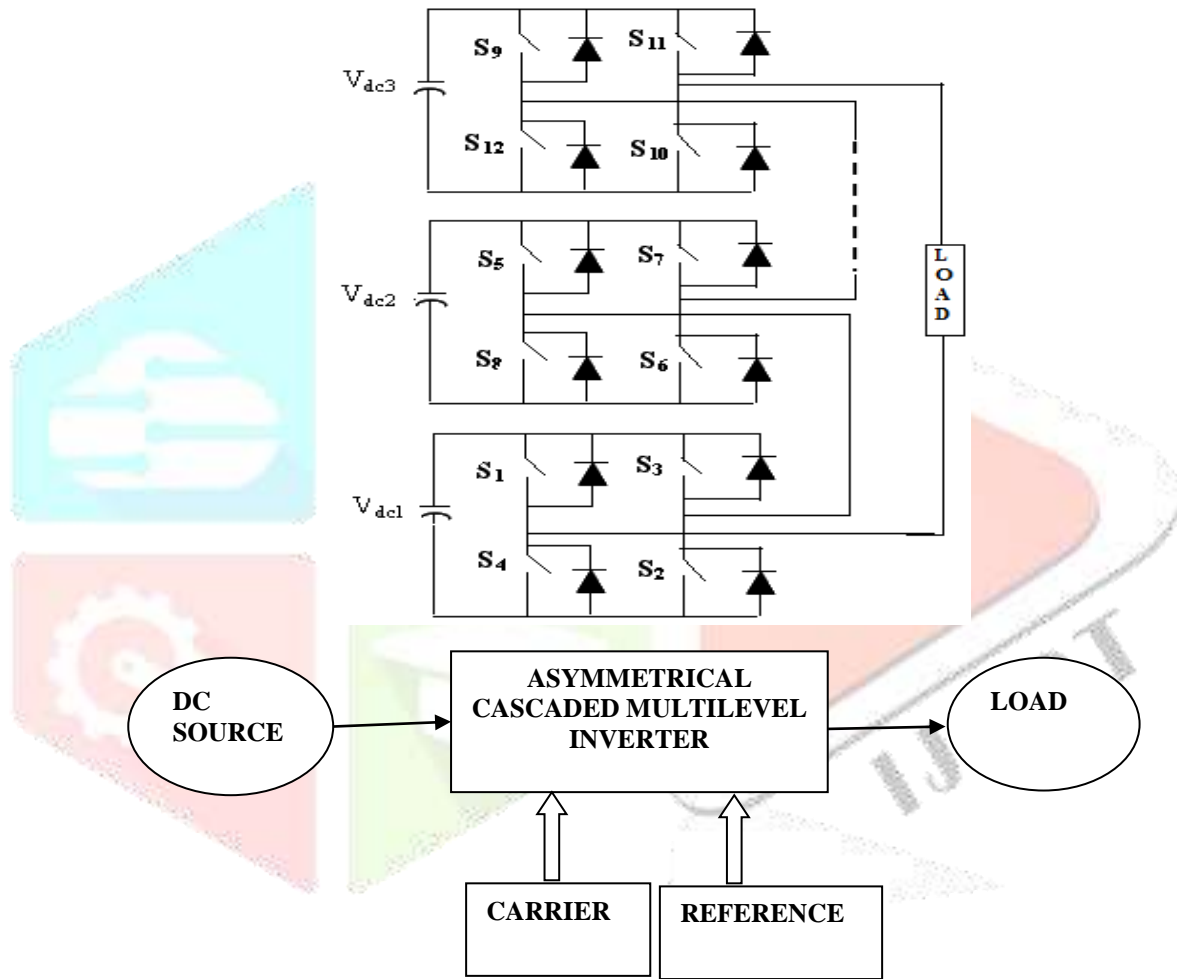


Fig -1: Block Diagram of Proposed System

Fig -2: General Circuit for H-Bridge Inverter

3. MODULATION TECHNIQUES

Single pulse width modulation is an easy technique for reduction of harmonics. In this technique sine wave is compared with triangular wave and finally it produces gate pulses. SPWM is one of the modern techniques, used to suppress harmonics presented in the quasi-square wave.

3.1 Modulation Index

Modulation index can be classified into two types

- Amplitude modulation index
- Frequency modulation index

3.2 Amplitude Modulation Index

The Amplitude modulation index (m_a) can be given by the amplitude of carrier signal and the reference signal used can be defined as,

$$M_a = A_c / A_r \tag{2}$$

Where,

A_r = Amplitude of reference signal

A_c = Amplitude of carrier signal

3.3 Frequency Modulation Index

The modulation index depends on the frequency of the reference signal and the carrier signal used. The frequency modulation index can be expressed as

$$M_f = f_c / f_r$$

(3)

Where,

f_c = carrier signal frequency

f_r = reference signal frequency

4. CIRCUIT DIAGRAM FOR PROPOSED INVERTER

Circuit diagram of Asymmetrical H-bridge multilevel inverter employing Binary DC input source shown in fig 3. By using V_{dc} , $2V_{dc}$, it can synthesize seven output levels; 0, V_{dc} , $2V_{dc}$, $3V_{dc}$, $-V_{dc}$, $-2V_{dc}$, $-3V_{dc}$.

In the proposed circuit topology, if n is number of H-bridge module has independent DC sources in sequence of the power of 2 an expected output voltage level is given as

$$V_n = 2^n, n = 1, 2, 3 \tag{4}$$

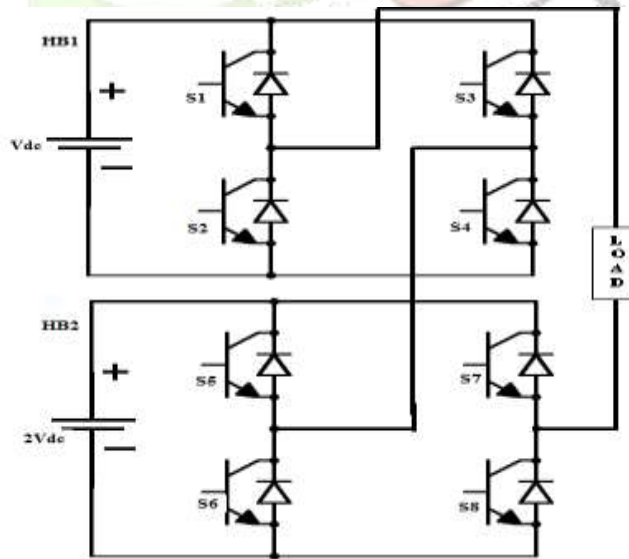


Fig -3: Circuit diagram for seven level inverter

Fig 3. Shows Trinary DC source H-bridge inverter by using V_{dc} , $3V_{dc}$. it can synthesize nine output levels; 0, V_{dc} , $2V_{dc}$, $3V_{dc}$, $4V_{dc}$, $-V_{dc}$, V_{dc} , $2V_{dc}$, $-3V_{dc}$, $-4V_{dc}$. In the nine levels proposed topology, the number of H-bridge module is denoted as n , and

it has independent DC sources in sequence of the power of 3 an expected output voltage level is given as

$$V_n = 3^n, n = 1, 2, 3 \tag{5}$$

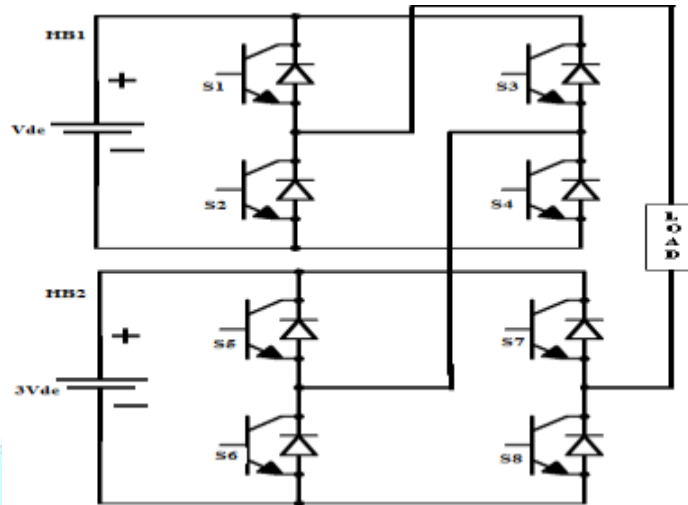
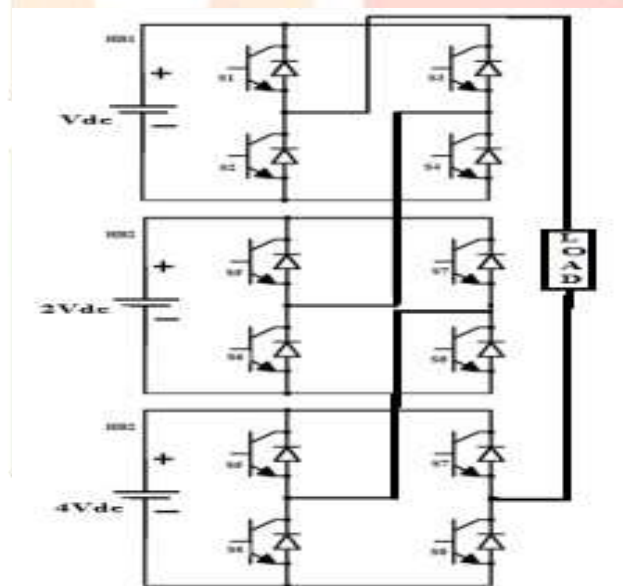


Fig- 4 : Circuit diagram for nine level inverter

In fifteen levels proposed topology, is shown in fig 4. It can synthesis fifteen output level 0, Vdc ,2Vdc , 3Vdc , 4Vdc , 5Vdc , 6Vdc



,7Vdc , -Vdc , -2Vdc , -3Vdc , -4Vdc , -5Vdc , -6Vdc , -7Vdc. In fifteen level inverter the H-bridge module is denoted as n, it has independent DC source in sequence of power 2 and the estimated output voltage level is given as, $V_n = 2^n, n=1, 2, 3$

Fig- 5: Circuit diagram for fifteen level inverter

5. SIMULATION RESULTS

In this paper, the simulation model of proposed H-bridge inverter is shown in below figures. The simulation model is done by using MATLAB / SIMULINK. The analyses of total harmonic distortion for proposed Simulink are given below:

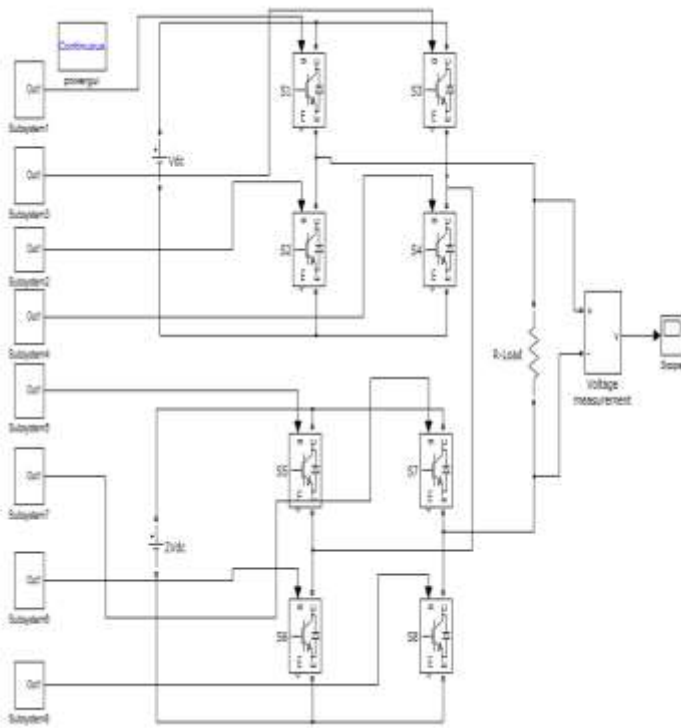


Fig-6: Proposed asymmetrical seven level Simulink model

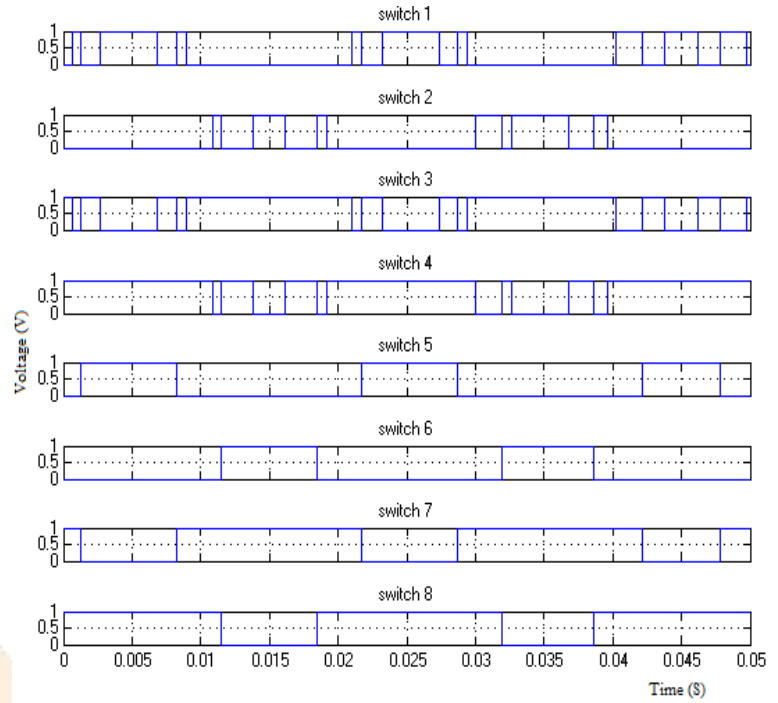


Fig -7: Pulse pattern for seven level inverter

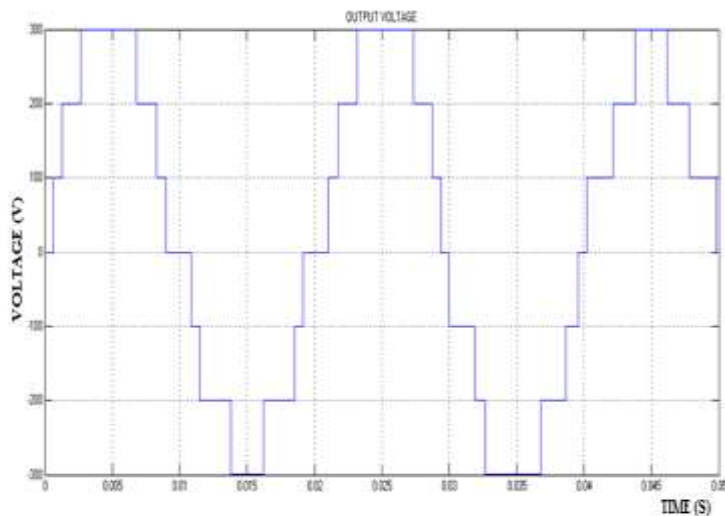


Fig -8: Output voltage waveform

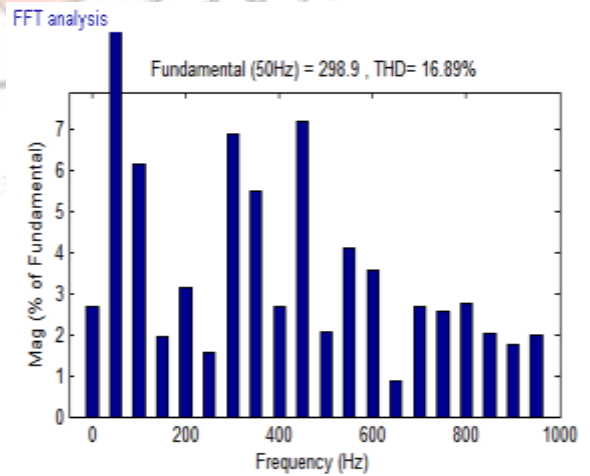


Fig -9: FFT Analysis

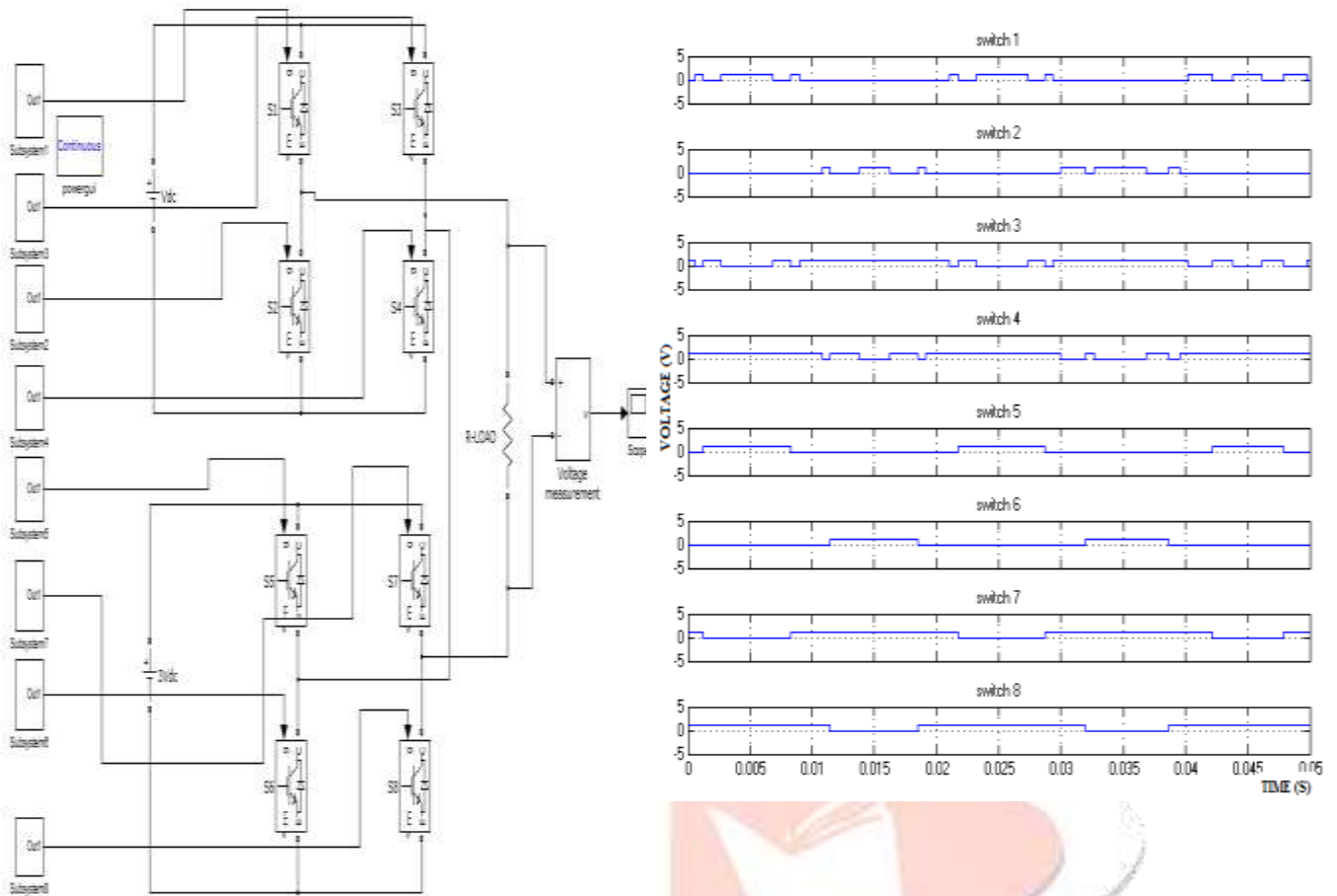


Fig -11: Nine level inverter pulse pattern

Fig -10: Simulink model for asymmetrical nine level inverter

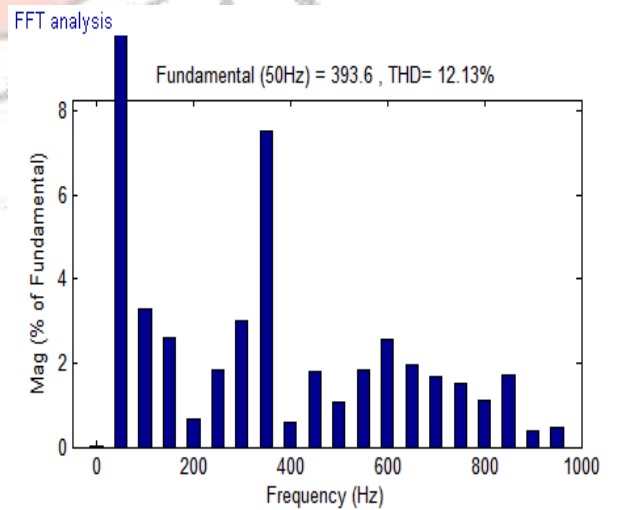
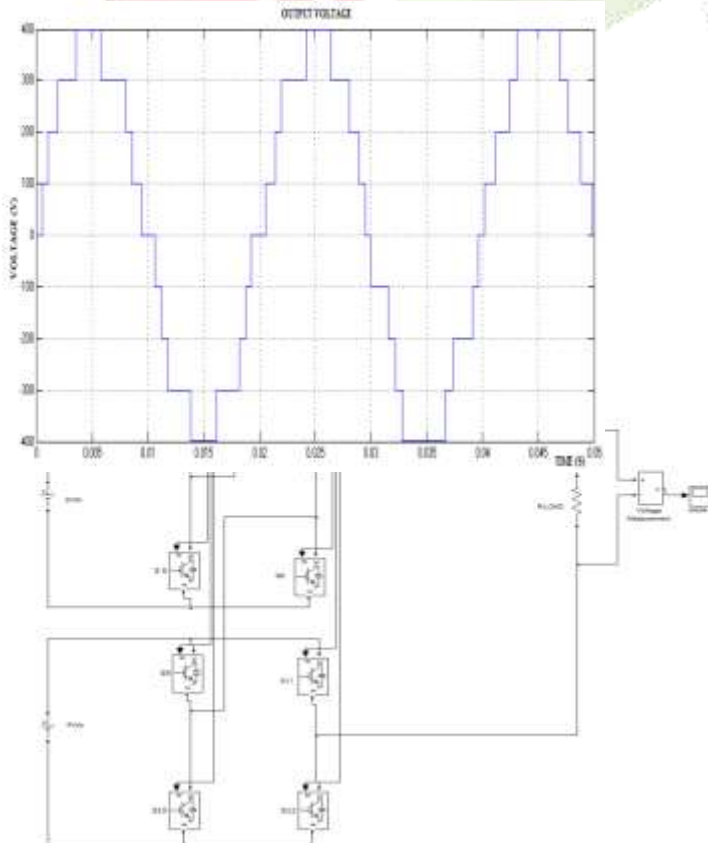


Fig -12 : Output voltage waveform

Fig -13: FFT analysis

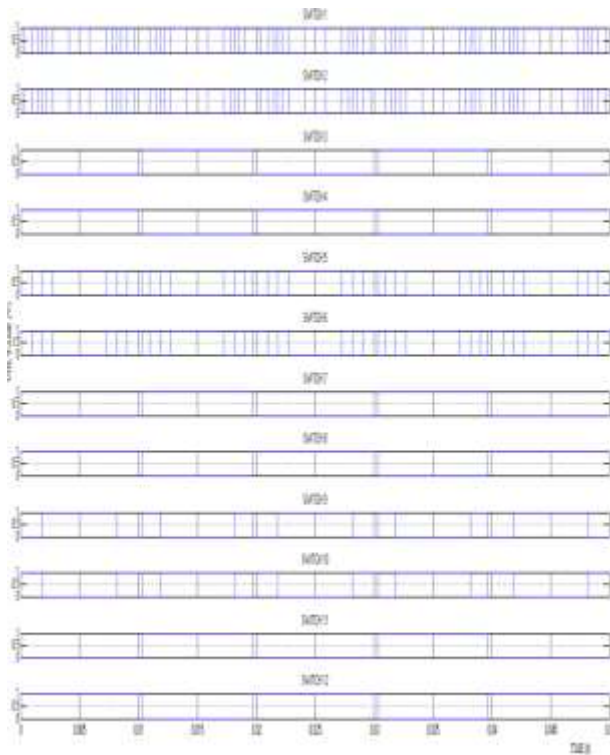


Fig -14: simulink model for Fifteen level inverter



g -15: Fifteen level pulse pattern

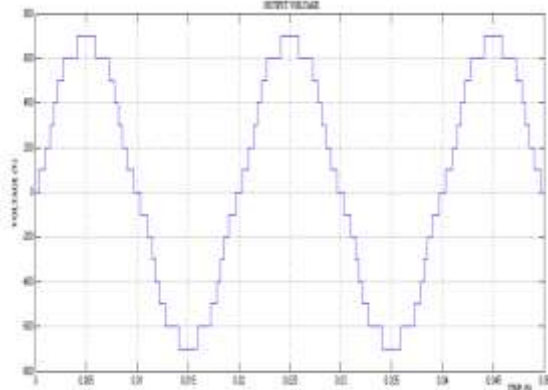


Fig -16: Output voltage waveform

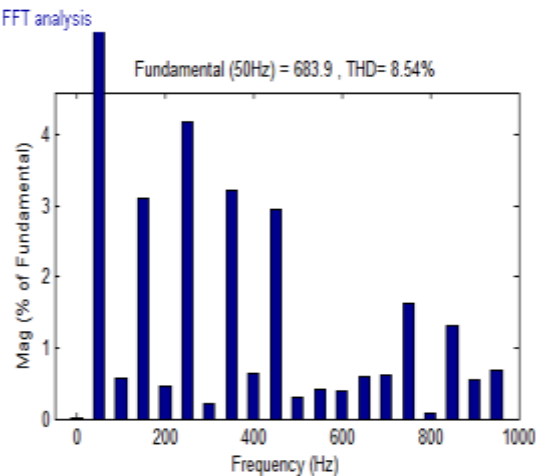


Fig -17: FFT analysis

6. COMPARITIVE ANALYSIS

S.NO	NO. OF LEVELS	THD (%)
1.	7-LEVEL	16.89
2.	9-LEVEL	12.13
3.	15-LEVEL	8.54

From above comparative analysis, we can note that fifteen level inverter has low total harmonic distortion compare to seven and nine level.

7. CONCLUSIONS

In proposed work, the performance of asymmetrical cascaded H-bridge seven level, nine level and fifteen level inverters with R-load by using sinusoidal pulse width modulation technique has been analyzed by MATLAB / SIMULINK. From above comparative table, the fifteen-level inverter has **8.54** low total harmonic distortion compared to seven level and nine level inverters. To improve the efficiency of the system, by implementing closed loop control for better performance in future work.

REFERENCES

- [1]. P.Manikandan G.Uma Devi A.Thimo theu, S. Prabakaran, "Implementation of multilevel inverter using sinusoidal pulse width modulation technique", ISSN: 2278 – 7798, International Journal of Science, Engineering and Technology Research (IJSETR), Volume 2, Issue 7, July 2013
- [2]. K.pradeep, G. Laxminarayana, "Comparative Analysis of 3-, 5- and 7-Level Inverter Using Space Vector PWM" ISSN 2278 – 8875, International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, Vol. 2, Issue 7, July 2013
- [3]. Dr.P.Melba Mary, N.K.Jawahar Muthu, M.S.Sivagamasundari,"Comparative Analysis of THD in Symmetrical and Asymmetrical Cascaded H-Bridge Seven Level Inverter", ISSN 2278 – 8875, International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, Vol. 3, Issue 3, March 2014.
- [4]. Bharath. K, R.J.Satputaley," Single Phase Asymmetrical Cascaded Multilevel Inverter Design For Induction Motor" International Journal Of Electrical, Electronics and Data Communication, ISSN: 2320-2084, Volume:1, Issue:3.
- [5]. R.Bharath, V.Arun, "9-Level Trinary DC Source Inverter Using Embedded Controller" IOSR Journal of Engineering (IOSRJEN) Volume 2, Issue: 10, October 2012,pp 90-95.
- [6]. Zhong Du, LeonM.Tolbert, JohnN.Chiasson and Burak Ozpineci, "A Cascaded Multilevel Inverter Using a Single DC Source" 2006 IEEE.
- [7]. G.Murali Krishna, V.V.N.Murthy, K.Lakshmi Ganesh, "THD Analysis Of Symmetrical and Asymmetrical Cascaded H-bridge Multilevel inverters with PV Arrays "et al./IJAIR
- [8]. Muhammad H.Rashid, Power Electronics Circuits, Devices and Applications, Prentice Hall, 2nd Ed.
- [9]. FangZheng Peng, Jih-Sheng Lai, And Rodriguez Multilevel inverter: A Survey of topologies, controls and applications, Industrial Electronics, IEEE Transactions, Volume:49, issue:4 :4.pp 724-738, Aug 2002.
- [10]. S. Sivasankari, C. R. Balamurugan,"Fifteen Level Cascaded Multilevel Inverter Using Embedded Controller " International Journal of Information Science and Intelligent System, 3(1): 1-7, 2014