IMPLEMENTATION AND CHARACTERIZATION OF MODULAR RESIDUE REVERSE CONVERTERS BY SELF- SELECTION OF MODIFIED CARRY USING FPGA

A.Mounika[1], Dr. S.V.Jagadeesh Chandra[2], [3]K. Rani Rudrama
[1]P.G Student, [2]Professor in LBRCE, [3]Asst. Professor in LBRCE
[1]Department for Electronics and communication Engineering
[1]Lakireddy Balireddy college of engineering, Vijayawada, India.

Abstract : In this approach, the selection of carrying free operation takes place in modulo residue converters. The residues are used to calculate the results of given arithmetic functions. An arithmetic unit is a special unit used to calculate any type of calculation in VLSI circuits. In modern technology, the size of VLSI chip is decreased for every one-and-half years. The performance of VLSI increases in terms of the area, and power consumption. The existing design contains reverse residue converters using prefix operator used to reduce delay requirements, the drawbacks in this design is power consumption increases and area increases due to its critical path. This project deals with residue converters by further enhancement a self-selection of modified carry is used. The implementation can take place using FPGA to reduce area and power concerns.

Index Terms - Residue reverse converters, modified CSLA, BEC converters, modified residue prefix operation.

I. INTRODUCTION

In recent years, many industries, and other technologies acquire better design to develop their quality of the work by adding extra features and modify their design to make better performance in IC Chip. The size of VLSI chip is decreased for every 18 months According to Moore's law. By changing the chip size, the number transistor spacing is going to be decreased. The change of the features will fasten the execution speed and provide better trade-off to their speed, area, power. Large integration of IC takes place by integrating all active and passive elements in a single chip. The size of the chip going to be decreased by using suitable methods of using recent technology. An Adder is a common basic component of any integrated designs. There are different types of adders' operations takes place to perform the addition, subtraction and for other operations performed logically. Many advanced technologies are held in many industries to perform takes for recent use. Many companies take it a challenging task to make a new design to reduce their size and increase their performance to provide a better trade-off between area and power. Residue converter is a design used only for the converting conventional data to the binary form. The main task of it for many applications like; fault tolerance, error correction, and detection, and for preprocessing of the image. The main approach in this is to reduce [1], the slow operation and increase computation speed. Parallel prefix adder operation is to secure the data a better way and adds easy methods for faster computation speed and make approximate result values and make the performance check. The increase the wider chain leads complex of design. So, the selection of modified carry operation takes place to reduce the carry waiting time and make a simple design for calculating area and power.

II. TYPES OF RESIDUE CONVENTIONAL ADDER

The Numbering Systems uses both forward and reverse converters to form small integers to make large integers representation. the below figure shows the block diagram for residue converters ;

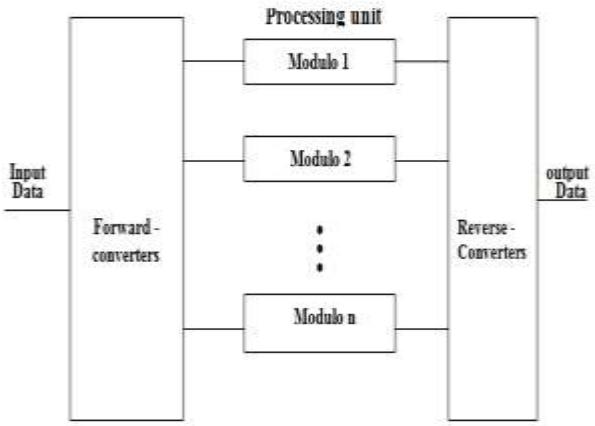

fig: Residue Number System

In the field of digital arithmetic computing, RNS can place an important role. These conversion systems can complete their entire operation using a finite set of modular addition. Modular arithmetic's can done to produce a small set of residues to form large unique integer sets .The below figure shows the best choosing of selecting an appropriate value among a finite number of small integer values using multiplexer;

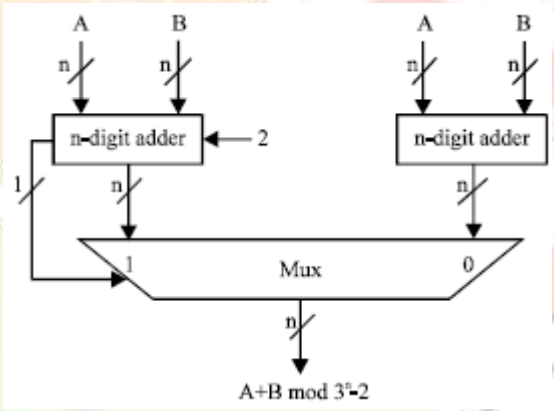

Fig: Modular residue operation

III EASE OF USE

The selection of modified carry operation takes place by using BEC Converters for entire design in place of RCA Adders. The main purpose of BEC Adders is willing to decompose transistor spacing will reducing large gate count.

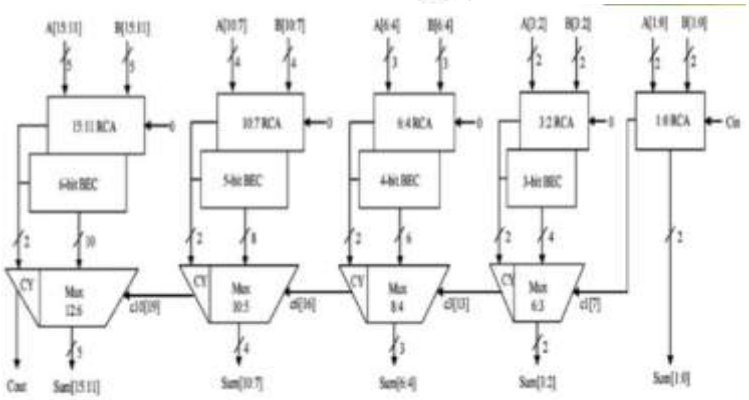

Fig (ii). Modified carry select adder

The proposed design used in place of reverse residue systems to reduce propagation speed and reduce the gate-transistor count. The power factorization in this is estimated using Analytical X power analyzers. The propagating delay and device utilizations

consider using the synthesis report. Existing design contains large LUT'S and large device occupancy compared to proposed MCSA adders. The delays in this reduced compared to existing approach.

IV EXISTING CONVENTIONAL REVERSE CONVERTER DESIGN

I. AREA-POWER PERFORMANCE IN MODULAR REVERSE RESIDUES

Due to large module sets the logic operations increases then complexity increases and large space takes by them. The power consumption increases due to large modules occupancy in this process. The performance of power-delay product values can be synthesized in synthesis report and power factor can be calculated using X power analyzer. In this design the power and delay can calculate using a number of prefix operators to reduce the delay produce. So, prefix operators uses large wiring complexities to increase propagating carry speed and large power occupancies for entire operations cost.

II.CARRY-SELECTION OPERATION

The carry-select adders contain selection of two sets of cascading ripple adders with different carry input values. The prime advantages of using ripple adders are reducing waiting time for carry and reduction power using low power techniques. Ripple adder is the heart of CSA adder to its cascading structure and selection of carry using multiplexers. Due to large number of bits CSA adder is disadvantage based on area. Each cascading stage of RCA adder occupies a set of full adders and half adders charges large gate area. The basic structure of 2-bit carry select adder;

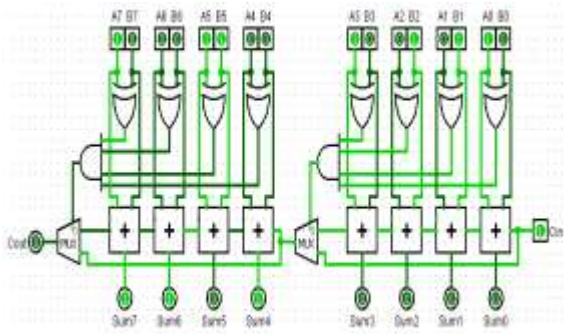

Fig (i): Structure of 2-Bit carry select adder

Due to large gate count and large transistor spacing the area and delay in this adders increases. so, a number of applications should be developed in day-to-day designs to decompose transistor spacing and reduce gate count.

Equations:

Residue systems are used to calculate N integers;

$$\{m_1, m_2, m_3, \ldots, m_N\}$$

Let X is a least integer with M modules then,

$$x_i = X \text{ modulo } m_i$$

Mixed radix (or) Chinese remainder theorem is important algorithm techniques used in residues to form uniform finite set of mixed representations.

V. METHODOLOGY

In this design, the main function of CSA Adder is to reduce the delay and increase their computation speed. The area and power reduction of adder can takes place by reducing a large gate and then decreases the number of transistor count. The major disadvantage of using these adders is it's large area occupancy and large power consumption. So, to reduce these limitations the modified conventional adders are used to compress large area and reduce the large power consumption. The calculation of area can be shown by using schematic report and X power analyzer is a tool used to calculate the output power.

VI RESULTS AND DISCUSSIONS

The design of selecting the modular residue carry adders takes place using Xilinx Sparten3E Device. Modified conventional carry adders are important cascading structure with no carry waiting time and propagate carry by initial representation with carry-in 0 and 1.The entire design for this adder takes place by using VHDL Language and choosing target Device by using sparten3e. MCSA is important structure for its cascading of RCA adders. The area occupancy of MCSA adders can be synthesized using synthesis report shown in fig (i).

I. Synthesis Report:

```
Device utilization summary:
---------------------------

Selected Device : 3s500efg320-5

 Number of Slices:                      4  out of   4656     0%
 Number of 4 input LUTs:                7  out of   9312     0%
 Number of IOs:                        27
 Number of bonded IOBs:                13  out of    232     5%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------
```

Fig (i) Synthesis Report for modified conventional CSA adder

The performance carry select operation can be known using simulation Report. The schematic figures in this can be done using RTL Schematic. The simulation report for CSA adder shown in below fig (ii).

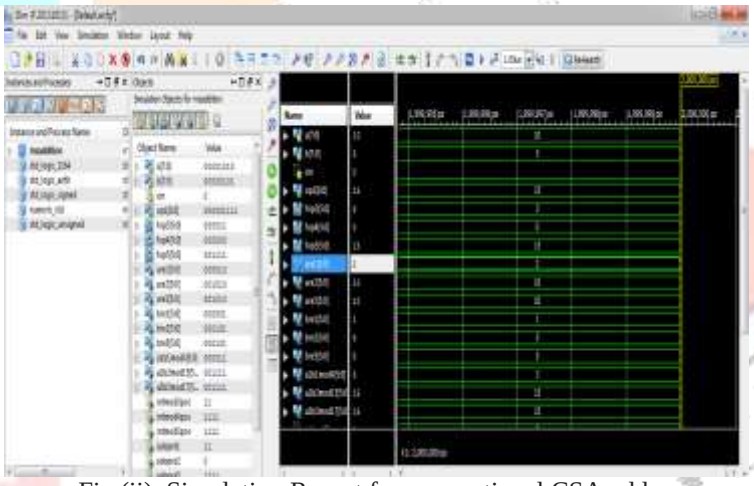

Fig (ii). Simulation Report for conventional CSA adder

The Schematic form of CSA adders contains a number of cascaded RCA adders which is used to estimate the output of the target device. The schematic view of cascaded CSA adders can be shown in below fig (iii)

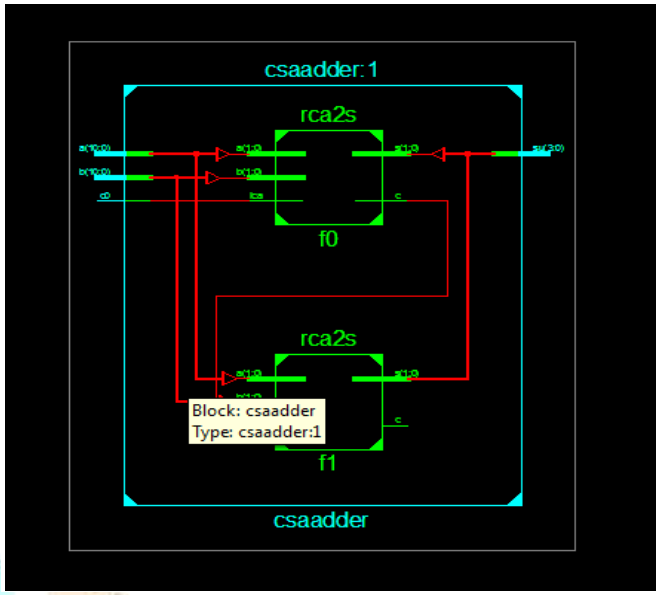

Fig (iii). CSA Adder Schematic view

In VLSI designs, the structure of residue converter design using modified conventional CSA adders can takes place with the help of RTL Schematic. The number of logic blocks for the entire design can be viewed using schematics can be shown in fig (iv).

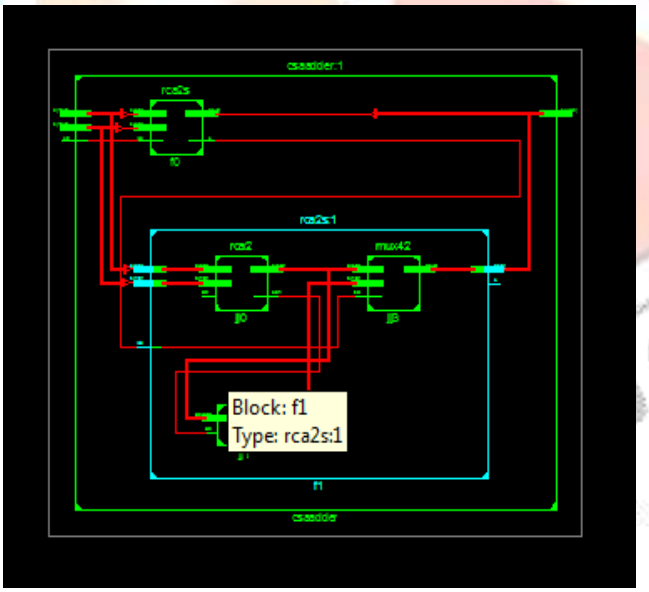

Fig (iv). RTL Schematic for MCCSA Adder

The number of buffer cells can be presented in the residue carry select adder to view the target device by using Xilinx ISE 14.7 .The Spartan 3e is the one of the family in FPGA to focus output of target blocks. Hardware Description language can be used to generate the entire program. The RTL Schematic buffer cells can be shown in below fig (v).

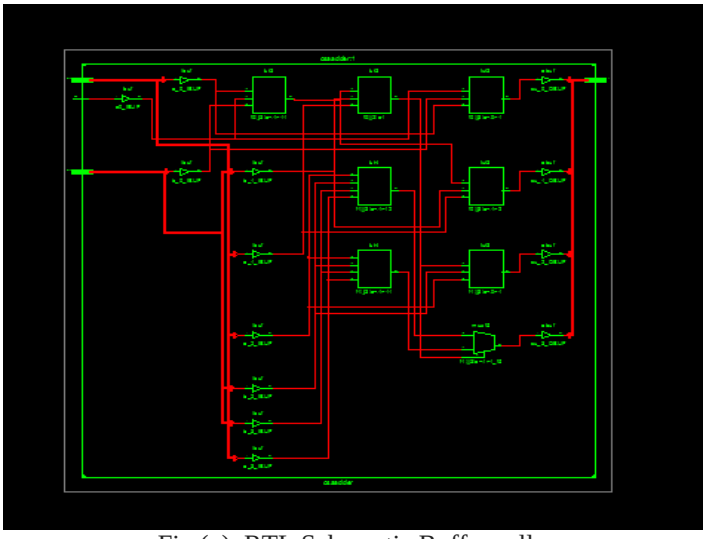

Fig (v). RTL Schematic Buffer cells

II. Output Power Analysis:

X Power analyzer is the important tool to generate the output power by changing their frequency in Mhz. The Existing power analysis of residue prefix converters is more due to number of logic gates and large space occupied by transistors. The output power for existing residue reverse converter design shown in below fig (vi).

Fig (vi). Existing Power for reverse prefix operator design

The output power for conventional MCSA adder generates 80mws of less power compared to existing residue converters design shown in below fig (v).

Fig (vi). Output power for conventional MCSA adder

Figures and tables:

Carry select adder is one of the fastest adders to produce large computation speed and form fastest adders' structure. It has RCA Adders, and multiplexer for the design of conventional adders. The circuit diagram for Normal CSA adder can be shown in fig [1].

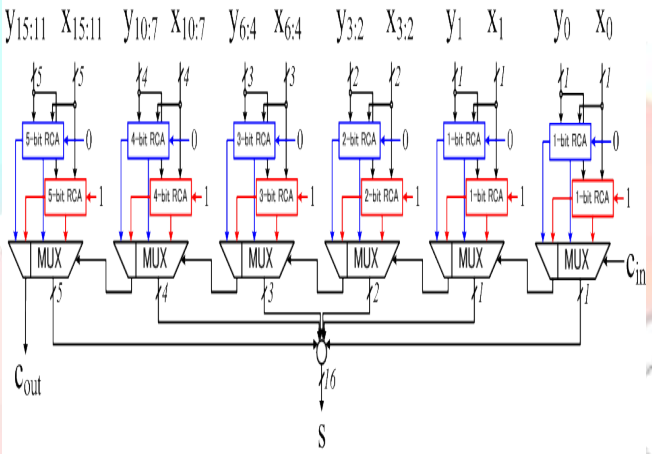

Fig [1]. Normal structure for CSA adder

The dual ripple carries present in CSA adder to produce carries inputs and selecting the carry bits takes place by using multiplexer gate. Due to ripple carry adders, it acquires large number of gates which results large area occupancies shown in below fig.

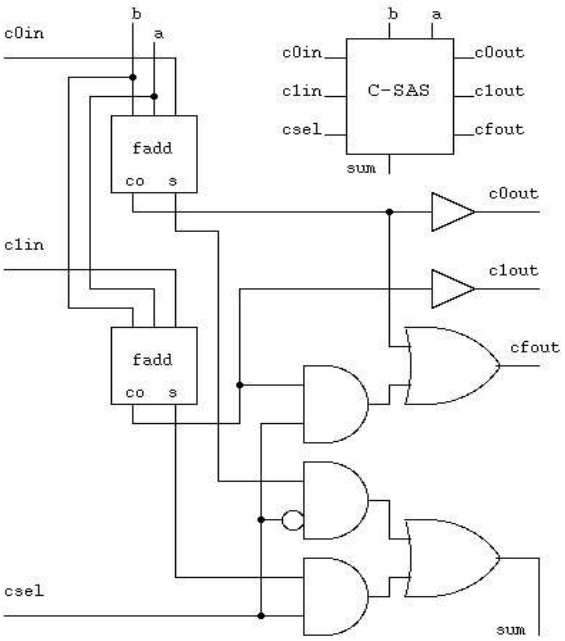

Fig [2] arithmetic operation of CSA Adder

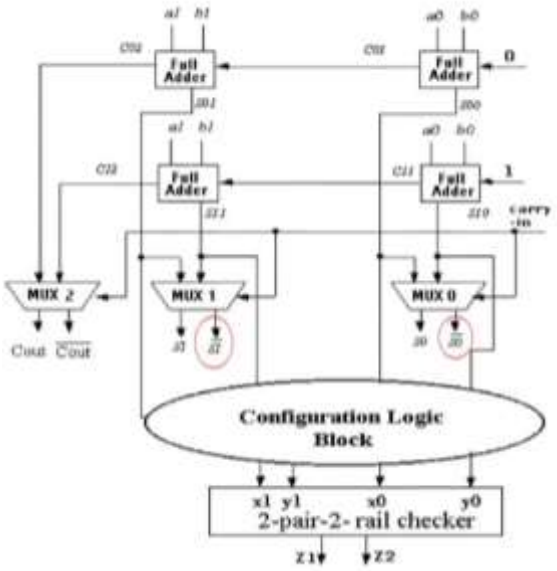

Fig [3]. 2-bit carry-select Adder

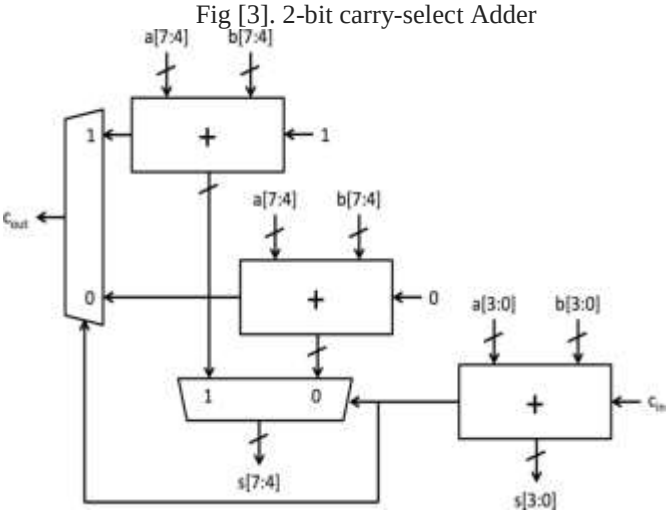

Fig [4] ripple carries structure

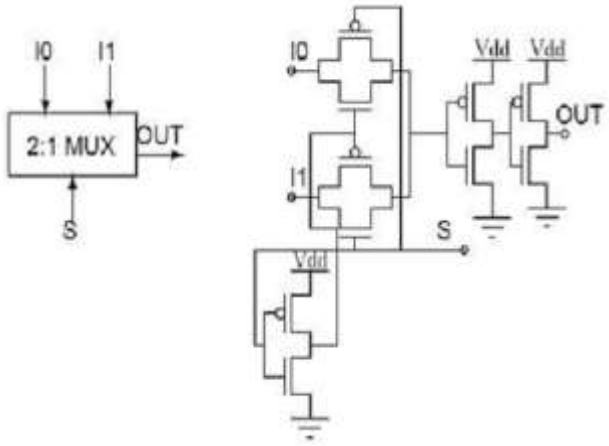

Fig [5] basic circuit diagram for MUX

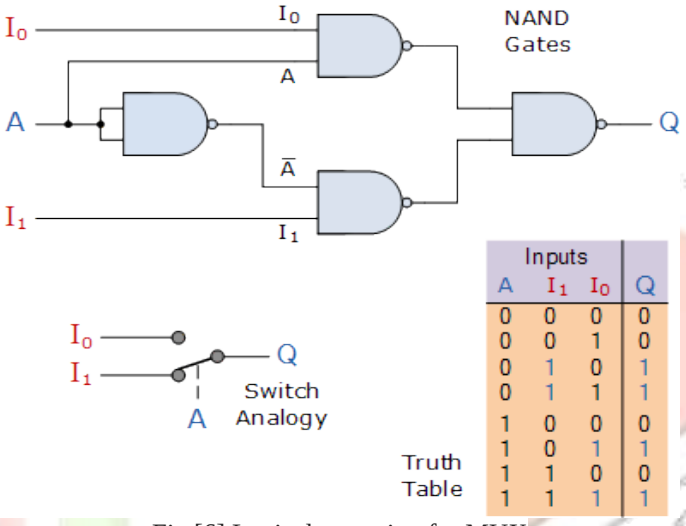

Fig [6] Logical operation for MUX

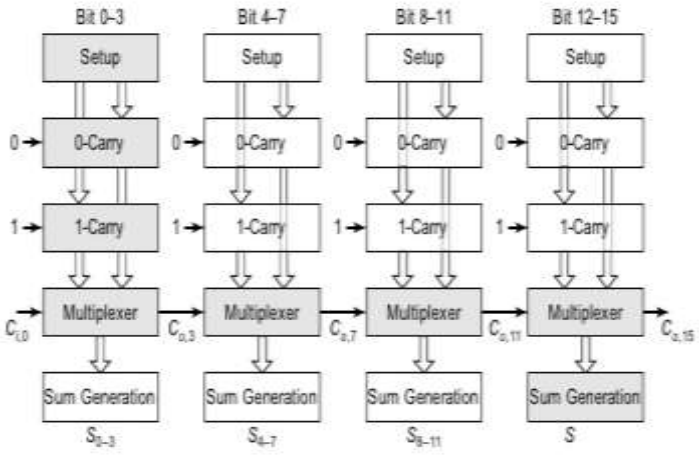

Fig [7] Critical path for CSA Adder

The major disadvantage of using Conventional CSA Adders its area and power consumption due to twice operation for RCA adders. The number of logical gates and transistor count increases due dual RCA Adders. So, in place of RCA operations Excess -1-Bit converters are used to compress the large area occupancy. The modified CSA Adders can be shown below;

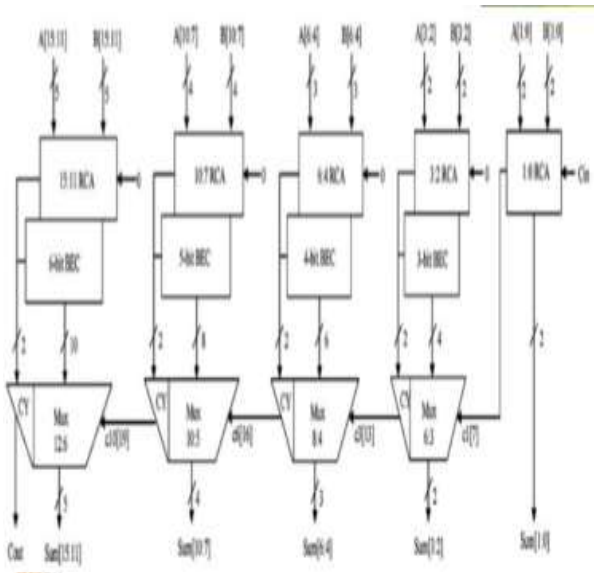

Fig [8] modified conventional CSA Adder

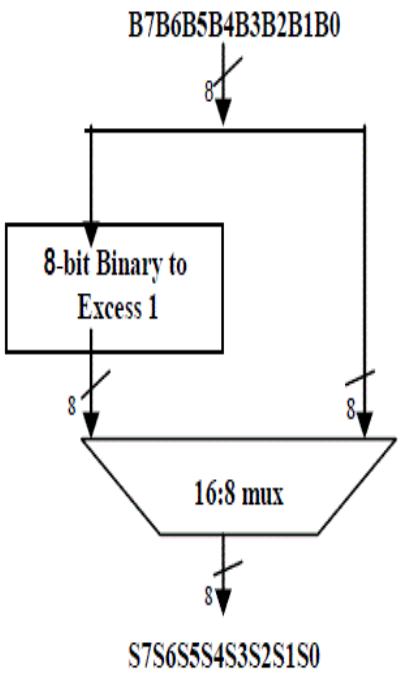

Fig [9] BEC Converter

Table1: performance analysis of adders

	4-bit			8-bit			16-bit		
Types of Adders	Area	Power(in mW)	Dela y(in ns)	Area	Power(in mW)	Del ay (in ns)	Area	Power(in mW)	Del ay (in ns)
RippleCarry Adder	Slice-04 LUT-08 I/O-14	56.05	13.902	Slice-08 LUT-15 I/O-26	56.05	18.646	Slice-18 LUT-32 I/O-50	56.05	33.378
Carry Look Ahead Adder	Slice-04 LUT-08 I/O-14	56.05	11.897	Slice-08 LUT-15 I/O-26	56.05	15.749	Slice-19 LUT-33 I/O-50	56.05	26.486
Carry Select Adder	Slice-06 LUT-11 I/O-14	56.05	11.547	Slice-13 LUT-24 I/O-26	56.05	14.903	Slice-30 LUT-56 I/O-50	56.05	19.934
Carry Save Adder	Slice-03 LUT-06 I/O-14	56.05	9.142	Slice-13 LUT-23 I/O-26	56.05	15.096	Slice-31 LUT-54 I/O-50	56.05	18.485
Carry Increment Adder	Slice-03 LUT-06 I/O-14	56.05	9.043	Slice-11 LUT-20 I/O-27	56.05	14.143	Slice-24 LUT-42 I/O-51	56.05	23.249
Carry Skip Adder	Slice-04 LUT-08 I/O-14	56.05	13.521	Slice-09 LUT-15 I/O-26	56.05	15.345	Slice-14 LUT-25 I/O-50	56.05	18.552

Table 2: Area and power performance for existing and proposed model

S.NO	ADDERS	Area	Power
1.	Existing residue reverse converters	2156mm^2	103mW
2.	Conventional CSA Adder	72mm^2	91mW
3.	Proposed MCSA adders	51mm^2	80mW

V. Acknowledgement:

I feel honored of this opportunity to express a deep sense of gratitude to guide and acknowledgement to our indebtedness to Dr.S.V.Jagadeesh Chandra, Professor for VLSI for assisting us to select the given project, giving valuable guidance, encouragement and effort guiding us throughout our project. We also thank our friends for their support and help they had rendered us through the preparation of the project.

References:

[1] Azadeh Alsadat Emrani Zarandi, Amir Sabbagh Molahosseini, Mehdi Hosseinzadeh, Saeid Sorouri, Samuel Antão, and Leonel Sousa, Reverse Converter Design via Parallel-Prefix Adders: Novel Components, Methodology, and Implementations, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS 1, 1063-8210 © 2014 IEEE, DOI 10.1109/TVLSI.2014.2305392

[2] Sangeetha Rani, Er. Sachin Kumar, Comparison Analysis of 16 Bit Adders, international journal of technical research and Applications, volume2 issue 4 PP. 93-94, ISSN 2320-8360

[3] N. Udaya kumar, K. Bala Sindhuri, K. Durgateja, D. Sai satish, Implementation and Comparison of VLSI Architectures of 16 Bit Carry Select Adder Using Brent Kung Adder, International Conference on Innovations in Power and Advanced Computing Technologi [i-PACT2017], 978-1-5090-5682-8 /17/$31.00 ©2017 IEEE

[4] T. Abhiram, T. Ashwin , B. Sivaprasad, S. Aakash, J.P. Anita, Modified Carry Select Adder for Power and Area Reduction, 2017 International Conference on circuits Power and Computing Technologies [ICCPCT] , 978-1- 5090-4967- 7/17/$31.00 © 2017

[5] C. N Shilpa, D. Kunjan. Shinde, H. Nithin V. Shivamogga, Design, Implementation and Comparative Analysis of Kogge Stone Adder using CMOS and GDI design: A VLSI Based Approach, 978-1-5090-1144-5/16 $31.00 © 2016 IEEE DOI 10.1109/CICN.2016.117

[6] N. Sainath Reddy, JVR Ravindra, A Novel Modulo 2n + 1 Fused Multiply-Adder unit for secured VLSI architectures, 2014 International Conference on Circuit, Power and Computing Technologies [ICCPCT], 978-1-4799-2397-7/14/$31.00 ©2014 IEEE

[7] Hassan Kehinde Bello, Kazeem Alagbe bolagade, An Efficient CRT Based Reverse Converter for {2^2n+1-1, 2n-1, 2^2n-1} Moduli Set, Journal of Advances in Mathematics and Computer Science 25(6):1-9, 2017; Article no.JAMCS.38517 DOI: 10.9734/JAMCS/2017/38517

[8] A. B. Prem kumar, E. L. Ang, and Edmund M.-K. Lai, Improved Memory less RNS Forward Converter
Based on the Periodicity of Residues, IEEE transactions on circuits and systems—ii: express briefs, vol. 5 no.2 1057-7130/$20.00 © 2006 IEEE

[9] S. Surumi. Sukanya Sundaresh, Modified Reverse Converter in Residue Number System via Specific Hybrid Parallel Prefix Adders, International Journal of Science and Research (IJSR) ISSN (Online): 2319-7064, Volume 4 Issue 2, February 2015