MULTIPLY AND ACCUMULATION OPERATION USING HIGH SPEED RoBA MULTIPLIER

ANNADATHA CH LAKSHMI[1], A. RAGHAVARAJU [2]
[1]PG Student, Dept of ECE, Chebrolu Engineering College, JNTUK
[2] Associate Professor, Dept of ECE, Chebrolu Engineering College, JNTUK

Abstract- In this article, we suggest an approximation multiplier that is high speed after energy efficiency. Approaching it is the round of operations to the nearest exponent of two. In this way, the multiplication part of the computation multiplier improved speed and energy consumption are omitted in the price from a small mistake. The proposed approach applies to both Signed and unsigned we suggest three devices make the approximate multiplier that includes one for non-signatories and two for signed operations. Efficiency of the proposed multiplier when comparing its performance with those related to some approximate and exact multiples using different design parameters. In addition, the effectiveness the approximate multiplier proposed in two images is studied processing applications, that is, sharpness and homogeneity of the image. Approximate multipliers are used in two applications for sharpness of the image.

Keywords-Energy efficiency, Approximate multiplier and Power consumption

I. BACKGROUND

Energy minimization is one of the main design requirements in almost any electronic systems, especially the portable ones such as smart phones, tablets, and different gadgets [1]. This starts from the constrained perceptual capacities of individuals in watching a picture or a video. Notwithstanding the picture and video handling applications, there are different ranges where the precision of the math operations is not basic to the usefulness of the framework. Having the capacity to utilize the rough registering gives the originator the capacity of making tradeoffs between the exactness and the speed and additionally control/vitality utilization. Applying the estimate to the number juggling units can be performed at various outline deliberation levels including circuit, rationale, and engineering levels, and also calculation and programming layers. The guess might be performed utilizing distinctive systems, for example, permitting some planning infringement (e.g., voltage over scaling or over timing) and capacity estimation strategies (e.g., altering the Boolean capacity of a circuit) or a mix of them. In the classification of capacity estimation strategies, a multiplier of approximating math building squares, for example, adders and multipliers, at various outline levels have been proposed. In this paper, we concentrate on proposing a rapid low power/vitality yet rough multiplier proper for mistake versatile DSP applications.

II. LITERATURE SURVEY

Inexact unsigned duplication and division in view of an estimated logarithm of the operands have been proposed. In the proposed duplication, the summation of the surmised logarithms decides the aftereffect of the operation. Consequently, the increase is improved to some move and include operations. In this work, AWTM was utilized as a part of a continuous benchmark picture application appearing around 40% and 30% decreases in the power and region, individually, with no picture quality misfortune contrasted and the instance of utilizing an exact Wallace tree multiplier (WTM) structure. In a strategy for expanding the exactness of the duplication approach was proposed. It depended on the disintegration of the information operands. This strategy significantly enhanced the normal mistake at the cost of expanding the equipment of the inexact multiplier by around two times.

In a dynamic fragment technique (DSM) is presented,which plays out the duplication operation on a m-bit section beginning from the main one piece of the information operands. A dynamic range fair-minded multiplier (DRUM) multiplier, which chooses a m-bit portion beginning from the main one piece of the information operands and sets the minimum noteworthy piece of the truncated esteems to one, has been proposed. In this structure, the truncated esteems are duplicated and moved to left to create the last yield. In an inexact 4×4 WTM has been recommended that uses an erroneous 4:2 counter. Likewise, a blunder rectification unit for remedying the yields has been proposed. To develop bigger multipliers, this 4×4 off base Wallace multiplier can be utilized as a part of an exhibit structure.

In a specific check (or relative), an engaging model for automated preparing at the nanometer scale. Correct processing is particularly intriguing for PC gear diagrams. The wander incorporates the examination and blueprint of two new unpleasant approachs 4-2 for use in restraint. These structures depend upon different traits of weight, so invalid in this check (measured by the slip-up rate and the implied standard partition of this botch) ought to be conceivable to the extent estimation in light of the wander of the advantages of the structure (number of transistors, deferment of vitality usage). Four novel cases of gathered pump are open and dismembered for the Dadda multiplier.

Wide show comes to fruition and displayed a great deal of proliferation programming to process pictures. The results prescribe that the proposed structure achieves a basic reducing in charge spread, deferral and number of transistors stood out from the certifiable diagram; in like manner, two of the proposed two designs offer the open entryway for augmentation of picture streamlining the extent that typical intervals botches and a top of the line bustle/repeat extent (more than 50dB, for example, imagery).

III. PROPOSED MULTIPLIER

The proposed approximate multiplier, which is also efficient in the region, was constructed by modifying the traditional multiplication approach at the algorithm level assuming the values of a round chimney. We call this approximate multiplier (ROBA). The proposed multiplication approach applies to signed and unsigned multipliers that show three improved architectures. The efficiencies in these structures are evaluated by comparing delays, energy consumption, energy products and energy delay (EDPS) and areas where there are approximate and minute multipliers (minutes). The contributions of this project can be summarized as follows:

1) Introduce a new scheme to multiply ROBA by modifying the traditional multiplication approach.

2) Describe the three hardware architectures of the proposed multiplication scheme for operations with and without a signature.

A. Multiplication Algorithm of RoBA Multiplier

The main idea behind the proposed multiplier is to take advantage of the ease of operation when the numbers are two a n (2n). For details on the operation of the approach multiplier, first, let us denote the rounded entry numbers of A and B by R and B, respectively. The double A can be rewritten by B

$$A \times B = (A_r - A) \times (B_r - B) + A_r \times B + B_r \times A - A_r \times B_r. \quad \text{.....(1)}$$

$$A \times B \cong A_r \times B + B_r \times A - A_r \times B_r. \quad \text{.....(2)}$$

Therefore, one can perform the multiplication process using three transformation operations and two addition / subtraction operations. In this approach, the closest values for A and B must be determined in the form of 2N. When the value of A (or B) equals 3 × 2p-2 (where p is a positive integer greater than an arbitrary one), they have two values in the form of 2n with absolute differences equal 2p and 2 p -1. While both curators lead to the same effect on the proposed multiplier accuracy, the choice of a larger one (except for the case of p = 2) leads to the application of smaller devices to determine the nearest rounded value, and therefore, it is considered in this project. It derives from the fact that numbers in the form of 3 × 2P-2 is considered not interested in both rounding and simplifying the process down, and can achieve smaller logical expressions if they are used in rounding.

B. Hardware Implementation of RoBA Multiplier

Based on (2), we provide the schematic hardware implementation diagram for the multiplier suggested in Figure 1, where the inputs are represented in a complementary format. First, the input marks are determined and the absolute value of each negative value is generated. Next, the approximation mass gets the closest value for each absolute value in the form of 2n.

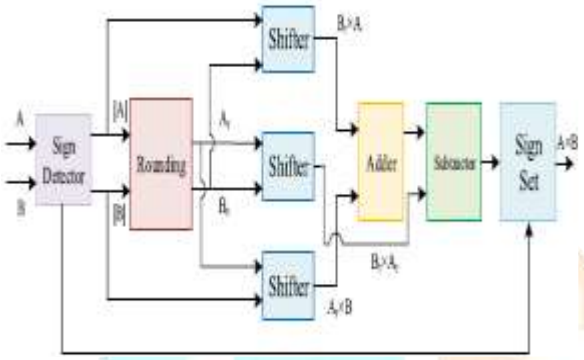

Fig.1. Block diagram for the hardware implementation of the proposed multiplier.

Note that the bit width for the output of this block is n (the absolute importance of the absolute value of n-house in the complementary pattern of the sign is zero). For the nearest value of input A, we use the following equation to determine each output bit of the rounding block:

$$
\begin{aligned}
A_r[n-1] &= \overline{A[n-1]} \cdot A[n-2] \cdot A[n-3] \\
&\quad + A[n-1] \cdot \overline{A[n-2]} \\
A_r[n-2] &= (\overline{A[n-2]} \cdot A[n-3] \cdot A[n-4] \\
&\quad + A[n-2] \cdot \overline{A[n-3]}) \cdot \overline{A[n-1]} \\
&\vdots \\
A_r[i] &= (\overline{A[i]} \cdot A[i-1] \cdot A[i-2] + A[i] \cdot \overline{A[i-1]}) \cdot \prod_{i=i+1}^{n-1} \overline{A[i]} \\
&\vdots \\
A_r[3] &= (\overline{A[3]} \cdot A[2] \cdot A[1] + A[3] \cdot \overline{A[2]}) \cdot \prod_{i=4}^{n-1} \overline{A[i]} \\
A_r[2] &= A[2] \cdot \overline{A[1]} \cdot \prod_{i=3}^{n-1} \overline{A[i]} \\
A_r[1] &= A[1] \cdot \prod_{i=2}^{n-1} \overline{A[i]} \\
A_r[0] &= A[0] \cdot \prod_{i=1}^{n-1} \overline{A[i]}.
\end{aligned}
\qquad \text{……..(3)}
$$

In the proposed equation, R [i] is one in two cases. In the first case, A [i] is one and all the bits on the left side are zero, while A [i - 1] is zero. In the second case, where [i] and all its left bits are zero, [i - 1] and A [i - 2] are one. After determining the rounding values, using three displacement blocks of a barrel, the products are calculated as BR, B, B, B and A. Therefore, the conversion amount is determined based on the logarithm 2-1 (or recorder 2-1) OB). Here, the width of the input bit of the shift lever blocks is n, while its outputs are 2N.

One of the 2N bits is used by Kog Stone Snake to calculate the sum of R × B and B × A. The output of this EDR and R × B are the input of the mass of the supertector whose output is the absolute value of the output of the proposed multiplier. Since R & B have the form of 2n, the sub-inputs can take one of the three input patterns shown in Table I. The corresponding output patterns are also shown in Table I.

The input and output formats have inspired us to visualize a simple circuit based on the following expression:

$$\text{out} = (P \text{ XOR } Z) \text{ AND } (\{(P \ll 1) \text{ XOR } (P \text{ XOR } Z)\} \text{ or } \{(P \text{ AND } Z) \ll 1\})$$

Table I: All possible cases for Ar × Br AND Ar × B + Br × A Values

Input 1 (A_r×B+B_r×A)	*Input 2 (A_r×B_r)*	*Output*
000...11...xxx	000...10...000	000...01...xxx
000...11...xxx	000...01...000	000...10...xxx
000...10...xxx	000...01...000	000...01...xxx

Where P is A + B + B × A and Z × R × B. The corresponding circuit to execute this expression is smaller and faster than the conventional subtraction circuit. Finally, if the scoring score of the final result should be negative, the exit of the subtractor will be denied in the marker of the set of blocks. To eliminate values, which have complementary representations, the corresponding circle based on ¯X + 1 must be used. To increase the speed of the negation, one can transcend the process of increasing the phase of negation by accepting the associated error. As will be seen later, the importance of the error decreases with the increase of the entrance width. In this project, if the exact (almost) negation is performed, the implementation is called multiplier of duplication (S-Roba) multiplier [approximately S-Roba (S-Roba) multiplier].

In the case where the input is always positive, to increase the speed and reduce the power consumption, the signal detector and the signal cluster blocks are removed from the architecture, providing us with the so-called Roba architecture (U-Roba). signed In this case, the output of the rounding block is n + 1, where this bit is determined on the basis of [n] = A [n - 1] • A [n - 2]. This is because the 11x state is not signed. . . x (where x denotes not to disturb) with n bit width, its rounding value is 10 ... 0 with bit width of n + 1. Therefore, the input width of the modulators is n + 1. However, due to the maximum transformation It is considered that N-1, 2N shows the output bits of the modulators.

IV. RESULTS AND DISCUSSION

To evaluate the viability of the proposed multiplier, there was a discrepancy between the three replicas of Rosa's banks and some incorrect and correct multipliers. Pug and Wooly were selected in the light of the Wallace tree design (as a valid marker) and Wallace multiples (as an incorrect location) as correct multiples. In addition, due to imprecise complications, DSM8, DRUM6 and them were selected. Since [12] we have not used the equipment, we have prohibited this investigation. The complications were activated with the Verilog tone dialect technique and then modulated using the Synopsys compiler scheme with the integration option with the target diff base with a 45 nm innovation.

A. Existing System Results:

Device Utilization Summary				
Logic Utilization	Used	Available	Utilization	Note(s)
Number of 4 input LUTs	436	4,896	8%	
Number of occupied Slices	225	2,448	9%	
Number of Slices containing only related logic	225	225	100%	
Number of Slices containing unrelated logic	0	225	0%	
Total Number of 4 input LUTs	437	4,896	8%	
Number used as logic	436			
Number used as a route-thru	1			
Number of bonded IOBs	32	158	20%	
Average Fanout of Non-Clock Nets	2.78			

Fig.2. Design summary

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Timing Summary:
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Speed Grade: -4

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 38.263ns

Timing Detail:
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All values displayed in nanoseconds (ns)
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Fig.3. Synthesis report

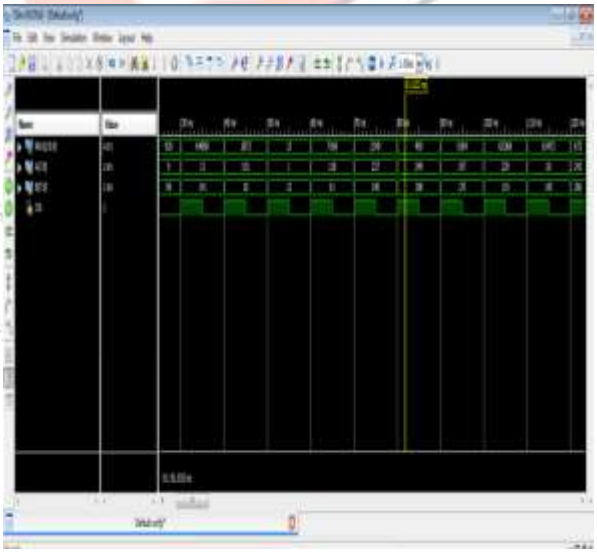

Fig.4. Simulation results

B. Proposed System Results:

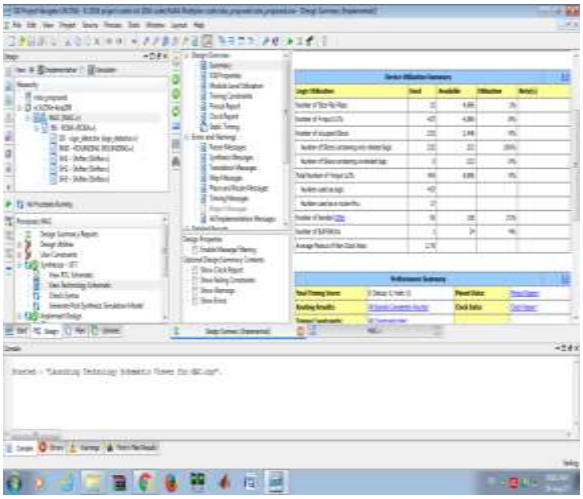

Fig.5. Design summary of proposed system

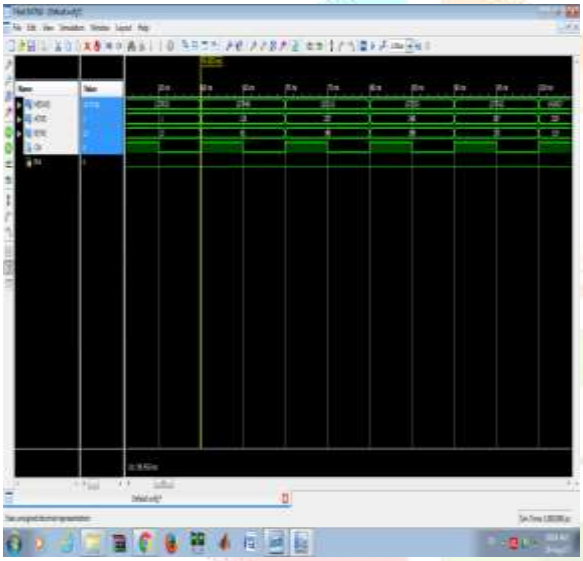

Fig.6. Simulation results

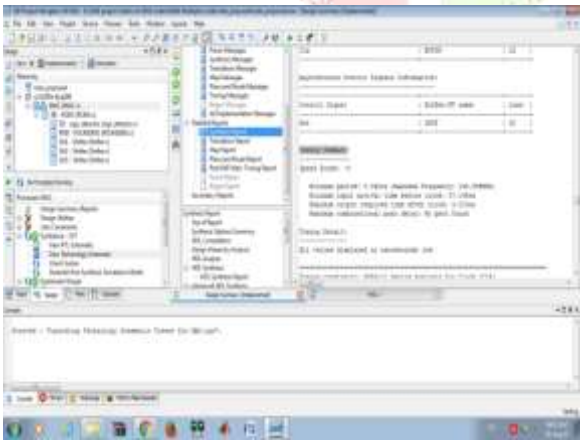

Fig.7. Synthesis report

V. CONCLUSION

In this research, we proposed a high speed approach after energy efficiency called Roba multiplier. The proposed multiplier, which is highly accurate, was based on the approximation of the entries in Figure 2n. In this way, the computational capacitance portion of the multiplication was eliminated to improve the speed and energy consumption at a small error rate. The proposed approach was applied to the signed and unsigned complications. Three applications for approximate multiplier devices were discussed, including one for unsigned processes and two signed processes. The powers of the proposed multipliers were evaluated by comparing them with some nearby and nearby multipliers using different design parameters. The results showed that in most cases (all), the Roba multiplier architectures exceeded the approximate (micro) multiples. In addition, the effectiveness of the approach of approximate multiplication proposed in two applications to treat images of sharpness and homogeneity was studied. The comparison revealed the same qualities as those of the exact multiplication algorithms.

VI. REFERENCES

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Authors:

Ms. ANNADATHA CH LAKSHMI has completed her B.Tech in ECE Department from Chirala Engineering College, JNTU Kakinada. Presently she is pursuing her Masters in VLSI & Embedded Systems (VLSIES) in Chebrolu Engineering College, Chebrolu, India.

Mr. A RAGHAVARAJU has completed B.Tech (ECE) from Jawaharlal Nehru University, Hyderabad, M.Tech (ECE) from Anna University, Chennai, and Pursuing PhD from KL University, Guntur. He is having 10 years of experience in Academic, Currently working as Associate Prof at Chebrolu Engineering College, Chebrolu, India.