Design and Implementation of Comparison Brent Kung Adder & Quantom Dot CellularAutomata Adder using Carry skip Adder

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ABSTRACT

Carry skip logic (CSKA) is one of replaced in many data processing processors to perform fast arithmetic functions. Adders are the basic building blocks in digital integrated circuit based designs. Ripple carry adders are slowest adders as every full adder must wait till the carry is provoke from previous full adder. In this paper, we present a Carry skip logic (CSKA) structure that has a higher speed yet lower energy consumption compared with the conventional one. In this paper, AND-OR-Invert (AOI) and OR-AND-Invert (OAI) compound gates for the select logic for existing and proposed method. In addition, instead of utilizing Parallel prefix Adder, the proposed structure makes use of QCA technique for arithmetic operations. The quantum-dot cellular automata (QCA) approach means one of the possible solutions to reduce the power consumptions, area and delay for general processors.

1. INTRODUCTION

There are many works on the subject of optimizing the speed and power of these units, which have been reported. Obviously, it is highly desirable to achieve higher speeds at low-power / energy consumptions, which is a challenge for the designers of general purpose processors. One of the effective techniques to lower the power consumption of digital circuits is to reduce the supply voltage due to quadratic dependence of the switching energy on the voltage.

Nanotechnology draws much attention from the public now-a-days. Because the current silicon transistor technology aspect challenging problems, such as high power consumption and difficulties in feature size reduction, alternative technologies are sought from researchers. Quantum-dot cellular automata (QCA) is one of the promising future solutions. Quantum dot cellular automata, which is an array of coupled quantum dots to implement boolean logic functions. The advantage of QCA is high stuffing densities by virtue of the small size of the dots, simplified interconnection and low area delay product.

The basic idea behind using VSS CSKA structures was based on almost balancing the delays of paths such that the delay of the critical path is minimized compared with that of the FSS structure. This deprives us from having the opportunity of using the slack time for the supply voltage scaling. To provide the variable latency feature for the VSS CSKA structure, we replace some of the middle stages in our proposed structure with a PPA existing in this paper. The existing hybrid variable latency CSKA structure is shown in Fig. where an *Mp*-bit existing PPA is used for the *p*th stage (nucleus stage). Since the nucleus stage, which has the largest size (and delay) among the

2. Existing system

2.1 Hybrid variable latency CSKA

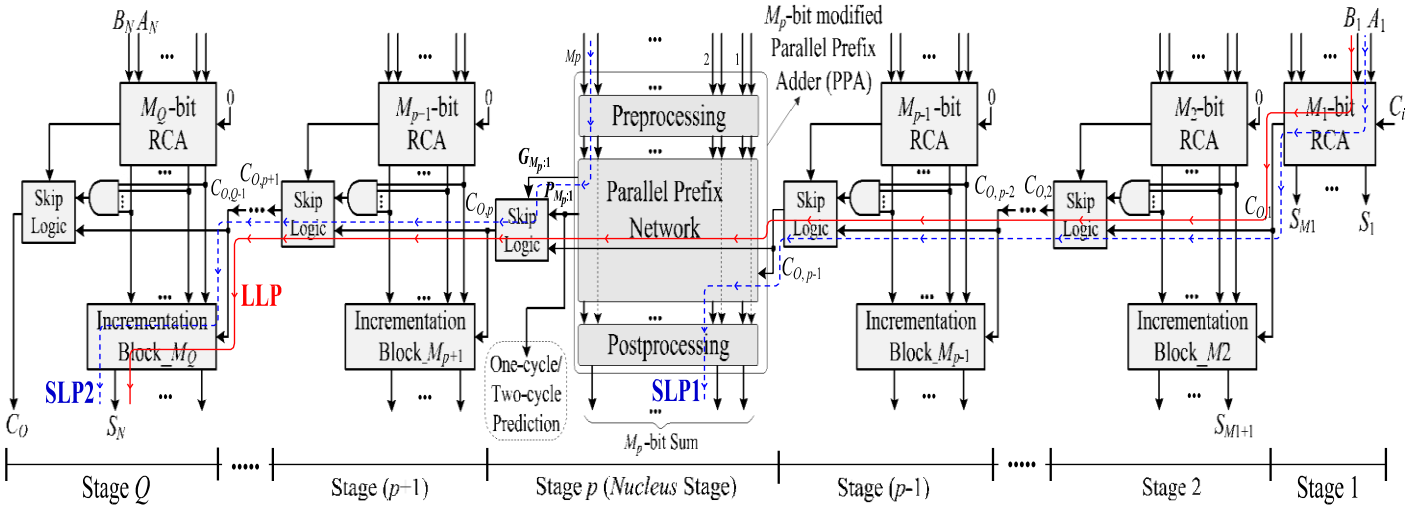


Fig. Structure of Hybrid variable latency CSKA

stages, is present in both SLP1 and SLP2, replacing it by the PPA reduces the delay of the longest off-critical paths.

Thus, the use of the fast PPA helps increasing the available slack time in the variable latency structure.

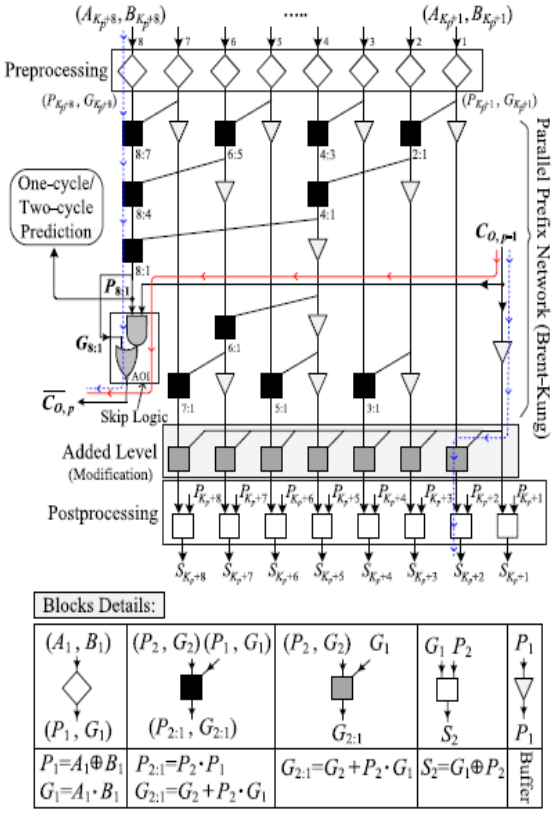
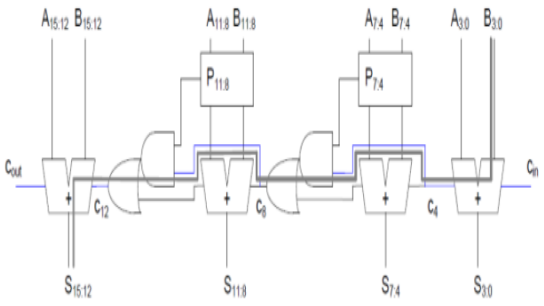


Fig 2. Internal structure of the *p*th stage of the proposed hybrid variable latency CSKA.

It should be mentioned that since the input bits of the PPA block are used in the predictor block, this block becomes parts of both SLP1 and LP2. In this hybrid structure, the prefix network of the Brent–Kung adder is used for constructing the nucleus stage Fig. One the advantages of the this adder compared with other prefix adders is that in this structure, using forward paths, the longest carry is calculated sooner compared with the intermediate carries, which are computed by backward paths. In addition, the fan-out of adder is less than other parallel adders, while the length of its wiring is smaller. Finally, it has a simple and regular layout. The internal structure of the stage *p*, including the modified PPA and skip logic, is shown in Fig. Note that, for this figure, the size of the PPA is assumed to be 8 (i.e., $Mp = 8$).

2.2. Carry-Skip Adder

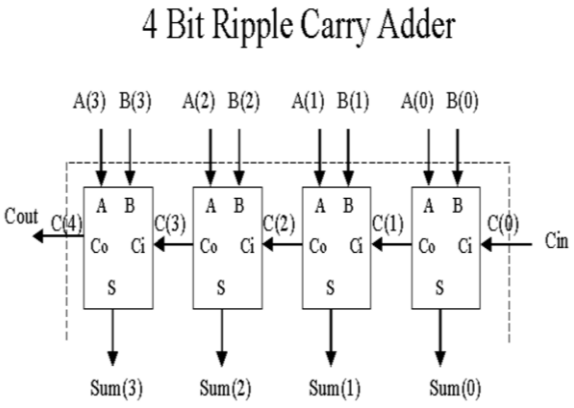
The carry-skip adder design presented in this paper uses a combination of RCAs together with carry-skip logic (SKIP), carry-generate logic (CG), and group generate-propagate logic (PG). The complete adder is divided into a number of variable-width blocks.



Both the carry generation and skip logic use AOI and OAI circuits. The width of each block is limited by the target delay T. Each block is further divided into subblocks. A subblock may contain additional levels of subblocks in a recursive manner. The lowest-level subblock is formed by a number of variable width RCAs. The adder structure is described as follows: There is an alternative way of reducing the delay in the carry-chain of a RCA by checking if a carry will propagate through to the next block. This is called carry-skip adder.

RCA

Ripple Carry Adder can be constructed with full adders connected in cascade, with the carry output from each full adder connected to the carry input of the next full adder in the chain. Fig. shows the interconnection of four full adder (FA) circuits to provide a four bit ripple carry adder.



3. Proposed Quantum Dot Cellular Automata Adder

In 1993, Lent et al. proposed a physical implementation of an automaton using quantum dot cells. The automaton quickly gained popularity and it was first fabricated in 1997. Lent combined the discrete nature of both cellular automata and quantum mechanics, to create nano-scale devices capable of performing computation at very high switching speeds and consuming extremely small amounts of electrical power. Today, standard solid state QCA cell design considers the distance between quantum dots to be about 20 nm, and a distance between cells of about 60 nm. Quantum dot Cellular Automata are based on the simple interaction rules between cells placed on a grid.

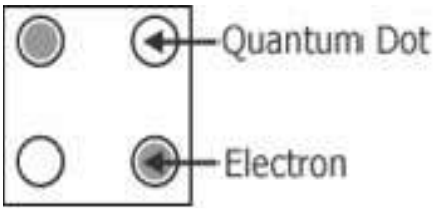


Fig 3: Simplified Diagram of QCA Cell

A QCA cell is constructed from four quantum dots arranged in a square pattern. These quantum dots are sites electrons can occupy by tunneling to them. Because of Columbic repulsion,

the two electrons will always reside in opposite corners. The locations of the electrons in the cell (also named polarizations P) determine two possible stable states that can be associated to the binary states 1 and 0. Although adjacent cells interact through electrostatic forces and tend to align their polarizations, QCA cells do not have intrinsic data flow directionality.

The basic QCA cell consists of four quantum dots in a square array coupled by tunnel barriers. The physical mechanism for interaction between dots is the Coulomb interaction and the quantum-mechanical tunneling. Electrons are able to tunnel between the dots, but they cannot leave the cell. If two mobile electrons are placed in the cell, in the ground state and in the absence of external electrostatic influence, Coulomb repulsion will force the electrons to dots on the opposite corners. The Figure 3 shows a simplified diagram of a quantum-dot cell.

If the cell is charged with two electrons, each free electron to tunnel to any site in the cell, these electrons will try to occupy the furthest possible site with respect to each other by virtue of mutual electrostatic repulsion. Therefore, two distinguishable cell states exist. Figure 3.1 shows the two possible minimum energy states of a quantum dot cell. The state of a cell is called its polarization, denoted as P.

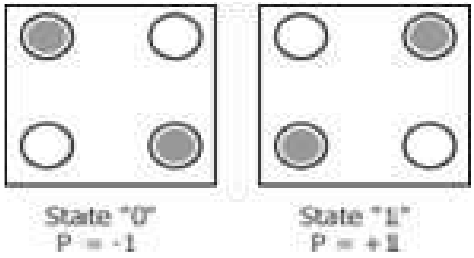


Fig 3.1: Four Dot Quantum Cell

Although arbitrarily chosen, using cell polarization P = -1 to represent logic "0" and P = +1 to represent logic "1" has become standard practice.

3.2 Majority Gate

A majority gate consists of five QCA cells that realize the function of M(a; b; c) = ab + bc + ac.

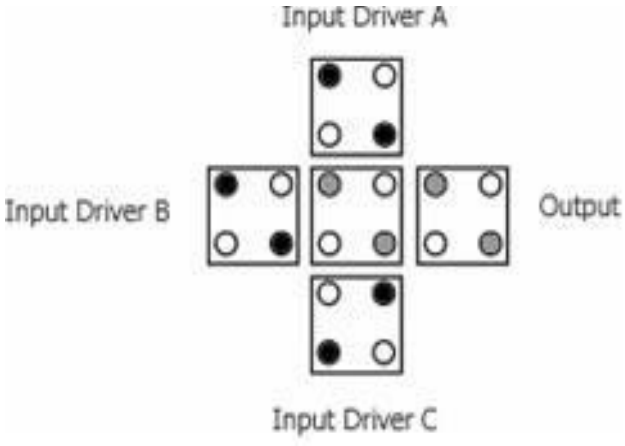


Figure.3.2. Majority gate

Two-input AND gate and OR gates can be designed by fixing one of the majority gate inputs to ”0” and ”1”, respectively shown as follows. AND = M(a,b,0) OR = M(a,b,1) If one input is set to 0, then the output is the AND of the other two inputs. If one input is set to 1, then the output is the OR of the other two inputs. With ANDs, ORs, and inverters, any logic function can be realized.

4. Modification Block diagram

The Proposed Hybrid Variable Latency CSKA replaced. In this Structure proposed structure with QCA modified in this paper.

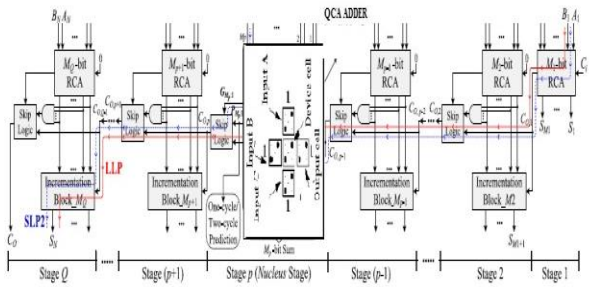


Fig. Block diagram of QCA and CSKA.

This paper first presents efficient quantum-dot cellular automata (QCA) design for the Ladner–Fischer prefix adder. Then efficient QCA design of a hybrid adder that combines the Ladner–Fischer adder with a ripple carry adder.

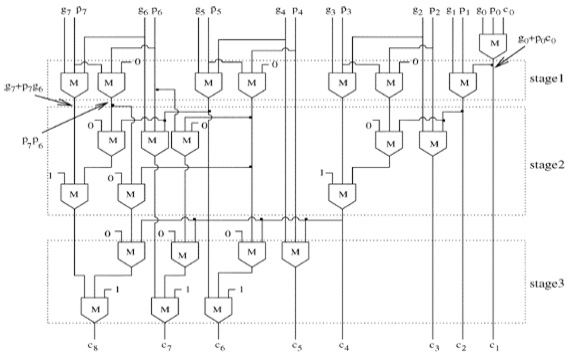


Fig 4.1.Block diagram of Majority Gate

We show that the hybrid adder has better performance (in terms of latency) in QCA than a Ladner–Fischer or a ripple carry adder. We also show that the hybrid adder has a smaller area-delay product than existing adder designs in QCA.

The Ci, is produced at bit-stage i if either one is provoke at that stage or if one is propagated from the preceding stage. So a carry is provoke if both operand bits are 1, and an incoming carry is propagated if one of the operand bits is 1 and the other is 0.

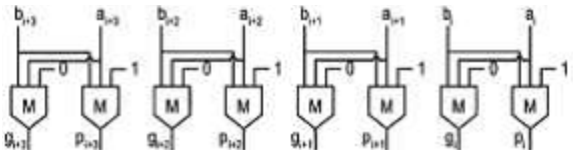


Fig Generation of propagate and generate bits

Gi = AiBi and Pi = Ai^Bi

Let Pi and Gi denote the generation and propagation, Compared with a

ripple adder, as well as some of the other adders, a pure carry-look ahead adder has higsh logic costs. Furthermore, high fan-in and fan-out requirements can be problematic: the fan-out required of the Gi and Pi signals grows rapidly with n, as does the fan-in required to form Ci. For sufficiently large values of n, the high fan- in and fan-out requirements will result in low performance, high cost, or designs that simply cannot be realized.

5. SIMULATION RESULTS

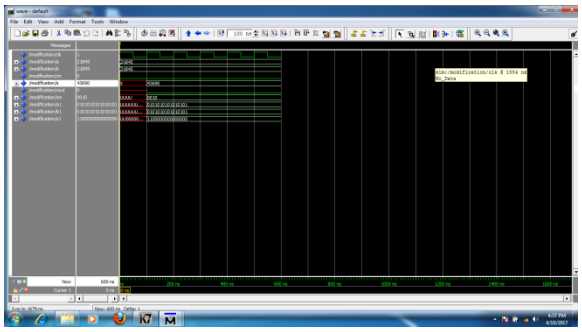
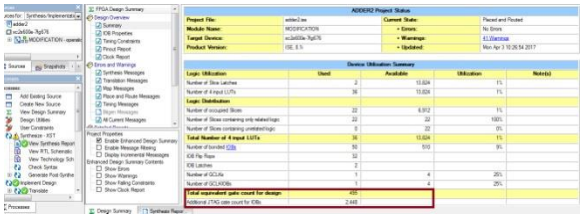
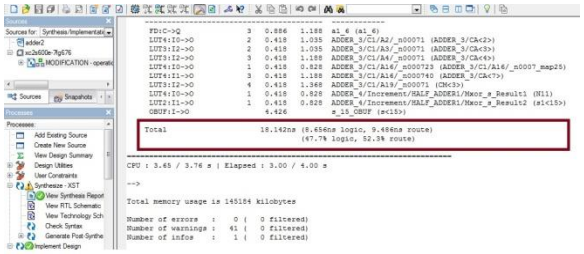


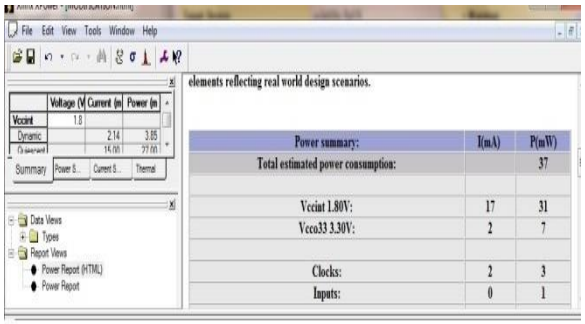
Figure.8: Simulation waveform of QCA Adder



Figure(a) AREA



Figure(b) DELAY



Figure(c) POWER CONSUMPTION

6. CONCLUSION

The main idea of this project is to introduce QCA method. In the current work, the QCA is used instead of PPA method. This QCA method can be used for low power consumptions, area and delay, the required logic can be executed within an optimized area which performs faster when related to the previous one.

PARAMETERS	PPA	QCA
POWER(Wts)	41	37
DELAY	20ns	18.14ns
AREA(Register)	549	495

Table.1: Comparison of parameters Area, Delay & Power consumption

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