Design of Low Power Reconfigurable Router for Network on Chip (NoC) Applications

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Abstract:The reconfigurable router for NOC has been arranged in the present business. Here the router which has been planned contains four channels viz, west, east, south and north and a solitary framework switch. An individual channel contains MUX and FIFO memory. The information inputs and yields are confined by MUX and information stockpiling is accomplished utilizing FIFO memory. At first, south channel is planned alongside its sub-pieces like MUX and FIFO memory. Later the framework switch and remaining channels are planned. At last, planned channels alongside their MUX, FIFO buffer and a cross bar switch are fused to present the whole router structure. The execution of the router is completed by method for Verilog HDL. Obtained results show that the proposed design consumes less power compared to the previously designed reconfigurable routers.

KEYWORDS: Network on Chip(NoC); Reconfigurable Router; First in First out(FIFO) Buffer; Crossbar Switch; Multiplexer; Register Transfer Level(RTL) Design, Low Power.

I. INTRODUCTION

There has been an expansion in the quantity of Intellectual property (IP) centers for an inserted framework furthermore in the calculation prerequisite. The computational necessities of complex calculations can be taken care of by the superior installed stages which is created as there is a prerequisite for an implanted framework. An advances in the assembling innovations , lessened measurements in the transistor gadget , there has been bringing up in the pressing thickness and expanding in the extensive number of IP centers are fused ceaselessly inside the chip ,this offering raise to the idea of Multiprocessor framework on Chip (MPSOC's).

The scaled measurements in the semiconductor transistor gadget encourage to absorb number of Intellectual Property (IP) obstructs on a solitary System-On Chip (SOC). Be that as it may, it prompts most recent inconveniences in between IP network. Interconnection in the old shared transport neglects to profit the adaptability and versatility when managing countless in a solitary chip. So to conquer these constraints, Network-On-Chip (NOC) has been presented. As NOC bifurcates the estimation from the correspondence parts , this makes workable for NOC to manage the cost of a versatile and adaptable secluded design.

Massive size systems are downsized in NOC's and connected to the dug in SOC .As immense measure of IP centers are consolidated on a singular part in the NOC outline , the correspondence component gets to be one of the exceptionally predominant issue among these centers. One fundamental key element is that, correspondence inside these IP centers must be sans mistake. A very much arranged course of action is required to do this correspondence.

A few system topologies have been presented and the choice of the topology is the first and the principal thing. The NOC's has three fundamental key parts viz switches, wrappers and connections. Router is the most vital and fundamental component of NoC's. The advancement in the framework execution, decrease in region and less power are the key needs of the router structure .The fundamental objective of the present work is to devise a reconfigurable router.

II. LITERATURE SURVEY

The growing complexity of customizable single-chip multiprocessors is requiring communication resources that can only be provided by a highly-scalable communication infrastructure. This trend is exemplified by the growing number of network-on-chip (NoC) architectures that have been proposed recently for system-on-chip (SoC) integration. Developing NoC-based systems tailored to a particular application domain is crucial for achieving high-performance, energy-efficient customized solutions. The effectiveness of this approach largely depends on the availability of an ad hoc design methodology that, starting from a high-level application specification, derives an optimized NoC configuration with respect to different design objectives and instantiates the selected application specific on-chip micronetwork. Automatic execution of these design steps is highly desirable to increase SoC design productivity. This work illustrates a complete synthesis flow, called Netchip, for customized NoC architectures, that partitions the development work into major steps (topology mapping, selection, and generation) and provides proper tools for their automatic execution (SUNMAP, xpipescompiler). The entire flow leverages the flexibility of a fully reusable and scalable network components library called xpipes, consisting of highly-parameterizable network building blocks (network interface, switches, switch-to-switch links) that

are design-time tunable and composable to achieve arbitrary topologies and customized domain-specific NoC architectures. Several experimental case studies are presented In the work, showing the powerful design space exploration capabilities of the proposed methodology and tools.

III. PROPOSED DESIGN

In this present work, planning of complete router structure and outline of its related sub-modules has been talked about. Portrayal about all these is appeared in the beneath area. Router assumes a basic part in Network-On-Chip. A router is a gadget that exchanges the information parcels along the PC systems. The fundamental occupation of the router is , it will identifies the system point to which information ought to be transmitted towards its wanted destination. It will take after the steering calculation to forward the information. Router does the activity coordinating undertaking, in this way information sending turns out to be simple from one gadget to the next with no data sticking. Without the router NoC can't be exist. Along these, router frames the most crucial part of NoC. Essentially router incorporates a buffers, switch and arbiters.

The planning of the router incorporates the making four channels to be specific, west channel, east channel, north channel and south channel alongside a crossbar switch as appeared in fig 1. To outline all these channels, at First-InFirst-Out (FIFO) buffer and multiplexer must be made. At last all the planned channels, a crossbar switch are consolidated to accomplish the complete router architecture.

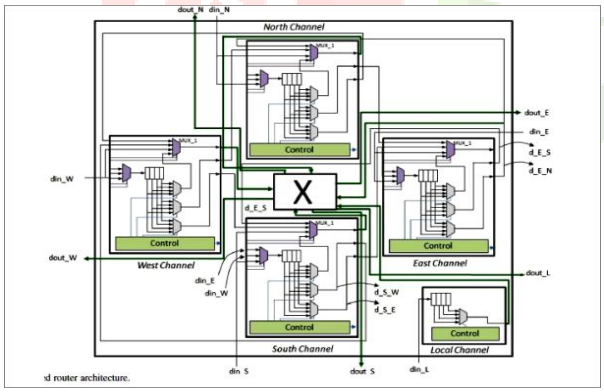

Fig.1. Router Architecture

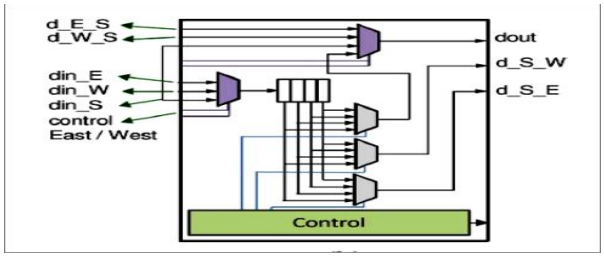

Fig. 2. Input FIFO in South Channel

Every channel involves First-In-First-Out buffer which has 16 areas and five multiplexers. The measure of information present in the FIFO buffer is implied for the conditions like 0%, 25% , half , 75% and 100%, then five multiplexers are utilized. To accomplish control over all these five multiplexers, control component is utilized. The configuration of buffer in a south channel is appeared in fig 2.

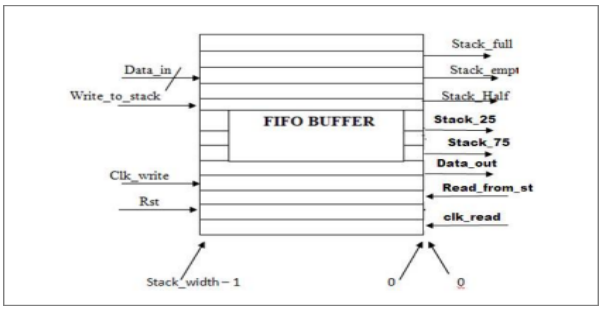

Fig.3. Design of FIFO Buffer

The outline of FIFO support is portrayed in fig.3. On the off chance that the velocity of the source clock is higher than that of pace of destination clock ,then it can't for the destination clock to test the information at the pace of source clock. This will bring about loss of information. To triumph this issue ,two autonomous timekeepers i.e. clk_read and clk_write has been utilized for both the read and compose operation as appeared in the above fig 3. This will accelerate the operation and postponement turns out to be less. In the present work ,First-In-First-Out (FIFO) buffer is utilized. Fundamentally buffer is a capacity gadget i.e. it is utilized to store the information temporarily. Though FIFO is basically refers as information which is entered at first is handled first and that one is given as yield. This is the rationale behind the FIFO support.

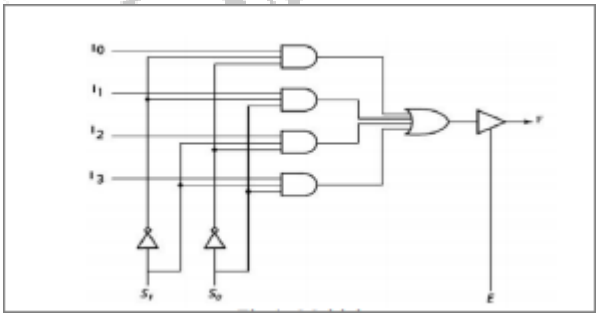

Fig.4. Multiplexer

The 4x1 multiplexer is utilized as a part of this work and it is executed utilizing fundamental AOI logic gates is shown in figure 4. 4x1 multiplexer has four information signals I0, I1, I2 and I3 and single yield sign. The two select inputs s0 and s1 are utilized to choose any of the inputs out of four inputs. Essentially multiplexer contains select inputs to choose any of the info signal inside numerous information signals. Along these lines select inputs acts like a control inputs .Based on the information given on the select inputs , just that specific information sign is changed to the single yield line.

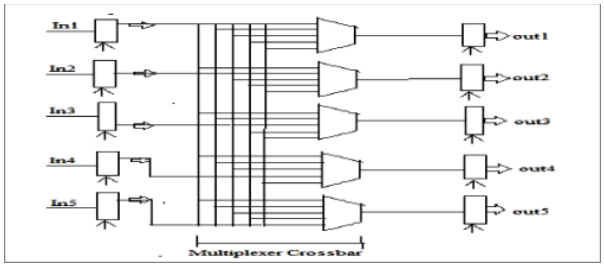

Fig.5. Crossbar Switch

Crossbar switch can be considered as a heart of the router information way. Network switch or the cross point switch are another names for the crossbar switch. The primary capacity of the crossbar switch is, it will interfaces the few inputs to a few yields. In the present work, the devise of the framework switch has 5 inputs and corresponding 5 yield ports. At the instance of the router capacity, crossbar switch associates the information from information sign to the yield signal. The entryway level circuit of the crossbar switch is appeared in fig 5.

IV. METHODOLOGY

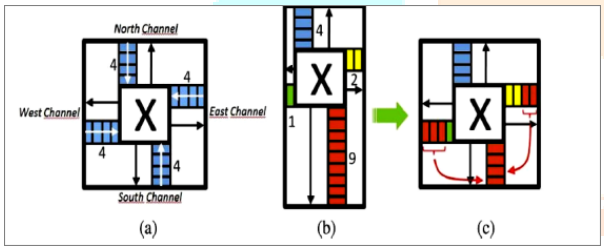

Fig. 6. (a) Design of router with buffer size 4 (b) Router design according to require of data (c) Router design with sharing of data among neighboring ones.

The proposed idea in this work is appeared in the fig 6. As appeared in the figure 6, figures (a) and (b) are the beforehand existed frameworks. A reconfigurable router engineering with the settled support size is proposed as given in fig(a) .In this framework , as all the buffer sizes are altered at profundity 4 ,when all the buffers are filled totally, then the buffers can't store the recently arrived information .This prompts the information misfortune and power utilization turns out to be more. Because of this execution of the router additionally corrupts. To defeat these issues, router design according to the necessity of the information for various NoC applications is proposed as delineated in fig (b). Here the span of the south FIFO is made bigger i.e. it is settled at profundity 9 contrasted with east ,west and north buffers. While the north buffer size is settled at profundity 4, which is bit bigger than west at profundity 1 and east at profundity 2. In this outline , at whatever point any buffer are filled totally then new information is made to store in the south FIFO . Once if south FIFO is full ,it not able to store the following arrived information and there by again information misfortune happens .therefore , power utilization turns out to be progressively and execution turns out to be less. Again this framework additionally neglects to meet the sought prerequisites. To dispense with all these , low power reconfigurable buffer is proposed as appeared in fig (c) and this is the present technique which has been received in this present work. In the present work , FIFO's are composed in a manner that they are having the capacity of offering the information to their neighbouring ones. This outline technique helps in minimizing the information misfortune and recoveries the power as opposed to the past strategies. This outline can be utilized for any uses of NoC's .

IV. RESULTS

Simulation.

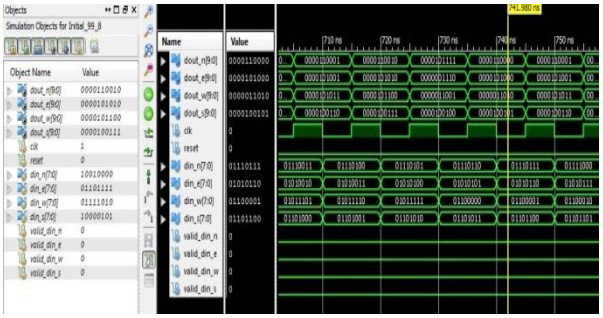

Fig7: Top module simulation waveform.

RTL Schematic.

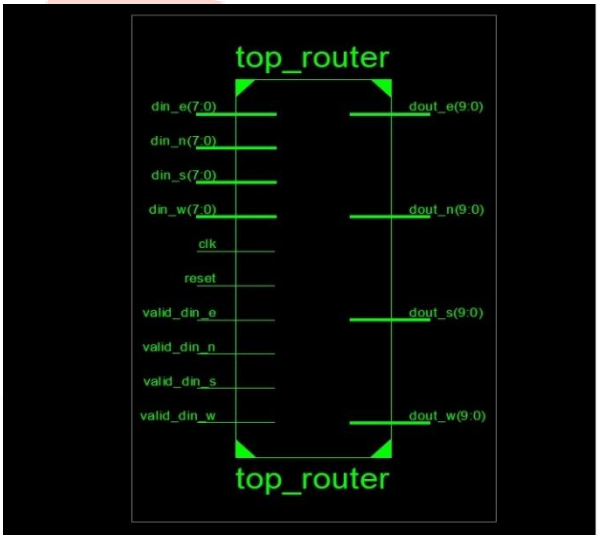

Fig8:RTL Schematic.

Design Summary.

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	203	4656	4%
Number of Slice Flip Flops	182	9312	1%
Number of 4 input LUTs	359	9312	3%
Number of bonded IOBs	78	232	33%
Number of GCLKs	1	24	4%

Timing Summary.

```
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 280 / 40
--------------------------------------------------------------------------------
Offset:              6.104ns (Levels of Logic = 3)
  Source:            EAST_INPUT_FIFO/read_cnt_0 (FF)
  Destination:       dout_e<9> (PAD)
  Source Clock:      clk rising

  Data Path: EAST_INPUT_FIFO/read_cnt_0 to dout_e<9>
                                Gate     Net
    Cell:in->out      fanout   Delay    Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDR:C->Q             23   0.514    1.174  EAST_INPUT_FIFO/read_cnt_0 (EAST_INPUT
     LUT3:I0->O            1   0.612    0.000  EAST_INPUT_FIFO/mux10_3 (EAST_INPUT_FI
     MUXF5:I1->O           1   0.278    0.357  EAST_INPUT_FIFO/mux10_2_f5 (dout_e_0_0
     OBUF:I->O                 3.169           dout_e_0_OBUF (dout_e<0>)
    ----------------------------------------
    Total                      6.104ns (4.573ns logic, 1.531ns route)
                                       (74.9% logic, 25.1% route)

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Fig9: Timing summary of the project.

Power Analysis.

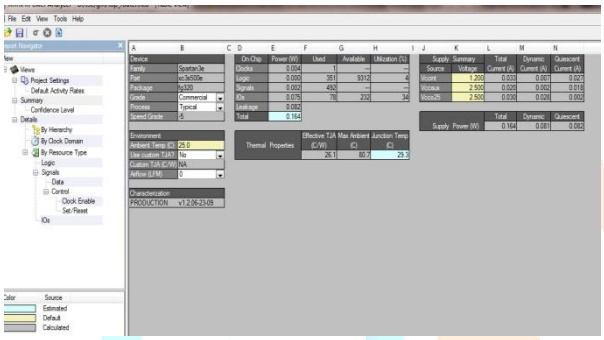

Fig10: Power analysis of the project.

V. CONCLUSION

The reconfigurable router need to use in NOC is arranged in the present work. The primary point of the arranged configuration is to accomplish High execution of the framework and Low power utilization. Router is the most fundamental part of NOC. The proposed router plan has 4 channels viz West, East, North and South. An individual channel contains FIFO support for information stockpiling reason and multiplexers to have the control on information inputs and yields. In this work, Stack profundity of FIFO buffer is thought to be 16, where each of the memory areas can store 8 bit of information. 5 multiplexers are available in each of the channel. Among 5 multiplexers,2 of them are utilized for controlling the information and information yield signals. While remaining 3 multiplexers are utilized to control the read and compose operations of FIFO. The proposed router outline is actualized utilizing Verilog HDL. Modelsim is utilized for reproduction and blend is done utilizing Xilinx ISE Design Suite 14.5. Xilinx SPARTAN-6 FPGAs is utilized for union of reconfigurable router. Complete power computation is done utilizing Xpower Analyzer tool,after the reproduction and combination of the proposed router. The entire power portrayed by the router structure is 20mw. Around 6mw of power has been decreased in this configuration. In this manner the diminished power is of around 14mw ,from the proposed router plan, which is appeared in underneath table.

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