BIT SWAPPING LFSR AND SCAN CHAIN ORDERING

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Abstract: This paper presents a novel low-transition linear feedback shift register (LFSR) that is based on some new observations about the output sequence of a conventional LFSR. The proposed design, called bit-swapping LFSR (BS-LFSR), is composed of an LFSR and a 2 times 1 multiplexer. When used to generate test patterns for scan-based built-in self-tests, it reduces the number of transitions that occur at the scan-chain input during scan shift operation by 50% when compared to those patterns produced by a conventional LFSR. Hence, it reduces the overall switching activity in the circuit under test during test applications. The BS-LFSR is combined with a scan-chain-ordering algorithm that orders the cells in a way that reduces the average and peak power (scan and capture) in the test cycle or while scanning out a response to a signature analyzer. These techniques have a substantial effect on average- and peak-power reductions with negligible effect on fault coverage or test application time.

Keywords: LFSR, Scan chain, Bit swapping, ,scan chain ordering, BS-LFSR

Introduction:

The main drawback of the existing algorithms is that they aim only to reduce the average-power consumption while loading a new test vector, and they ignore the power consumption that results while scanning out the captured response or during the test cycle. Furthermore, some of these techniques may result in lower fault coverage and higher test application time. In our existing Architecture it has more switching activity, which makes the CUT to work with more switching transitions. Since the input transitions are more this will leads to more switching transition inside the chip which will lead to more power consumption.

Propsed Approach for BS-LFSR:

The proposed BS-LFSR for test-per-scan BISTs is based upon some new observations concerning the number of transitions produced at the output of an LFSR.

Lemma 1: Each cell in a maximal-length n-stage LFSR (internal or external) will produce a number of transitions equal to 2n−1 after going through a sequence of 2n clock cycles.

Lemma 2: Consider a maximal-length n-stage internal or external LFSR ($n > 2$). We choose one of the cells and swap its value with its adjacent cell if the current value of a third cell in the LFSR is 0 (or 1) and leave the cells un swapped if the third cell has a value of 1 (or 0). T this arrangement for an external LFSR (the same is valid for an internal LFSR). In this arrangement, the output of the two cells will have its transition count reduced by T saved = 2(n−2) transitions. Since the two cells originally produce 2 × 2n−1 transitions, then the resulting percentage saving is T saved% = 25%.

Lemma 3: For an external n-bit maximal-length LFSR that implements the prime polynomial xn + x + 1 as shown in Fig. 7.1, if the first two cells (c1 and c2) have been chosen for swapping and cell n as a selection line,

then o2 (the output of MUX2) will produce a total transition savings of 2n−2 compared to the number of transitions produced by each LFSR cell, while o1 has no savings (i.e., the savings in transitions is concentrated in one multiplexer output, which means that o2 will save 50% of the original transitions produced by each LFSR cell).

In this scan-chain-ordering algorithm, some cells of the ordered scan chain using the algorithm will be reordered again in order to reduce the peak power which may result during the test cycle. This phase mainly depends on an important property of the BS-LFSR. This property states that, if two cells are connected with each other, then the probability that they have the same value at any clock cycle is 0.75. (In a conventional LFSR where the transition probability is 0.5, two adjacent cells will have the same value in 50% of the clocks and different values in 50% of the clocks; for a BS-LFSR that reduces the number of transition of an LFSR by 50%, the transition probability is 0.25, and hence, two adjacent cells will have the same value in 75% of the clock cycles.)

The steps in this algorithm are as follows:

1) Simulate the CUT for the test patterns generated by the BS-LFSR.
2) Identify the group of vectors and responses that violate the peak power.
3) In these vectors, identify the cells that mostly change their values in the test cycle and cause the peak-power violation.
4) For each cell found in step 3 identify the cells that play the key role in the value of this cell in the test cycle.
5) If it is found that, when two cells have a similar value in the applied test vector, the concerned cell will most probably have no transition in the test cycle, then connect these cells together. If it is found that, when two cells have a different value, the cell under consideration will most probably have no transitions in the test cycle, then connect these cells together through an inverter.

It is important to note that this phase of ordering is done when necessary only, as stated in step 2 of the algorithm description that the group of test vectors that violates the peak power should be identified first. Hence, if no vector violates the peak power, then this phase will not be done. In the worst case, this phase is performed in few subsets of the cells. This is because, if this phase of ordering is done in all cells of the scan chain, then it will destroy the effect of algorithm found and will substantially increase the computation time.

RESULTS AND DISCUSSION

A low-transition TPG that is based on some observations about transition counts at the output sequence of LFSRs has been presented. The proposed TPG is used to generate test vectors for test-per scan BISTs in order to reduce the switching activity while scanning test vectors into the scan chain. Furthermore, a novel algorithm for scan-chain ordering has been presented. When the BS-LFSR is used together with the proposed scan-chain-ordering algorithm, the average and peak power is substantially reduced. The effect of the proposed design in the fault coverage, test-application time, and hardware area overhead is negligible.

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