Applications of XOR Gate Using Ternary Logic

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Abstract: Ternary Logic has been the topic of interest of many researchers due to its merits over common binary logic. Much of the previous work on ternary logic is purely theoretical nature. Due to the problems with the binary logic to reduce interconnect complexity and reduce chip area, it is giving motivation for the investigation of many hardware implementations of Ternary logic. Work on hardware implementation of three value devices has been more recent. Three types of Ternary logic inverters i.e. STI, PTI and NTI are implemented. With the increased number of logic states, bit handling capability of ternary logic circuits will increase. XOR gate is a digital logic gate that has a wide range of applications in digital systems. In this paper, various operations performed by TERNARY computers are implemented using XOR gate like modulo 2 addition, magnitude comparator, and controlled inverter etc.

IndexTerms **– Ternary Logic, XOR gate, PTI, STI, NTI**

I. INTRODUCTION

In the second half of the 20th century Russian SETUN and SETUN – 70 computers based on ternary logic were developed at the Moscow State University. Ternary logic is an effective approach over the default binary logic design technique because it allows to define one or more voltage levels which is 0, Vdd / 2 and Vdd. It allows a circuit to be simple in design and energy efficient due to its property of reduction in circuit overhead such as interconnects and chip area. The main advantage of ternary logic is its computing power and lower demand for memory. However, electronic implementation of ternary logic gates is not as straight forward as in the case of binary logic gates.

II. TERNARY LOGIC GATES

Ternary logic gate is a logic gate that uses ternary signals. Ternary logic circuits can be implemented in current mode and voltage mode. In voltage mode, distinct voltage levels are represented as logic levels. The voltage mode signals are again classified into two types: balanced form (-1, 0, +1) or unbalanced form (0, 1, and 2). Ternary logic can be implemented by using three basic gates i.e. inverter, NAND and NOR gates. The ternary inversion can be implemented in 3 ways: 1. Simple ternary inversion 2. Positive ternary inversion and 3. Negative ternary inversion. The functionality of ternary inverter is shown below:

Table 1Truth table for ternary inverter

in	out		
	STI	PTI	NTI
0	2	2	2
1	1	2	0
2	0	0	0

2.1 Simple Ternary Inverter (STI)

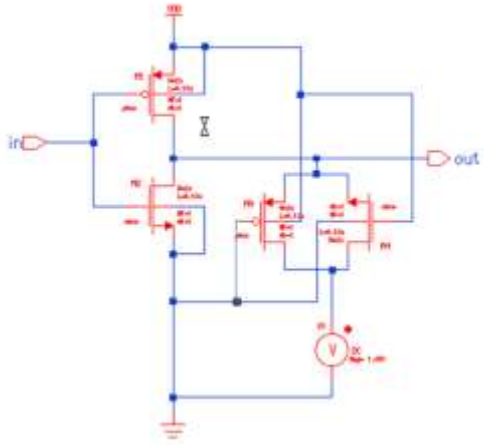

Figure 1: STI Inverter

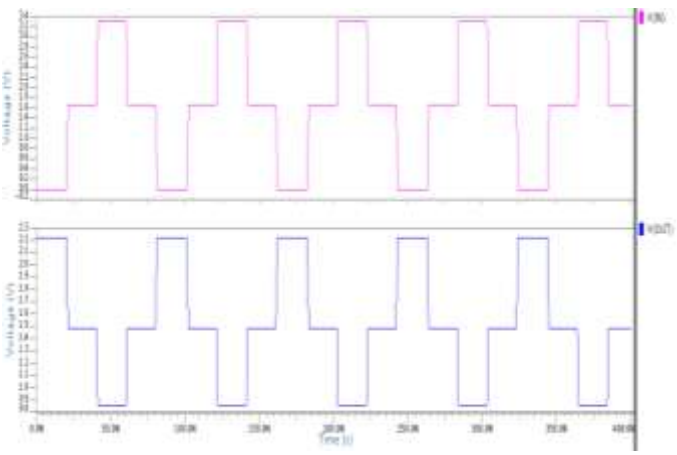

Figure 2: Output of STI Inverter

Fig 2.1 shows the simple ternary inverter. Simple CMOS binary inverter can be extended to ternary inverter by connecting a high performance transmission gate at the output. The transmission gate is always in ON state. CMOS inverter produces high(2) for low input(0) and produces low(0) for high input(2). But for middle level(1), both the transistor are near cut-off. So, the transmission gate pulls the output to the voltage(1) applied at the input of transmission gate.

2.2 Positve Ternary Inverter (STI)

PTI produces low output(0) for high(2) input and produces high(2) for the remaining two levels of input. A PMOS pass transistor is connected at the output. The PMOS pass transistor is permanently in ON state and pulls the output to high state when when both the input transistors are near cutoff.

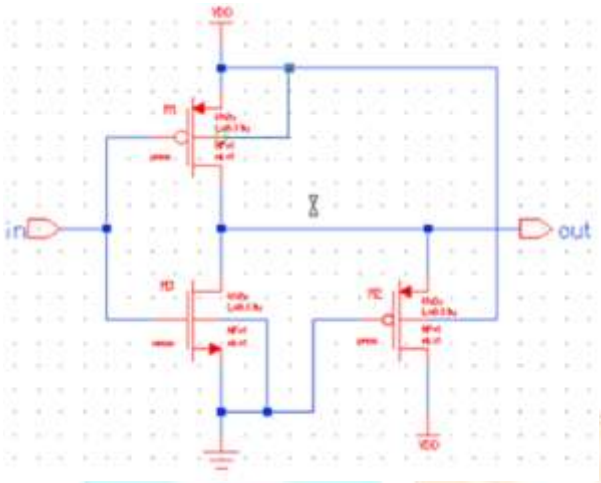

Figure 3: PTI Inverter

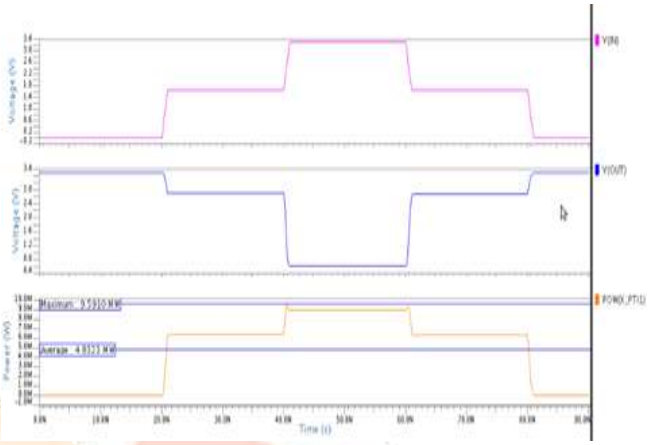

Figure 4: Output of STI Inverter

2.3 Negative Ternary Inverter (NTI)

NTI produces high output(2) for low(0) input and produces low(0) for the remaining two levels of input. An NMOS pass transistor is connected at the output. The NMOS pass transistor is permanently in ON state and pulls the output to low(0) state when both the input transistors are near cutoff.

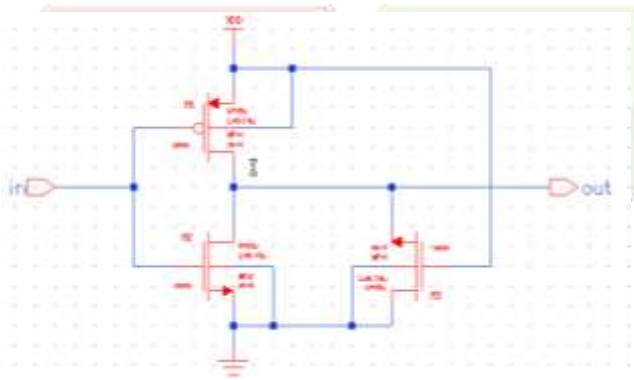

Figure 5: NTI Inverter

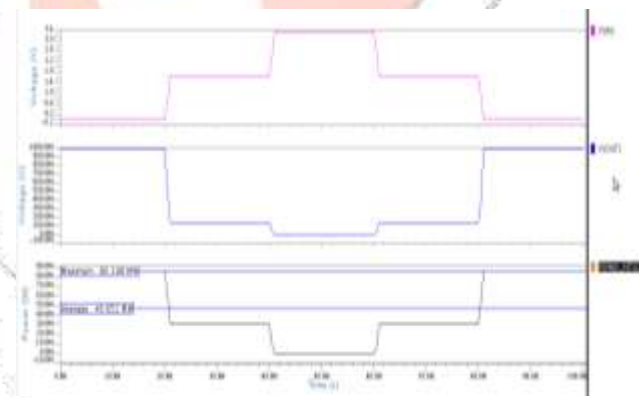

Figure 6: Output of NTI Inverter

III. UNIVERSAL TERNARY LOGIC GATES

Like Binary NAND and NOR gates, ternary NAND and NOR gates can also be used to implement any logic. Here Simple ternary NAND and NOR gates are implemented by connecting a transmission gate at the output. Standard or Simple ternary gates are represented by a dot in the gate symbol. Ternary EX-OR gate can be designed using Ternary NAND gate. Table2 shows the functionality of ternary logic gates.

Table 2 Truth table for ternary NAND, NOR and EX-OR gates

A	B	NAND	NOR	EX-OR
0	0	2	2	0
0	1	2	1	1
0	2	2	0	2
1	0	2	1	1
1	1	1	1	1
1	2	1	0	1
2	0	2	0	2
2	1	1	0	1
2	2	0	0	0

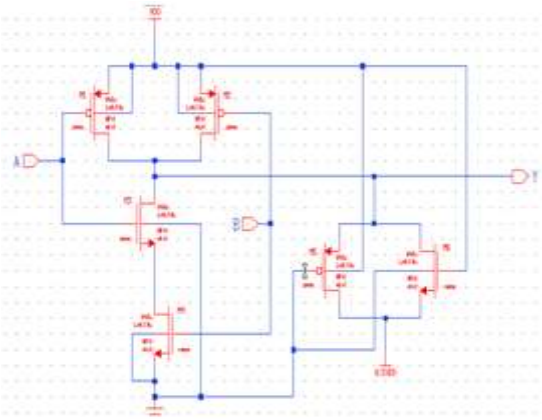

Figure 7: ST-NAND Gate

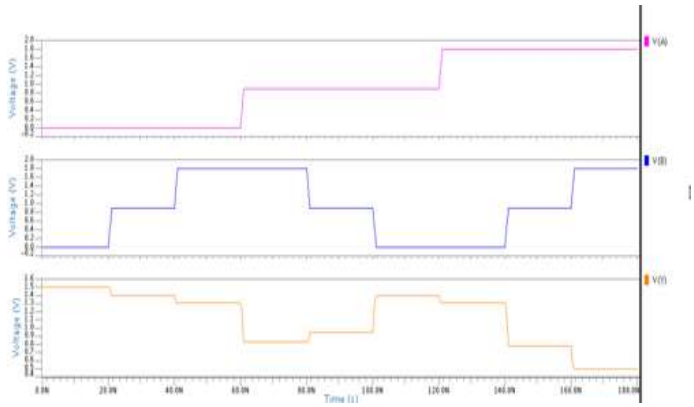

Figure 8:Output of ST-NAND Gate

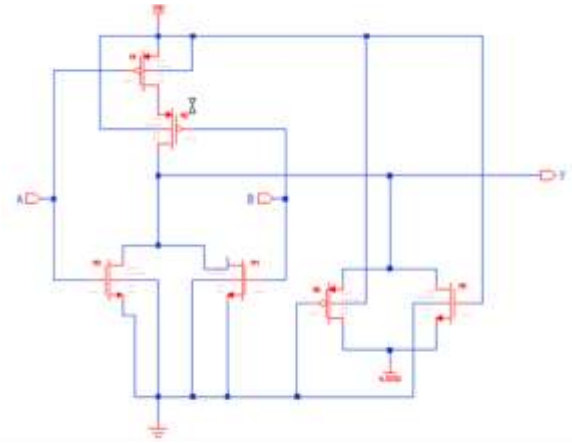

Figure 9: ST-NOR Gate

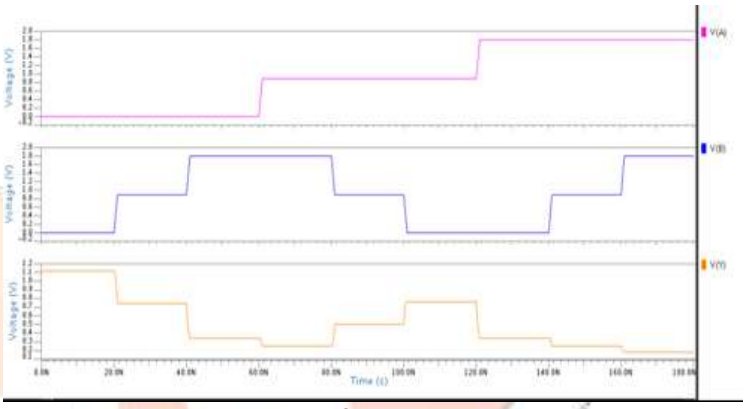

Figure 10:Output of ST-NOR Gate

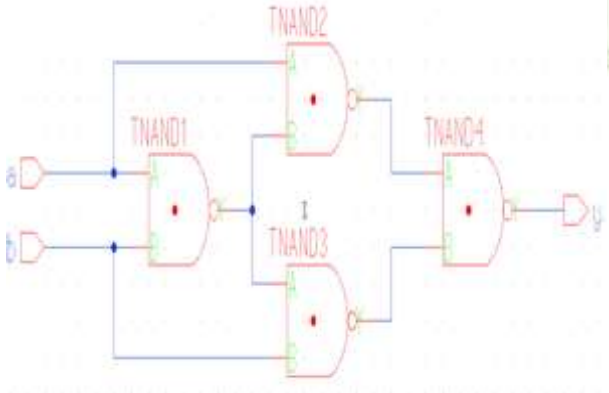

Figure 11: Ternary EX-OR Gate

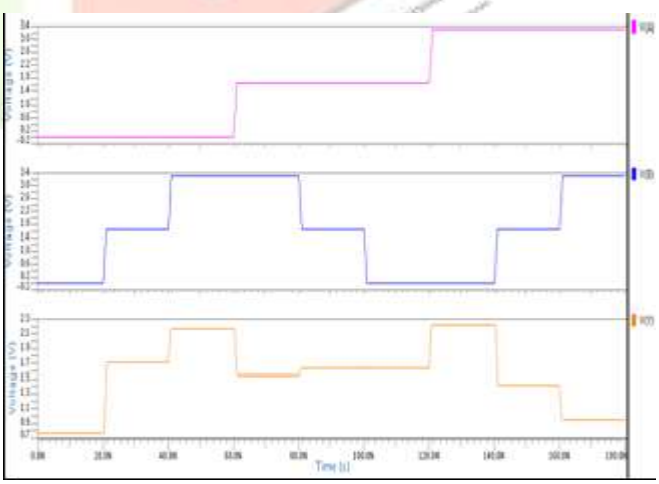

Figure 12:Output of ternary EX-OR Gate

IV. RESULTS OF VARIOUS APPLICATIONS OF TERNARY EX- OR GATE

4.1 Ternary Controlled Buffer / Inverter

One of the practical application of EX-OR gate in transmitting data is Buffer / Inverter. Here EX-OR gate can be used as Inverter or Buffer by using a Control input. When the control input is enabled it acts as an Inverter otherwise it acts like a data Buffer. Table 3 shows the functionality of the ternary controlled Buffer/Inverter.

Table 3 Truth table for ternary Controlled Buffer/Inverter

Control input	X	Y	Z
0	A	B	C
1	$\overline{A}$	$\overline{B}$	$\overline{C}$

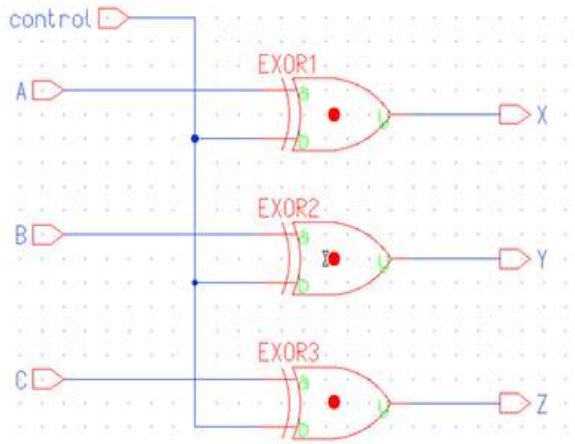

Figure 13: Ternary Controlled Buffer / Inverter

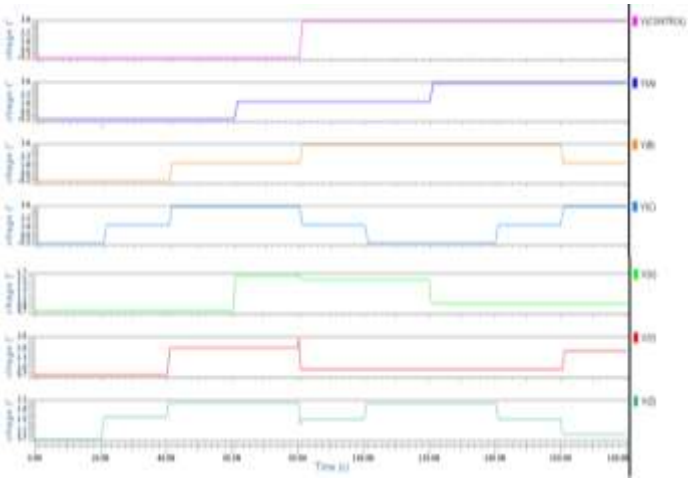

Figure 14: Output of Ternary Controlled Buffer / Inverter

4.2 Ternary 1-bit Comparator

In digital systems, comparison of magnitude of data is very essential. Here1-bit comparator is designed using ternary logic. In this logic the data can be compared for three levels i.e., low (0), intermediate (1) and high (2). Table 4 shows the functionality of the ternary 1-bit comparator.

Table 4 Truth table for ternary 1-bit Comparator

A	B	A eq B	A gt B	A lt B
0	0	2	0	0
0	1	1	0	1
0	2	0	0	2
1	0	1	1	0
1	1	1	1	1
1	2	1	0	1
2	0	0	2	0
2	1	1	1	0
2	2	2	0	1

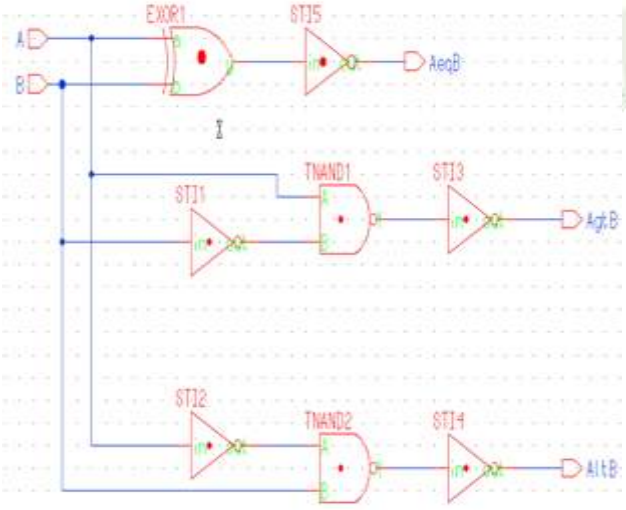

Figure 15: Ternary 1-bit Comparator

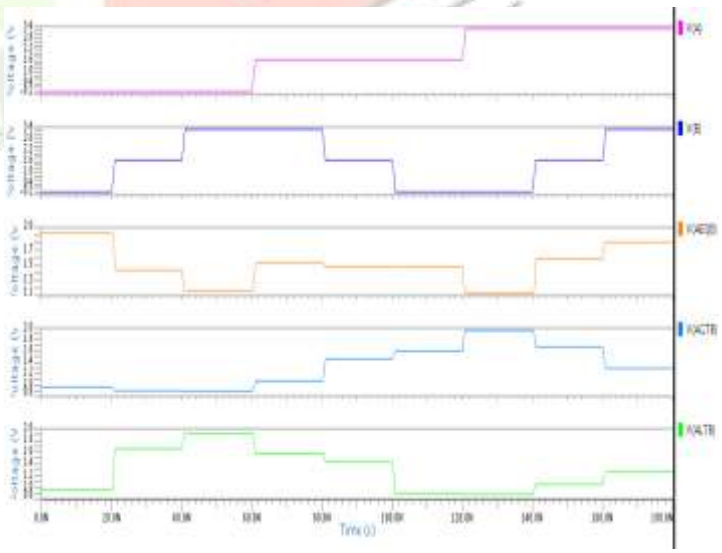

Figure 16: Output of Ternary 1-bit Comparator

4.3 Ternary Half Adder

The gate which performs modulo sum operation with including carry is known as EX-OR gate. The half adder generates sum of two bits. So to implement half adder EX-OR gate can be used to generate sum output. Table 5 shows the functionality of the ternary half adder.

Table 5 Truth table for ternary Half Adder

A	B	CARRY	SUM
0	0	0	0
0	1	0	1
0	2	0	2
1	0	0	1
1	1	1	1
1	2	1	1
2	0	0	2
2	1	1	1
2	2	2	0

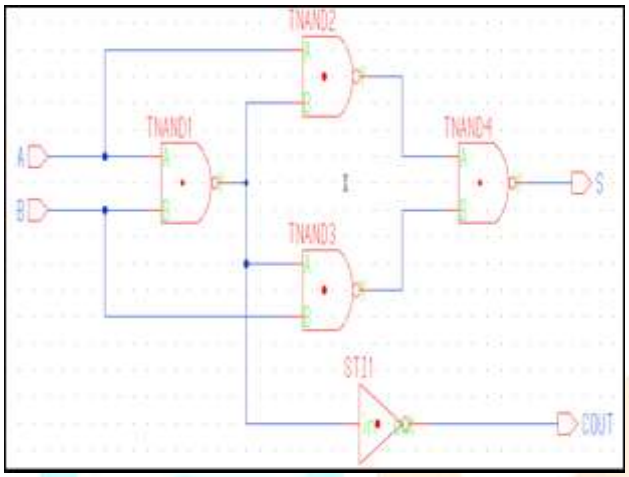

Figure 17: Ternary Half Adder

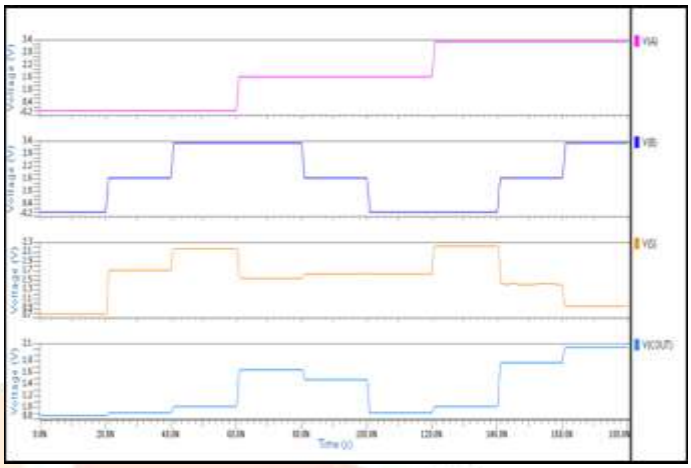

Figure 18: Output of Ternary Half Adder

IV. CONCLUSION

In this paper, we designed three types of ternary inverters like STI, PTI and NTI using unbalanced logic levels. Universal ternary gates also designed and simulated. Then, various applications of Exclusive-OR gate using ternary logic also implemented. All the designs are designed using Mentor Graphics HEP-2, 130nm technology. All the simulations are performed using ELDO simulator. The design process for combinational logic circuits can be extended to implement sequential logic circuits also. By using ternary logic we can transmit more information compared to conventional binary logic using less number of logic elements, thereby interconnect density can be reduced. Area of the design can also be reduced. It has specialized applications in error correcting codes, fuzzy logic etc.

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