Total Ionising Dose Effects on HfO_2 and Al_2O_3 Gate Oxide SOI FinFET

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Abstract: The total ionising dose (TID) effects on different gate oxide used in silicon on insulator (SOI) FinFET are investigated in this paper. The device structure under consideration shows a three-dimensional (3-D) architecture of Silicon on Insulator (SOI) 30nm n-channel FinFET with a high-k hafnium oxide (HfO2) and aluminum oxide (Al2O3) as gate electrode. To test the influence of TID on the FinFET device the 3-D simulations were performed in Visual TCAD using radiation dedicated code for different gate oxides. The TID effects modify the electrical properties leading to deterioration of the device and failure of the systems associated with them. The influence of dose rate on the build-up of fixed charge in the gate oxide region and the interface charge at the oxide-semiconductor interface was analyzed and observed its impact was observed on the device characteristics. It has been found that oxide trapped charge density is higher than interface trapped charge density. As a result of TID, there is an increase in the leakage current and transconductance after irradiation. It is observed that there is a threshold voltage shift with increasing dose of ionizing radiation for both the gate oxide materials.

Keywords: *Silicon on insulator (SOI), total ionizing dose (TID), FinFET, fixed charge, interface charge, threshold voltage shift.*

I. INTRODUCTION

Silicon-On-Insulator (SOI) technologies are becoming increasingly popular for use in commercial applications. To meet the ITRS specifications, multiple gate devices are an excellent option. Hence, it becomes imperative to study the radiation characteristics of the devices used in nuclear environments and space applications. Considerable attention must therefore be given to semiconductor devices as it is exposed to radiation of very high intensity. Total Ionizing Dose effect is one of the prominent effects on irradiated semiconductor devices. There is well-documented research to prove deterioration in device characteristics because of incoming radiation dose on the device. These deteriorations have reduced with modern SOI and multi-gate technologies. SOI devices have been shown to have better immunity to a total ionizing dose of radiation as compared to their bulk silicon counterparts [1]. But they are not completely immune to Total Ionizing Dose (TID) effects and its response is more complicated than bulk devices [2]. As new device technologies are emerging, it becomes necessary to study the response of the device to irradiation. In this paper, the effects of TID on a 30nm gate SOI FinFET are investigated. Radiation affects thin gate oxide as well as buried oxide layer which degrades the device characteristics. The device parameters such as ON current, threshold voltage, leakage currents and transconductance change as a function of the total dose of radiation. TID effects are strongly influenced by geometry of the device, method of fabrication, dose rate, biasing voltage, and temperature after the irradiation [3, 4]. TID effect is due to continuous accumulation of trapped charge in insulating layers and inversion channel formed along the top and sidewall of the fins [5]. Ultra-small SOI devices exhibit significant change in device characteristics due to TID exposures.

II. MECHANISM OF RADIATION

Broadly, radiation is split into two types, particle radiation and photon radiation. Particle radiation comprise of charged particles such as protons, electrons, alpha (α) particles, ions and neutrons. Particle radiation also activates ionization process, hence excess carriers are generated within a semiconductor device and material. Photon radiation compose of gamma (γ) rays and x-rays. The radiation effects that deal with ionization induced by γ rays is called total ionising dose. TID is measured in terms of the radiation absorbed by the material and it's given in rad (radiation absorbed dose) or gray (Gy) [6-9]. A rad is the measure of radiation which deposits 100 ergs of energy per gram of material.

SOI FinFET structure has been the object of intensive research when exposed to radiation. The most susceptible part of SOI FinFET structure to total dose response are the gate oxide, buried oxide (BOX) and the sidewall of the fin. The dominant physical processes which effect the device characteristics, is electron hole pair generation in radiation environment [3]. The charge pair volume density generated per rad in oxide material is 8.1 x 1012 pairs/cm3. The electrons are rapidly swept of the oxide within a few picoseconds due to high mobility. But still a fraction of electrons recombines with the holes in that first picoseconds. The recombination process depends on the magnitude of the electric field, which separate the electron-hole pairs, and the initial line density of charge pairs created by the incident radiation. The line density is inversely proportional to the spacing between electron hole pairs. It also depends on linear energy transfer and hence is a function of incident particle type and energy. The holes, which escape initial recombination, are relatively immobile and remain near their point of generation, hence trapped. The generation of traps in the gate oxide, BOX and the interface traps at the sidewalls of the fin, influences the electrical characteristics of an irradiated FinFET device. Positive charges can be trapped thereby changing the overall mobility and threshold voltage of the device under study. It is clear that when a device is exposed to radiation the three damage mechanisms occur which are: (1) Net surface state

density is increased; (2) a decrease in substrate resistivity; and (3) Carrier mobility is decreased in the channel. As a result, drain current reduction, mobility, transconductance and gain decrease and threshold voltage shift occurs.

III. FinFET Device Description

The Gds2mesh tool was used to build the 3D device structure model and mesh grid of an n-channel FinFET transistor. A 3-dimensional structure of 30nm n-channel Fully Depleted Silicon on Insulator (FDSOI) FinFET device simulated in Visual TCAD with shorted gate (SG) shown in **Fig.1**. It is a self-aligning process which replaces conventional CMOS devices in nanometer regime. The technology parameters and supply voltages used for 30 nm node devices simulations are according to International Technology Roadmap for Semiconductors (ITRS 2013). The device structure is optimized and designed for 30 nm gate length with I_{off} as one nanoampere as per ITRS requirements. The process parameters employed in these simulations with following specifications: channel doping (Na) = 1017 cm-3, peak of the doping profile (N_{sd}) =3 x 1020 cm-3, gate length (L_g) =30nm, Thickness of fin (T_{fin}) =20nm, Height of the fin (H_{fin}) =50nm, Fin Width (W_{fin}) =120nm, Metal (Tungsten) work function (Φ) =4.7eV, SOI layer thickness = 400nm.The electrostatics of conducting channel is controlled by the SG which forms the body of the device [3]. The thin channel region (body) stands vertically like the fin of a fish surrounded by the source and drain regions. As the gate oxide thickness is scaled, it is limited by gate tunneling leakage, hot electron effect and DIBL. Hence to overcome these limitations silicon dioxide (SiO2) is replaced with a high-κ dielectric such as hafnium oxide (HfO2). Where the hafnium oxide (HfO2) high-κ dielectric (k=22) gate wraps around the device n-type body, which has a height H_{fin} and thickness T_{fin} [10]. The high-κ gate dielectric increases the barrier width between the gate and the channel without increasing the gate capacitance and yielding the same threshold voltage. The value of Equivalent Gate oxide thickness (EOT) (T_{ox}) =1nm is calculated using the following formula given in **equation 1.**

$$EOT_{HK} = K_{SiO2}\frac{t_{high-k}}{K_{high-k}} \qquad (1)$$

IV. Result and Discussion

The effect of TID were carried out on a computer model of the 3D FDSOI n-channel FinFET device structure using Visual TCAD device simulator. Current-voltage characteristics at room temperature were carried out before and after irradiation of gamma rays. The simulations were carried out on two different gate oxide material hafnium oxide HfO_2 (k = 22) and aluminum oxide Al_2O_3 (k = 9.3). In all cases, the total dose was varied from 100krad to 1M varied in steps and the dose rate was maintained constant at 10rad/s. The changes in the I_d-V_{gs} characteristics, threshold voltage, transconductance, oxide trapped charge densities and interface trapped charge densities were measured, analyzed and reported.

4.1 I_d-V_{gs} Characteristics

The TID effect on HfO_2 and Al_2O_3 gate oxide of SOI FinFET was simulated. The device (I_d-V_{gs}) curves, transconductance (g_m) and threshold voltage (V_{TH}) were measured before and after exposure with various doses of gamma radiation to produce significant changes in the device. The drain to source voltage (V_{ds}) was constant at 50mV for threshold voltage extraction. The gate voltage sweep was taken from 0V to 1V in steps of 0.1V.

A conducting channel is formed between the source and drain, when appropriate gate voltage is applied so that current flows when the device is turned on. When FinFET devices are exposed to gamma radiation, these high energy electrons deposit energy into the device through electronic excitations. Hence ionization and displacement of atoms occur during the irradiation process. The

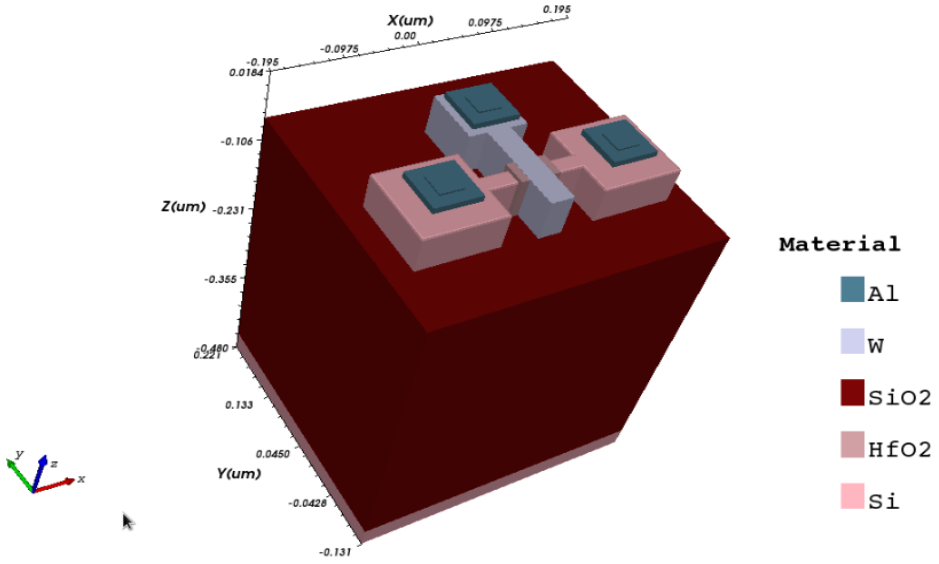


Figure 1 3-D Schematic view of high-k 30nm FinFET device structure considered for numerical simulation using Visual TCAD. radiation induced electron-hole pairs quickly undergo recombination and are not available for any further radiation effect, and some of the positively charged holes make slow dispersive transport towards the Si/SiO_2 interface where they are trapped in deep hole traps. Thus, some of the holes are captured by trapping sites typically located within the gate oxide, BOX and the interface traps at

the sidewalls of the fin, which plays a very important role in determining the device performance. A shift in the threshold voltage (that is, a change in the voltage which must be applied to turn the device on) is caused due to radiation-induced trapped charges, which is built up in the gate oxide. If this shift is large enough, the device cannot be turned off even at zero volts applied. **Figure 2** shows the I_d-V_{gs} curves of virgin and gamma irradiated devices for HfO_2 and Al_2O_3 gate oxide material. An increase in drain current

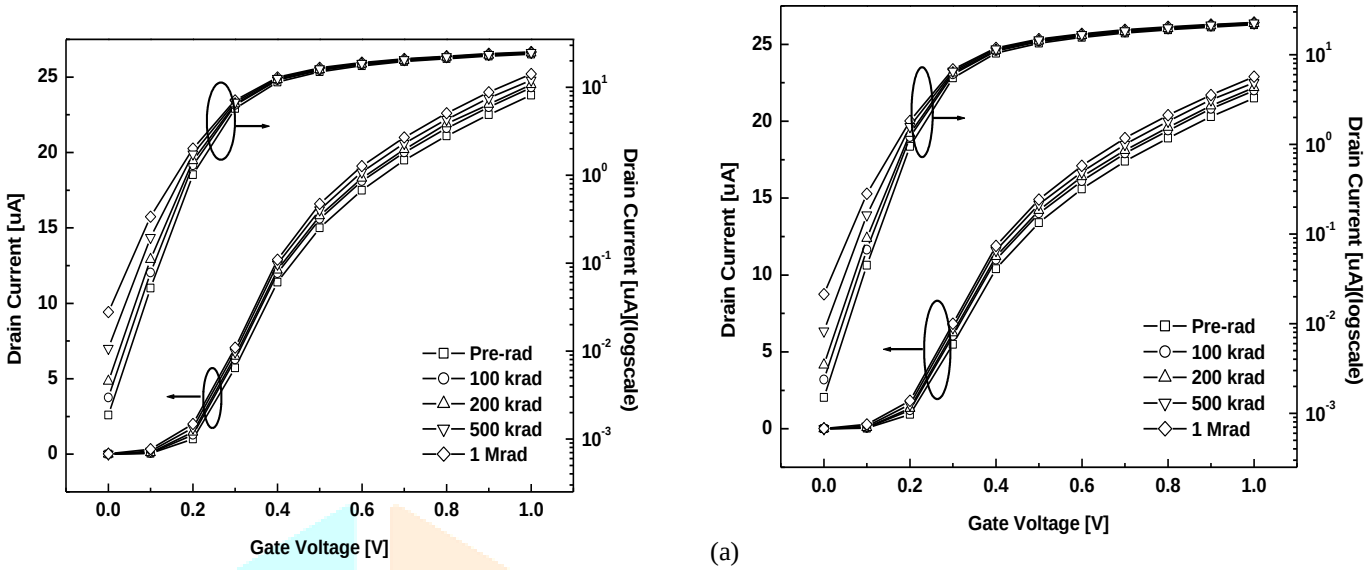


Figure 2 I_d-V_{gs} characteristic of gamma irradiated of 30nm n channel SOI FinFET device for (a) HfO_2 and (b) Al_2O_3 gate oxide material at V_{ds} =50mV.

An influential analog performance parameter of FinFET device is transconductance (g_m) which is directly linked with the drain current. The transconductance of the FinFET device is defined as the rate of increase in drain current per unit increase in gate voltage at fixed drain voltage. The mobility of the carriers determines peak transconductance in the n-channel. The carriers in the channel are scattered due to irradiation, and thereby degrade transconductance. From the **Fig. 3** it is observed that transconductance increases with increase in total dose rate up to the threshold voltage. Once the device is in conduction, the lines tend to overlap.

The threshold voltage of the virgin device was found to be 227.85mV and 231.18mV for HfO_2 and Al_2O_3 gate oxide material of 30nm n- channel SOI FinFET device. For the irradiated device the threshold voltage is shifted to 188.52mVand 194.30mV when it is exposed to a gamma dose of 1Mrad. From the **Fig. 4** it is observed that the shift in threshold voltage is due to accumulation of oxide and interface trapped charges. The change in threshold voltage shift is higher for HfO_2 than Al_2O_3 while the absolute value of the threshold voltage is higher for Al_2O_3 than HfO_2. Thus, device engineer should structure to prevent shift of the threshold voltage for a higher dose rate. The values are tabulated for threshold voltages and threshold voltage shift in **Table 1** for virgin and irradiated 30nm FinFET device for HfO_2 than Al_2O_3 gate oxide.

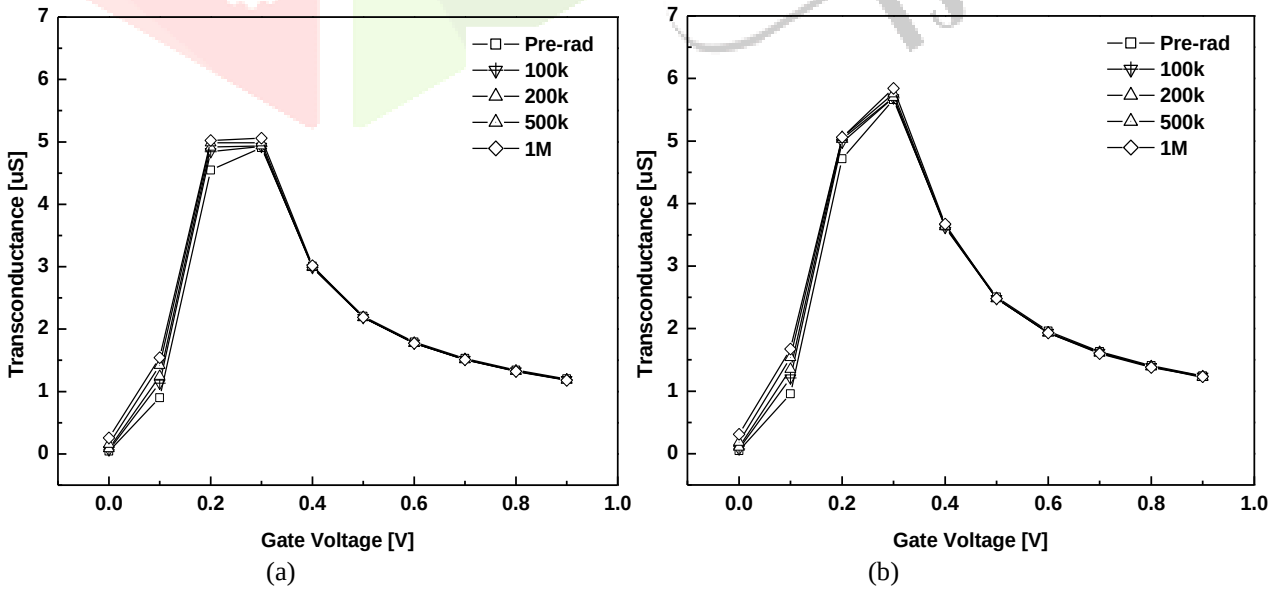
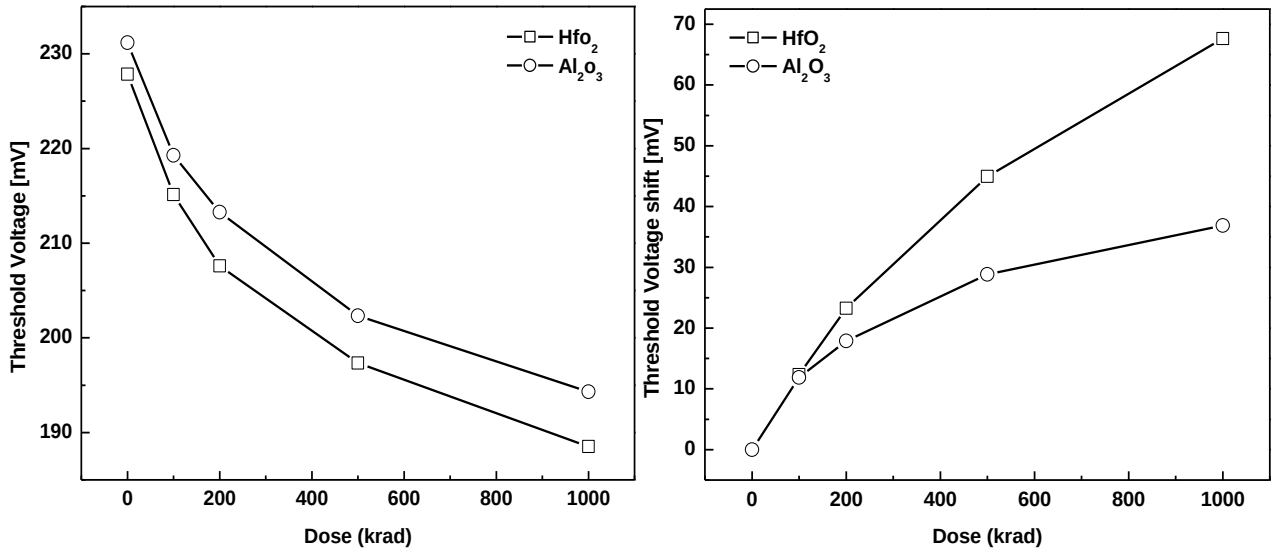


Figure 3 Transconductance of gamma irradiated 30nm n channel SOI FinFET device for (a) HfO_2 and (b) Al_2O_3 gate oxide material at V_{ds} =50mV.

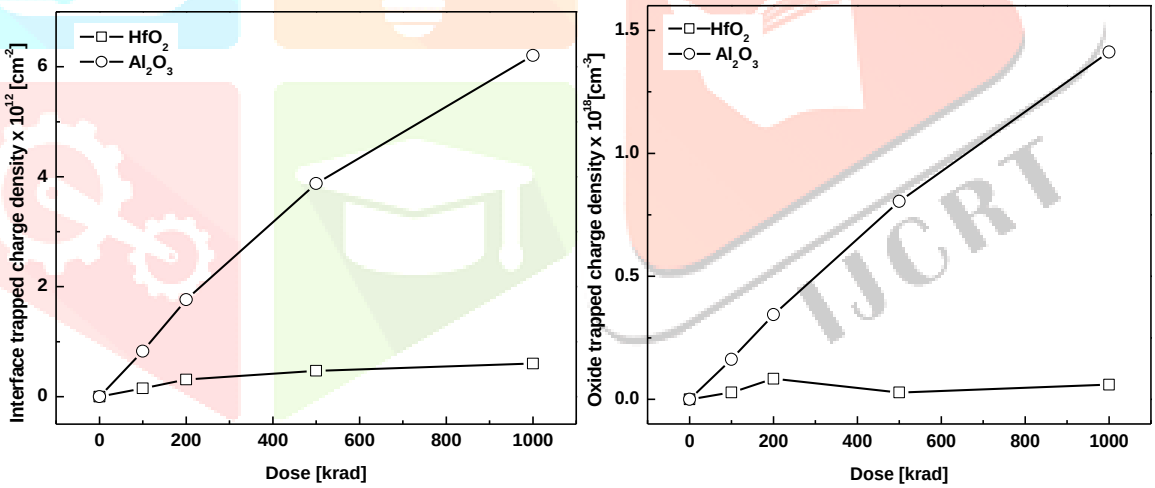


(a) (b)

Figure 4 (a) Threshold voltage and (b) Threshold voltage shift as a function of dose rate during irradiation of 30nm n channel SOI FinFET device for HfO_2 and Al_2O_3 gate oxide material at V_{ds} =50mV

4.2 Oxide and Interface Trapped Charges Density

As shown in Fig.4 the threshold voltage shift due to oxide and interface trapped charges for various doses of gamma radiation has been discussed in previous section. Ionizing radiation leads to charge trapping in insulating materials. It is clear that the oxide charge density is large compared to interface charge density, and hence the voltage shift due to oxide trapped charges becomes dominating. The simulated value of threshold voltage, threshold voltage shift, interface trapped charge density, and oxide trapped charge density for virgin and gamma irradiated device are summarized in Table I for HfO_2 and Al_2O_3 gate oxide material of 30nm n- channel SOI FinFET device. **Figure 5** shows the variation in oxide and interface trapped charges for various gamma doses.



(a) (b)

Figure 5 (a) Interface and (b) Oxide trapped charge density as a function of various gamma doses of 30nm n channel SOI FinFET device for HfO2 and Al_2O_3 gate oxide material.

Table I Threshold voltage shifts and trapped charge densities of 30nm n-channel SOI FinFET device for (a) HfO_2 and (b) Al_2O_3 gate oxide material.

Gate Oxide	γ-Dose	V_{TH} (mV)	Δ V_{TH} (mV)	N_{it}(cm^{-2})	N_{ox} (cm^{-3})
Hafnium oxide (HfO_2)	Virgin	227.85	-	0.0	0.0
	100 Krad	215.13	12.35	1.528×10^{11}	2.818×10^{16}
	200 Krad	207.60	23.27	3.094×10^{11}	8.362×10^{16}
	500 Krad	197.34	44.95	4.704×10^{11}	2.789×10^{16}
	1Mrad	188.52	67.65	5.996×10^{11}	5.936×10^{16}
Aluminum oxide (Al_2O_3)	Virgin	231.18	-	0.0	0.0
	100 Krad	219.29	11.89	8.25×10^{11}	1.628×10^{16}
	200 Krad	213.28	17.9	1.762×10^{11}	3.443×10^{16}
	500 Krad	202.32	28.86	3.875×10^{11}	8.047×10^{16}
	1Mrad	194.30	36.88	6.204×10^{11}	1.412×10^{16}

V. CONCLUSION

The 30nm n channel SOI FinFET device for HfO_2 and Al_2O_3 gate oxide material were analyzed for total dose response under different gate bias during irradiation at room temperature. The various performance parameters of the device were changed due to TID effect. The main degradation mechanism of gamma irradiated device is due to increase in trapped charge density. The oxide trapped charge was found to be higher compared to interface trapped charge. The threshold voltage for the irradiated FinFET device decreased significantly and it was observed that as doses of radiation increases it causes more degradation. The change in threshold voltage is higher for HfO_2 than Al_2O_3 gate oxide materials. For a low total dose, the threshold shifts to a similar degree but as the total dose increases, HfO_2 shows a higher shift in the threshold voltage even though the oxide thickness is higher for Al_2O_3. This strongly suggests that Al_2O_3 is a better dielectric for use in gate oxides when compared with HfO_2 in the face of radiation. The TID effect seriously degrades the device performance.

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