INTEGRATED AMPLIFIER TOPOLOGIES FOR ECG DEVICE

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Abstract: Different techniques for designing CMOS integrated amplifier for electrocardiogram (ECG) device is presented in this paper. It covers three design techniques namely Instrumentation Amplifier (IA), two stage op-amp, and tristate amplifier. After discussing the design techniques, they are compared for parameters like gain, CMRR, technology used, phase margin, unity gain bandwidth (UGB), phase margin, and power dissipation. The best utilizable topology for the ECG device is concluded in this work.

Index Terms **– CMRR, UGB, Instrumentation Amplifier**

I. INTRODUCTION

Current research shows that emotional or psychological stress may increase blood pressure and cholesterol which may lead to heart disease. Every year there are about 10-12 million deaths worldwide and around 2.4 million deaths in India due to heart disease [6-IMA]. As a result several medical devices have been manufactured to examine heart disease. The device that detects the rhythm of heart beat is called electrocardiogram (ECG) and graph produced by it is called electrocardiograph.

In considering the physiological signals extracted from human bodies, the amplitude of an electrocardiographic (ECG) signal is usually less than 100 µV. Such value is very weak as compared to the noise floor and imperfection of the commonly used operational amplifiers (Op-Amps). An instrumentation amplifier (IA) is usually employed to achieve the required performances[1].

Bio-potential signals are important to physicians for diagnosing medical conditions in patients. Bio-potential signals are very weak signals and in the presence of stronger common mode signals. Amplitudes and spectral ranges of some important Bio-potential signals completely cover the area from 10^{-6} V to almost 1 V and from dc to 10 kHz [4]. The ability of an amplifier to amplify required differential signals by rejecting unwanted common mode signals is known as common mode rejection ratio (CMRR) [4]. The ability of an amplifier to amplify required differential signals by rejecting unwanted common mode signals is known as common mode rejection ratio (CMRR) [4]:

... (1)

Where, is differential gain

is common mode gain

An op-amp has several parameters: based on the applications each of the parameter has its own significance. Among them a high voltage gain of greater than 80dB and high CMRR of greater than 90dB is preferred for Bio-medical applications [1]. These kinds of amplifiers are called as Biopotential amplifiers.

It has become utmost necessary to design an amplifier with high gain and high CMRR for biomedical application. Biological signals have very low level thus they have to be amplified properly before delivering to subsequent stages. Conventionally, Instrumentation amplifiers are used for the purpose of high CMRR [3]. Various amplifier topologies have been proposed for the purpose of Bio-potential signal acquisition targeting low power and high CMRR specifications. Single Op-amp topologies such as [4] have the advantage of lower power consumption. This report briefs the design of a two stage cascade of a Folded-cascode section in the first stage followed by a differential amplifier with a PMOS load. Common mode feedback (CMFB) technique is employed in the folded cascode section which increases the CMRR.

Orientation of this paper is as follows: Section I gives the brief introduction of design and implementation of amplifiers to be used for biomedical applications. Section II consists of various amplifier circuit topologies designed for ECG device. Section III

gives the brief comparison of all the techniques mentioned in section II. Section IV points out the best topology based upon the comparison table and finally section V shows future scope.

II. CIRCUIT TOPOLOGIES

There have been various techniques developed for amplifier design for biomedical application. This section gives a brief knowledge of three such techniques. Out of all the techniques available, techniques shown in this section are widely used.

As per the Association of Advancement of Medical Instrumentation, specifications for an amplifier should be as below:

Table I: Specifications for bio-potential Amplifier [4]

Parameter	Value
Gain	≥80dB
CMRR	≥90dB
Phase Margin	≥60°
Power Dissipation	<1mW

A. Instrumentation Amplifier

Figure 1 illustrates the block level diagram of instrumentation amplifier proposed in [3].

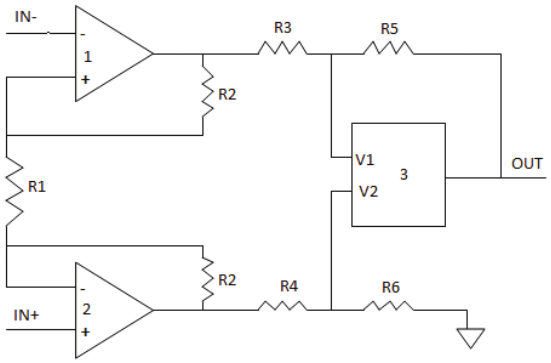

Figure 1: Block Diagram of Instrumentation Amplifier [3]

In this design, authors have used conventional three stage instrumentation amplifier for input stage and folded cascode op-amp at the output stage. In this design, an instrumentation amplifier is used in order to reject the common mode noise. Due to addition of folded cascode stage, noise generation of this technique is very low.

The operational amplifiers shown by block 1 and 2 are configured in negative feedback. Figure 2 shows the two-stage op-amp design which is used as input circuit. In this design MN1 and MN2 differential and current mirror MP1 and MP2 makes an input stage. In this design authors have used gm/Id technique to calculate the transistor sizing. This methodology also helps to decide the operating region of transistors. For this purpose below equation can be used:

... (1)

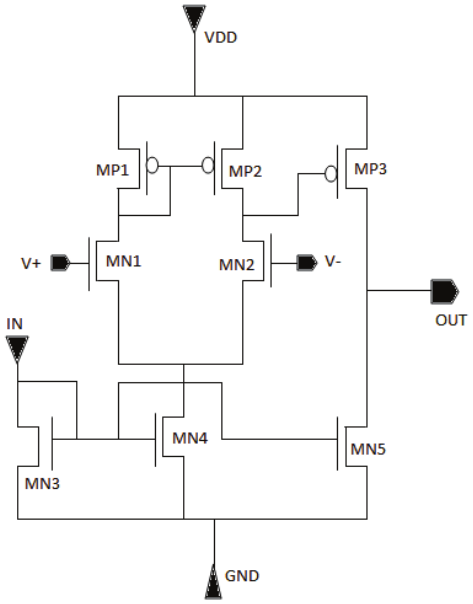

Figure 2: Two Stage CMOS Op-Amp [3]

The optimum transistor sizing obtained is shown in table I.

Table II: Folded Cascode Op-amp Transistor Sizing [3]

Transistors	Aspect Ratio (W/L)
MN1, MN2	5µ/200n
MN3, MN4	3 µ/200n
MN5, MN6	20 µ/200n
MP1, MP2	20 µ/200n
MP3, MP4	20 µ/200n
MP5, MP6	50 µ/200n
MN8	5 µ/200n
MN7	10µ/200n

B. Two Stage Fully Differential Amplifier

In [4] authors have presented a fully cascode amplifier in the first stage and a differential amplifier in the second stage. Common Mode Feedback (CMFB) technique is used in the folded-cascode section to improve CMRR. General block diagram of two-stage op-amp is shown below:

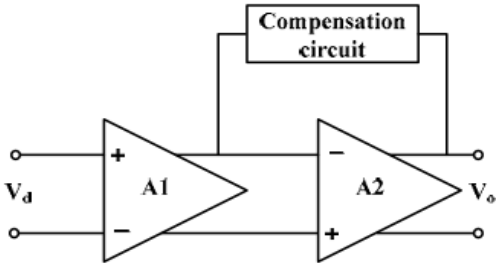

Figure 3: General Block Diagram of Two Stage Op-amp [4]

In this design, folded cascode is employed in order to increase linearity and to improve ICMR. As shown in figure 3 the two stage op-amp topology is used in order to increase the gain of the circuit. This also improves output voltage swing. In order to achieve high CMRR, CMFB technique is used with folded-cascode structure. CMFB stage works as sensing, comparing and controlling the signal [4].

In the mentioned design strategy, first stage is used to improve CMRR rather than focusing on gain and output swing. Keeping the output swing in mind, overdrive voltage is kept low. For sizing the transistors, authors have used gm/I_d technique. This requires the plot of gm/I_d vs V_{ov} and $I_d/(W/L)$ vs gm/I_d. In this work, length is chosen to be 0.5µm in order to avoid the channel length modulation.

C. Tristage Operational Amplifier

In the design shown in [5], a tristage operational amplifier is presented. In this design first stage is a differential amplifier afterwards three amplification stages were added to improve the gain of the circuit. Below figure shows the block level diagram of differential amplifier proposed in [5].

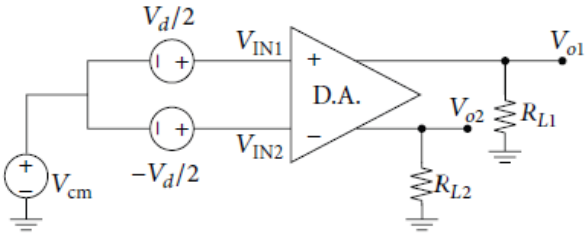

Figure 4: differential amplifier in common mode and differential mode [5]

Analysis of amplifier in common mode and differential mode gives the output voltage as below:

$$V_{o1} = (A_d/2) \times V_d + A_{cm} \times v_{cm} \text{.....(2)}$$

$$V_{o2} = -(A_d/2) \times V_d + A_{cm} \times v_{cm} \text{.....(3)}$$

Where, $V_d = v_{in1} - v_{in2}$, $v_{cm} = (v_{in1} + v_{in2})/2$

The common mode rejection ratio (CMRR) is defined as:

CMRR = ...(4)

Where, A_d is differential gain and

A_{cm} is common mode gain

For a good amplifier it is required to have high differential gain and ideally zero common mode gain. In this work, a balanced biased technique is used in order to reduce process sensitivity.

Being achieved high CMRR; two more stages are further added in order to achieve gain as high as possible at lower bandwidth of 100Hz since amplifier is designed for biomedical application. With the tail current of 7.5µA, transconductance g_m, and gate-to-source voltage (V_{GS}) can be designed by an appropriate dimension ratio, W/L, using following equations:

Where $V_{ov}=V_{GS}-V_{th}$

III. COMPARISON

Results obtained by employing various topologies discussed in section II, are compared in this section. Below table shows the detailed comparison of above techniques.

Table III: Comparison of Different Amplifier Topologies

Parameter	**[2]**	**[3]**	**[4]**	**[5]**
Amplifier Topology	IA*	IA*	Two-stage Op-Amp	Tri-stage
Technology (µm)	0.5	0.18	0.18	0.35
Gain (dB)	80	67.7	106.31	89.3
CMRR (dB)	117	92	131.02	136.7
UGB (Hz)	50	1.75	198.1	79.4
Phase Margin	-	-	57.33°	89.7°
Power Dissipation (µW)	-	263	685	328
Offset Voltage (µV)	60	-	0.28	5.2
Supply Voltage (V)	1.5	-	3.3	3.3

*: Instrumentation Amplifier (IA)

IV. CONCLUSION

Having being studied and compared various topologies, it can be concluded that two-stage op-amp presented in [4] gives the best optimum results as per the specifications provided by AAMI, as shown in table I. Apart from the UGB, all parameters satisfy the specifications required for an ECG device. Further it can be analyzed to reduce its UGB which will further be helpful in increasing gain. This design is simulated for all the process corners and results shown in table III is for typical process corner.

V. FUTURE SCOPE

With the help of integrated technology, entire ECG system can be designed on single IC. With this it is possible to shrink the down the size as well as to reduce the power consumption of ECG device. Integrating ADC and an active filter along with the presented amplifier makes a complete analog front-end that can be employed in biomedical instrument.

VI. REFERENCES

[1] Tsung-Heng Tsai, et al. 'Low-Power Analog Integrated Circuits For Wireless ECG Acquisition Systems'. *IEEE Transactions on Information Technology in Biomedicine* 16.5 (2012): 907-917.

[2] Ng, K.A., and P.K. Chan. 'A CMOS Analog Front-End IC For Portable EEG/ECG Monitoring Applications'. *IEEE Trans. Circuits Syst. I* 52.11 (2005): 2335-2347.

[3] Goel. A, Singh. G, 'A Novel Low Noise High Gain CMOS Instrumentation Amplifier For Biomedical Applications'. *International Journal of Electrical and Computer Engineering (IJECE)* 3.4 (2013):

[4] Abhilash, K.N.; Bose, S.; Gupta, A., "A high gain, high CMRR two-stage fully differential amplifier using gm/Id technique for bio-medical applications," *2013 IEEE Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics (PrimeAsia),*, pp.40-45, 19-21 Dec. 2013.

[5] Hsiao, Yu-Ming et al. 'Design A Bioamplifier With High CMRR'. *VLSI Design, Hindawi Publishing Corporation*, 2013 (2013): 1-5.

[6] Indian Medical Association (IMA),"Exercise and Heart" [Online]. Available: http://www.ima-india.org [Accessed: Sept. 8, 2015].

[7] Leslie Cromwell, Fred J. Weibell, Erich A. Pfeiffer, *Biomedical Instrumentation and Measurement*, Delhi: PHI Learning Pvt. Ltd., 2014.

[8] Allen, P. E, and Douglas R Holberg. *CMOS Analog Circuit Design*. New York: Oxford University Press, 2002. Print.

[9] Razavi, Behzad. *Design Of Analog CMOS Integrated Circuits*. Boston, MA: McGraw-Hill, 2001. Print.

[10] Baker, R. Jacob. *CMOS*. New York: IEEE, 2002. Print.

[11] Amit Kumar, Poonam Bhojani, "Improved Reliability Analysis Tool (ReAl) for Lifetime analysis of CMOS circuits", IEEE 2nd International Conference on Electronics and Communication systems (ICECS 2015), 26-27 Feb 2015.