Managing Power in CMOS Digital Circuit Using Sleep Switch and High Vt Techniques

[1]Prof. AnkurChangela

[1]Assistant Professor
[1]Electronics and Communication,
[1]IITE, Indus University, Ahmedabad

Abstract:The power consumption of Modern digital circuits has two components. The dynamic power is consumed only when the circuit performs a function and signals change. Leakage or static power isconsumed all the time, i.e., evenwhen the circuit isidle. Dynamic and leakagepower dependon power supply and to reduceconsumption of power, its supplyhas to be reducedwhich cannot be loweredbeyond a certain limit as it impacts the speedof the circuit. There is trade-off between power and speed in digital circuit designs and so an optimum solution is always looked forward to. In the earlier period, the prime concern of variedlarge scale integration(VLSI)designerwas area, performance,cost and reliability while power considerations wereof only secondary significance.Motivated by, emerging battery operateddevices likemobile phones, laptops, notebook etc. which demandmore battery backup which can be achieved by decreasing the power consumption of the device that depends on standardcells used to implementdevice. The purpose of this paper is to suggest a technique which brings an optimum solution to the consumption of both static and dynamic power. Static anddynamic power canbereduced using high thresholdvoltage (vt) and sleep switchtechniquesrespectively. The Techniqueproposedinthis paper isablend of both thesetechniqueshigh vtand sleepswitch. Theproposed technique, Synergetic PowerConsumptionTechniquewill help to reduce both the power withoutaffecting the speed of operation. The designwill be implementedusing high end Computer Aided Design (CAD) Tools. Standardtest signals will be applied to designand power will be measured.Powerconsumptionof digital circuit implemented with Synergetic Power Consumption Technique, Sleep-Switch technique and high-vt technique will be measured. For comparison, 8_bit ripple carry adder and dual rail domino 8_bit adder have been implemented with proposed technique and compared with the standard design. It has been observed that 23% of power is saved in case of 8_bit RCA with increase in delay by 20% and 37% of power is saved in case of dual rail domino with increase of 15% in delay.

IndexTerms–Threshold Voltage, Computer Aided Design, Low power dissipation, CMOS design.

I. INTRODUCTION

Inthe earlier period ofVLSIdesign, how to optimize the speed to implement real time applicationssuch as video games, videocompression, graphics etc was prime concern of VLSI Designer. As a result, they have implementedIntegrated Circuits(IC) with various high speed signals processing function to meet computationand entertainment demands. These solutions have solvedthe problem of speed requirementof real time application. At the same time, new problem of power requirementhas been emerged. Portable device like mobile phone need to have all real time modules without consuming much power. As aresult, strict limitation on power consumption in portableelectronicsdevices such as smart tablet, mobile phones, computers etc must be met by the VLSI chip designer without disturbing computational requirements. Since these devicesare rapidly making their way to the electronics market, total power consumption of such devices must be addressed as prime concern of designer. Most of these devices runs on battery and since it is desirable to maximize the run time with minimum requirementson size, battery lifeand weight allocated to batteries, it is very important to reduce the total power consumptionin such portable devicesand hence the most important factor to consider while designing semiconductor ICs for portable devices is 'low power design'.

II. CMOS DIGITAL CIRCUIT DESIGN

The most widely used style is the static CMOS family due to its advantages like low power, high speed and very good immunity againstthe noise. The CMOS circuit style falls undera broadclass of logic circuit called static circuits in which every point in time, output is connected to either V_{DD} or V_{SS}. A static CMOS is a combinationof two networks 1. Pull Up Network(PUN)and 2. Pull Down Network(PDN)as shown in the Fig1.

The Fig.1 shows the generic N-input logic gate whereall inputs in1 , in2 ...inN are distributed to both the pull-up and pull- down networks. Based on the inputs, pull-up network provides a connectionbetween the output and V_{DD} when output of the logic gate is meant to be Logic PUN.Similarly, thefunction of the pull-down network is to

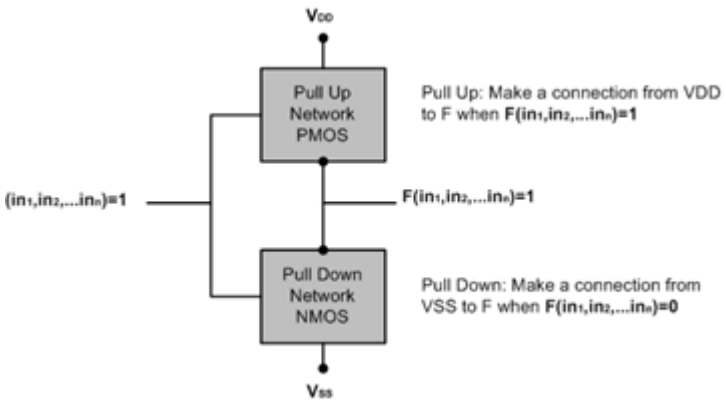


Fig1. Complementary logic gate as a combination of a Pull UpNetwork) and a PDN(Pull Down Network)

provide a connection between V_{SS} and output of the gate when output is meant to be Logic 0. The pull-up and pull-downnetworks are constructed in a mutually exclusive fashion such that one and only one of the networks are conducting in steadystate. Once all the transistors have settled, a path always exists between $V_{DD}$and output F for the high output or between $V_{SS}$and F for low output.

III. SOURCES OF POWER DISSIPATION IN CMOS

CMOS is the most commontechnologyused for manufacturing digital ICs. There are 3 major sourcesof power dissipation in a CMOS circuit. [1]

1) Switching Power
2) Power dissipated due to Short Circuit Current
3) Leakage Power

Total power in CMOS $P_{total}$is given by:

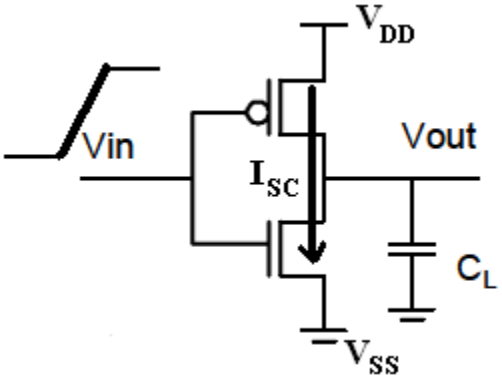
$$P_{total} = P_{Switching} + P_{ShortCircuit} + P_{Leakage} \quad (1)$$

SwitchingPower: The switching power is due to charging and discharging of load capacitor(C_L). Each time the capacitor CL gets charged through PMOS transistor,output voltage rises from 0 to V_{DD} , and certain amount of energy is drawn from the power supply. Part of this energy is dissipated in PMOS and remaining energy is stored in load capacitor(C_L) [2]. When output of the gate is driven to low state, load capacitor(C_L) is discharged, and the stored energy is dissipated in the NMOS transistor.Power consumptiondue to switching activity is given by the equation2

$$P_{Switching} = C_L V_{DD}^2 f_{0\to1} \quad (2)$$

Where:
C_L = Load Capacitor
V_{DD} = supply voltage
$f_{0\to1}$ = Represents the frequency consuming transitions.

Power dissipated due to Short Circuit Current: Short circuit current is due to rise and fall time of the input. In actualdesigns, theassumption of the zero rise and fall times of the input wave forms is not correct. The finite slope of the input signal causes a direct current path between VDD and VSS for a short period of time during switching, while the NMOS and the PMOS transistors are conducting simultaneously. [3] [4] To elaborate this consider an example of Inverter as shown in Fig2.



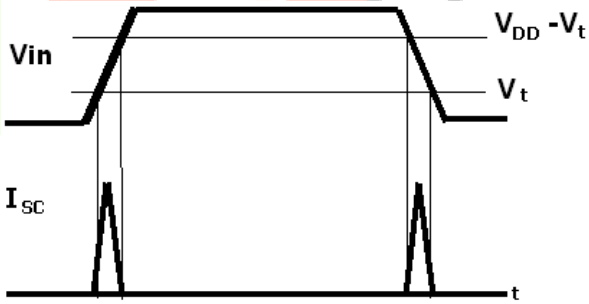


Fig.2. Basic CMOS Inverter Fig.3 Short Circuit current due to Transients.

Fig3 shows the input and short circuit current waveform. As shown in Fig.3, when input Vin is between Vt and V_{DD}-Vtboth PMOS and NMOS are conducting and direct path from VDD to ground exists which is responsible for short circuitcurrent. Average power due to short circuit current is given by equation3.

$$P_{Short\_Circuit} = t_{sc} V_{DD} I_{peak} f \quad (3)$$

Where,
t_{sc} = time both the devices NMOS and PMOS are conducting.
I_{peak} = Average short circuit current
f = frequency of switching activity

Leakage Power: When the input is such that, the pull-down network is OFF, and the pull-up network is ON and the output voltage is VDD, or Logic 1 or when the input is such that, the pull-up network is OFF, and the pull-downnetwork is ON and the output voltage is VSS, or Logic 0, in any of the this case one of the network is always OFF when the gate is in either of these logic states. Since no current flows into the gate terminal, and there is no dc current path from VDD to VSS hence, static power consumption is zero. However, there is a small amount of static power consumption due to reverse-bias leakage between diffused regions and the substrate [5] [6]. This leakage inside a device can be explained with a simple model that describes the parasitic diodes of a CMOS inverter, as shown in Fig4. The source drain diffusion and N-well diffusion form parasitic diodes. In Fig4, the parasitic diodes are

shown between the N-well and substrate. Because parasitic diodes are reverse biased, only their leakage currents contribute to static power consumption.

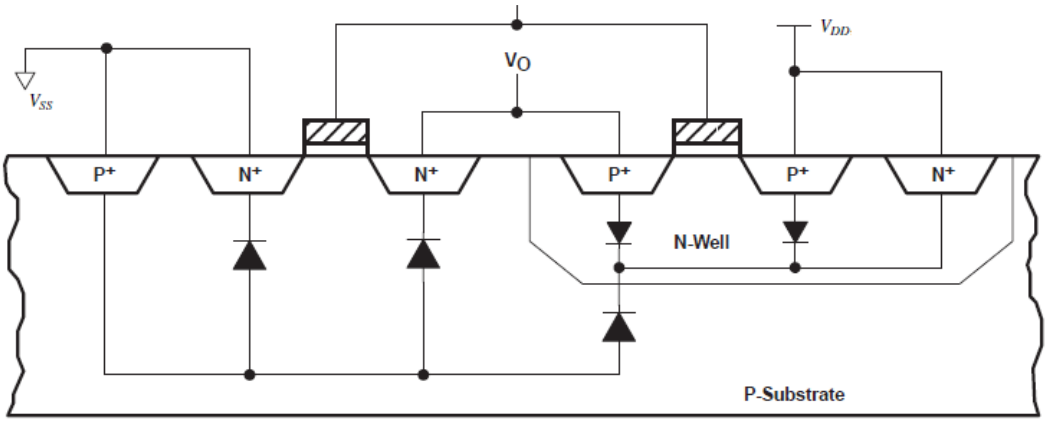


Fig. 4. Model Describing Parasitic Diodes Present in CMOS Inverter

The leakage current (I_{lkg}) of the diode is given in equation4.

$$I_{lkg} = i_s(e^{qV/kT} - 1) \quad (4)$$

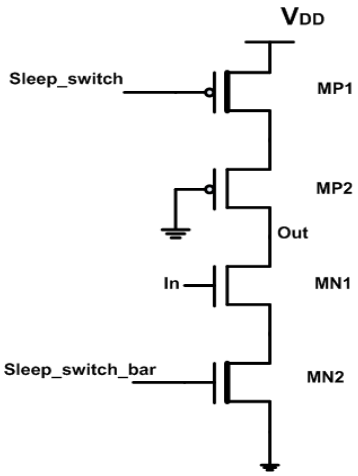
Where:
i_s = reverse saturation current
V = diode voltage
k = Boltzmanns constant (1.38 x 1023 J/K)
q = electronic charge (1.602 x 1019 C)
T = temperature
Leakage power consumption is the product of the device leakage current and the supply voltage is given by equation2.

$$P_{lkg} = I_{lkg}V_{DD} \quad (5)$$

IV. PROPOSED TECHNIQUE TO MINIMIZE POWER

As shown in equation2, 3 and 5, Voltage scaling is perhaps the most effective method of saving power as all powersdirectly depend on VDD [7]. As supply voltage is scaled down, output voltage swing will be reduced and systemloses immunity against the noise and due to this VDD cannot be reduced after certain limit. Further if VDD is scaled down, VGS VT is going to be reduce which intern going to reduce the speed of the circuit. To deal with this, dynamic voltage scaling may be applied to system in which threshold voltage of the MOSFET is also scaled down to maintain the voltage swing V_{GS}-V_T. Scaling down the threshold voltage leads to considerable rise in the leakage current of the transistors. Hence, there is a clear trade off among the active power and off-state leakage for a specified application, leading to methodical selection of V_{DD} and V_T.

Another method is to reduce the switching frequency i.e. the number of 0 to 1 and 1 to 0 power dissipating transitions.Switching frequency may be reduced on several levels in the design process beginning from circuit level to thearchitectural level. For an example consider Arithmetic and Logical Unit(ALU) of processor which performs arithmeticoperations like addition, subtraction multiplication etc... and logical operations like AND, OR and XOR. To performthese operations, ALU contains separate digital circuits for each operation. Operation to be performed is dependent on the instruction is being executed. Assume that ALU is executing addition then all other circuits except the circuitwhich performs addition has to be off to reduce the power consumption and these circuits are in sleep mode. In a sleep mode, gate is disconnected with the power supply when it is not being used. This technique is very useful in design when the part of the design is active at each instance of time so that only active part of the circuit gets connected to supply and other ideal part of the circuit gets disconnected to reduce the power consumption.



Proposed technique is implemented at gate level and to understand the same consider an Inverter(INV) as shown in Fig5. Inverter is made from four transistors MP1, MP2,MN1 and MN2. MP1 and MN2 together forms a sleep mode and MP2 and MN1 forms normal Fig.5 Proposed Gate Structure
inverter. Sleep switch signal is connected to MP1 and inverted sleep signal i.e. sleep switch bar is connected to MN2. When sleep mode is activated by making Sleep switch high MP1 transistor goes off and since sleep switch is high sleep switch bar goes low and MN2 goes off. Due to this, Inverter gets disconnectedwith power supply and even if there is switching activity at input, Inverter

will not respond to that switching activity as itis already disconnected with power supply. During the normal operation, sleep switch is low and sleep switch bar is high so, transistor MP1 and MN2 are on and inverter gets connected to power supply. When sleep mode is activated, MP1 and MN2 are off and very high off state leakage current will flow and to overcome this problem threshold voltage of MP1 and MN2 are kept high.

V. SIMULATION RESULT

Three logic gates, INVERTER,NAND and NOR are implemented using proposed technique at 180nm technology with3V power supply. Simulation is carried out using spice tool and results as been shown in Table I below. As shown in Table I, it is clear that power consumption of three gates is high compare to the gates implemented with proposed technique. Delay of gates, implemented with proposed technique is slightly increased then normal gates and it is clear that there is tradeoff between power and speed and one has to choose the optimum solution.

Gate	Normal		WithSleepSwitchTechnique	
	Delay(inns)	Power (inμwatt)	Delay(inns)	Power (inμwatt)
INV	0.45	163	0.65	6.522
NAND	0.53	184	0.75	4.546
NOR	0.7	470	0.83	38

TABLE I
PERFORMANCE ANALYSIS

Also, for comparison 8_bit ripple carry adder and dual rail domino adder has been implemented with proposed technique and using conventional method. It has been observed that 23% of power is saved in case of 8_bit RCA with increase in delay by 20% and 37% of power is saved in case of dual rail domino with increase of 15% in delay.

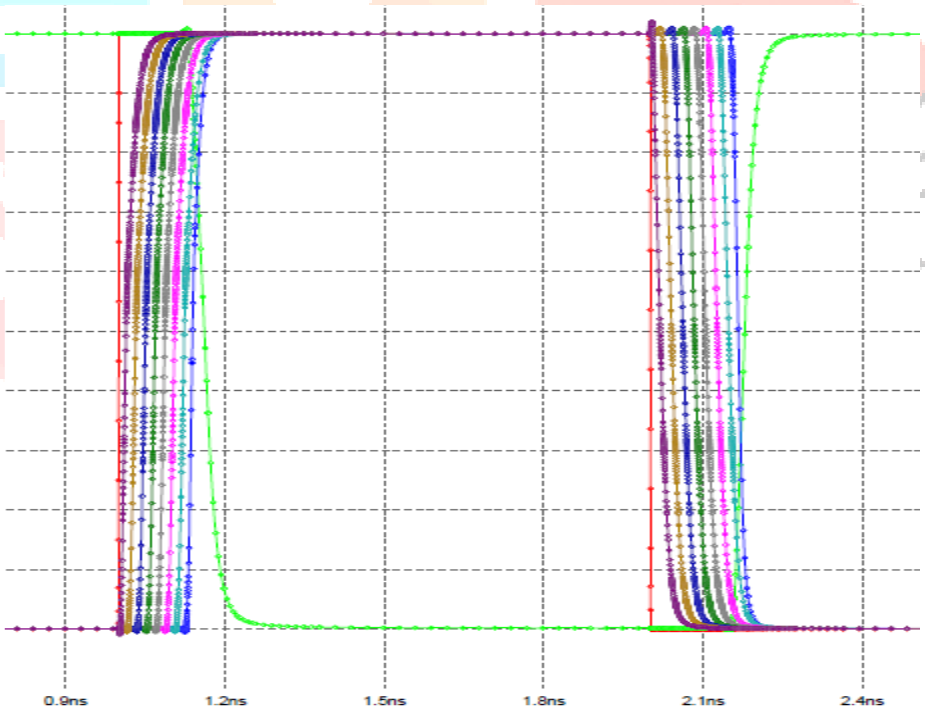


Fig. 6.Simulation Result of 8-bit ripple carry Adder

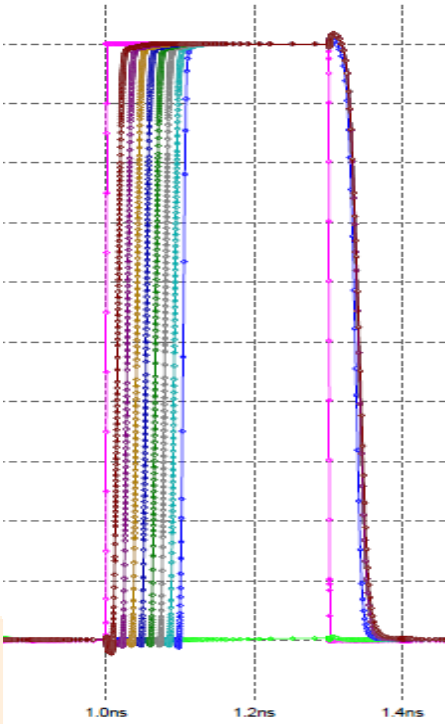


Fig.7. Simulation Result of 8-bit Domino ripple carry Adder

VI. CONCLUSION

This paper is focused on Low power implementation of CMOS digital circuit design at gate level. This paper describesthe low power techniques sleep switch and high Vt . Simulation of logic gates were carried out through ngspice with 180nm technology. Total power dissipation of proposed logic gate is measured and compared with normal logic gates. This technique can be used when some portion of the whole design is active.

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