Modern Design approach of Reduced Ordered Binary Decision Diagram (ROBDD) for testing Multiple Stuck-at Faults in Digital blocks

DR. ARVIND KUNDU[1], G.NARESH[2], MACHA BABU RAO[3]
[1]HOD, Dept of ECE, Scient Institute of Technology, Ibrahimpatnam, Hyderabad, India,
[2]Assistant Professor, Dept of ECE, Scient Institute of Technology, Ibrahimpatnam , Hyderabad, India,
[3]PG Scholar, Dept of ECE(VLSI & ES), Scient Institute of Technology, Ibrahimpatnam , Hyderabad, India.

Abstract: The test pattern for a multiple fault is the special test pattern for the special single stuck-at fault forming the multiple one. Test for all multiple faults is derived from any test for all single stuck-at faults. The length of the multiple faults test is linear function of the single faults test length. A multiple fault test is the one of high quality. In particular SEU and bridge faults may manifest themselves as multiple faults at the CLBs poles. Deriving test for all multiple faults was executed for the certain bench-marks. For them the length of the multiple faults test is about the twice length of the single faults test. The circuit is designed by covering the Shared ROBDD by CLBs. The entire project describes finding multiple faults in combinational logic blocks using ROBDD technique.

Index Terms: Multiple faults, ROBDD, combinational logic

I. INTRODUCTION

Design and test constitute a major cost component in the process of chip manufacturing. Over the years test oriented research has contributed significantly in minimizing test generation effort and simultaneously achieving desired test results. Current test strategies generally consider single stuck-at fault (SSAF) coverage. The assumption here is that the SSAF test set will detect other type of faults such as multiple stuck at and bridging faults with satisfactory coverage. To consider exclusive fault models other than SSAF will lead to long test computation times. A circuit with n-nets can have $3^n - 1$ multiple stuck at faults (MSAFs). This is an impractical number to derive tests for. Many approaches have been proposed to provide complete multiple fault coverage for fan-out free circuits, irredundant two-level circuits, and internal fan-out free circuits. In reality, circuits do have internal re-convergent fan outs. The other works focus on mapping SSAF tests to evaluate MSAF tests. Since SSAF test patterns are available, mapping them to detect MSAFs would drastically reduce test generation effort. SSAF test sets do detect 70% to 80% of the MSAFs. Researchers have looked at improving the MSAF coverage. The most recent work by Fujuta ET. Al. involves SAT based formulation for ATPG of circuits having large number of faults. The formulated SAT problem drops faults which are detected; however the corresponding constraints are not dropped. This allows them to deal with the solving process very efficiently. They have shown that the MSAF test set is only a slight extension to the single stuck at fault test set. Agrawal et al. use branch and bound algorithm to detect MSAFs which are not detected by single stuck-at fault tests. However, these proposals test the circuit as a whole for MSAFs leading to exponential test generation complexity.

Ensuring complete SSAF, MSAF, and delay fault testability during design stage helps reduce test pattern generation time. This also leads to minimum design alterations in case of unsatisfactory fault coverage at a later stage. On the other hand, there have been several design approaches proposed in the literature to improve circuit testability. One of such approaches is Reduced Ordered Binary Decision Diagram (ROBDD) based circuit design. For a ROBDD based implementation, each internal ROBDD node is replaced either by a multiplexer or an Invert-And-Xor sub-circuit. These synthesis methods offer 100% testability for single stuck-at and path delay faults. The method uses an additional input, whereas slight architectural modifications are made to eliminate the extra input. MSAF testability of ROBDD based mux implementations remain to be investigated. Exhaustive testing of a circuit-under-test would cover complex faults including MSAFs and bridging faults, however it is impractical. A practical approach called Pseudo exhaustive testing was proposed by McCluskey et.al. In. Their proposal was aimed at Built-In Self-Test architectures. Pseudo exhaustive testing strategy has a potential application to a ROBDD based structure which is inherently modular in nature. Test vector generation in this case would have a polynomial test generation complexity. This project presents a fully delay and MSAF testable circuit design. The major contributions of this paper are:

- A pseudo exhaustive test strategy to detect all MSAFs in ROBDD based circuits which has negligible test generation effort.
- All irredundant multiple faults of the circuit under test are proven testable.

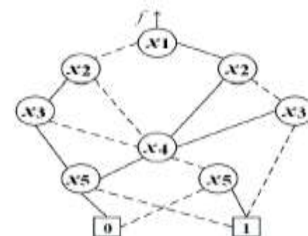

Fig.1. ROBDD example for Boolean function f.

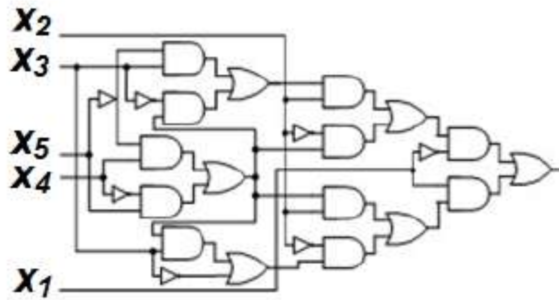

Fig.2. Or-based design (circuit C) for ROBDD

It is known that test for all multiple stuck-at faults at the gate poles is the one of high quality but the test cannot be obtained by enumeration of all multiple faults. It is possible to avoid enumeration only for special circuits. For example the circuit behavior have to be described with a system of irredundant sums of products (prime implicates of functions constituting the system) followed application of multi level synthesis method to such system. In this case the length of the test for all multiple stuck-at faults at the gate poles of the circuit obtained is not more than the number of literals in the system and the number of products of the system. The test for multiple stuck-at faults of the circuit is directly derived from the system. In this paper we found out possibility to built test for all multiple stuck-at faults at the CLBs (Configurable Logic Blocks) poles (without enumeration of faults) for circuits derived with covering Shared ROBDDs by CLBs in the frame of FPGA technology. We have proved that for these circuits there exist a test pattern for any single stuck-at fault at the CLBs poles and a test pattern for any multiple faults constituted from such single stuck-at faults. Moreover test for all multiple faults of the circuit is derived from any test for all single stuck-at faults of the circuit so that each test pattern of the last test gives rise to several test patterns comprising the test for multiple faults. The length of the multiple faults test is linear function of the single faults test length. The techniques of finding both tests are developed and some experimental results have been got. A multiple fault test is the one of high quality. In particular SEU and bridge faults may manifest themselves as multiple faults at the CLBs poles.

II. LITERATURE REVIEW

Test pattern generation algorithms for multiple faults have been proposed by several authors. All these works report a large search space and also explain the complexity of these multiple fault diagnosis approaches. Classical Automatic Test Pattern Generation (ATPG) algorithms are path oriented which means that, starting from the fault location, signal values are determined to allow initialization and propagation of the fault. As ATPG is NP-complete, finding a solution in general is very difficult and therefore the search is directed by heuristically methods. Binary decision diagram (BDD) based methods for ATPG have been proposed by many (Dreschler 1994). In addition, BDD based algorithms for ATPG offer the possibility to compute not only a single test pattern, but all the possible test patterns for the given fault. The property of BDDs in which exactly one path is sensitized by a given input combination proves advantageous for the design of circuits with low power consumption (Lavagno et al 1995). The disadvantage is that, BDDs may become inadequate for the problems considered, e.g. some relevant classes of Boolean functions cannot be represented efficiently by BDDs. In practical applications, it is quite frequent that circuits leading to large BDDs have to be used and therefore a solution of ATPG is not possible or at least very time consuming. Thus, several extensions of BDDs have been proposed in the last few years, Zero suppressed BDDs (ZBDDs) being one among them. The proposed method of test pattern generation for multiple faults is a novel method which makes use of ZBDDs. This method attempts to reduce the search space as compared to BDDs. The circuit without any faults is called the fault free circuit and that with faults is called the faulty circuit.

The method begins with the BDD representation of both the fault free and the faulty circuit. The exclusive OR operation of the fault free and the faulty BDD gives the test BDD. From the test BDD thus obtained, the corresponding ZBDD is derived. The ZBDD from which the test patterns are obtained is the test ZBDD. This method reduces the number of nodes by suppressing the zero paths, thereby reducing the memory space required and hence the test patterns are generated relatively faster when compared to their corresponding BDD. Many multiple fault diagnosis algorithms have been reported. Abadir and Reghbati (1986) proposed an extension to the D-algorithm, for integrated circuits described using BDDs. A fault model was developed at the functional level quite independent of the implementation details of the individual modules in the chip. A generalization of the D-algorithm was done which took the module level model and the functional description of the modules as parameters and generated tests to detect the faults in the fault model. As in the D-algorithm, the procedure employed three basic operations namely implication, D-propagation, and line justification. These operations were performed on the functional modules. Jha (2003) proposed the problem of detecting multiple faults in domino-CMOS logic circuits. The multiple faults could be faults of the stuck open and stuck-on types. It was shown that a multiple fault in the domino CMOS circuit can be mapped to a multiple stuck-at fault in its gate-level model. The method was first applied to initialize the domino- CMOS circuit.

Then a multiple stuck-at fault test set based on the gate level model of the circuit was applied. This resulted in the detection of all multiple faults, whose consistent faults are detectable. The proposed method of test pattern generation using ZBDD had a reduced number of ZBDD nodes and also a reduced number of paths for test pattern generation. Verreault et al (1991) considered multiple stuck-at-(0/1) faults at the gate level. First, a fault collapsing phase was applied to the network so that equivalent faults were eliminated. During the analysis, frontier faults were considered and there was at least a normal path from each faulty line to a primary output. It was shown that the set of frontier faults was equivalent to the set of multiple faults. Given an input vector, the normal circuit was evaluated and the fault effects were propagated. A fault

dropping procedure was then applied to eliminate faulty conditions on specific lines that were either absent or permanently masked by other faulty conditions. The method does not explicitly enumerate all the multiple stuck-at faults that may be present in the circuit.

Takahashi et al (1991) suggested a new test generation algorithm for combinational circuits with multiple faults. A new algorithm for generating a single sensitized path using a seven valued calculus and a decision algorithm for finding a completely single sensitized path were presented. A fault simulation technique was carried out by Takahashi et al (1994) for multiple faults based on a deductive fault simulation method. The conventional deductive simulation used linear lists to store fault sets, which was not appropriate for such large sets of multiple faults. Hence, sets of multiple faults were represented by Boolean functions. A distinct code word was assigned to each multiple fault using a coding method called Fermat Number Transform (FNT) coding. Bechir and Bozena (1995) presented a new approach for generating test vectors for combinational circuits. Here, the automatic test generator, called BDD-FTEST, uses an algebraic method to find a set of test vectors for single stuck lines. This algorithm involves a path- oriented search similar to the one used by conventional algorithms. This method determines the set of input assignments that would propagate a fault through a gate in the path from a faulty site to a primary output. The method had eliminated backtracking by comparing the BDD of the fault free circuit and that of the faulty one only at the dominators of the faulty line. To generate test vectors for large circuits, BDD-FEST uses tie observability of a line concept to identify the set of faults that may be propagated to a given primary output. In this approach, the primary outputs are studied separately. Each one of the primary output has its own variable ordering.

Then, when all the primary outputs have been studied, the remaining undetected faults are declared redundant, since they cannot be propagated to any primary output. Bolchini et al (1995) presented a testing algorithm, called BDD Test, which was applied after a standard random test pattern generation. In this way, all the faults rejected by the test pattern generator were analyzed by BDD Test which was always able to find a test vector or to declare the fault as a redundant one. Bhattacharya et al (1995) proposed a test generation technique for path delay faults in circuits employing scan /hold type flip flops. Reduced ordered binary decision diagrams (ROBDDs) were used to represent Boolean functions realized by all signals in the circuit, as well as to represent the constraints to be satisfied by the delay fault test. A novel procedure was derived by Agrawal et al (1996) for testing all multiple stuck-at faults in a logic circuit using two complementary algorithms. The first algorithm finds pairs of input vectors to detect the occurrence of target single stuck-at faults independent of the occurrence of other faults. The second uses a sophisticated branch and bound procedure to complete the test set generation on the faults undetected by the first algorithm. Arslan and O'Dare (1997) proposed a genetic algorithm based approach where test patterns for both delay and stuck-at faults were generated and binary strings were used as chromosomes. Mutation and cross over operations were performed to check whether the generated offspring was better than the parent chromosome. This process was repeated until the fittest chromosome which represents the optimized test pattern was generated. AL-Jumah and Arslan (1998) proposed a technique based on the use of artificial neural networks for the diagnosis of multiple faults in digital circuits. The technique utilized different quantities of randomly selected circuit test data derived from a fault truth table, which was constructed by inserting single stuck-at faults randomly in the circuit.

A test algorithm was developed by Becker (1998) using the capabilities of DDs as a data structure for tasks like fault detection, synchronization and built-in-self-test. These algorithms mainly concentrated on synthesis for testability approaches, where the circuits are derived from DD representations. Their testability properties with respect to static and dynamic fault models were analyzed. Hence, the computation of complete test sets and all redundancies could be done easily and efficiently based on DD manipulation algorithms. Bystrov and Almaini (1999) analyzed the diagnostic properties of Decision Diagrams (DD's) and described a method to provide test patterns for single and multiple stuck-at faults. This method also presented a test set compaction algorithm. The testability properties of circuits derived from Kronecker Functional DD's (KFDDs), a superset of BDDs and FDDs, were also discussed. The depth of KFDD circuits was reduced by the application of a composition method based on Boolean matrix multiplication. Ghosh and Fujita (2000) have presented an algorithm for generating test patterns automatically for functional Register Transfer Level (RTL) circuits that target detection of stuck-at faults in the circuit at the logic level using a data structure named assignment decision diagrams.

Hiroshi Takahashi et al (2002) suggested a method of diagnosing multiple stuck-at faults in combinational circuits using single and multiple fault simulations. The method added (removed) faults from a set of suspected faults depending on whether the result of multiple fault simulation at a primary output agreed (disagreed) with the observed value. However, the faults that are added or removed from the set of suspected faults are determined using single fault simulation. Diagnosis is carried out by repeated addition and removal of faults. A simulation-based incremental approach was derived by Liu et al (2002) for multiple stuck-at fault diagnosis in combinational and full-scan sequential digital circuits. The algorithm accepted a digital implementation corrupted with stuck-at faults and its gate level net list which was able to be simulated. It then iteratively identifies and fault-models the suspect locations one at a time until the set of faults modeled can functionally fully account for the faulty behavior.

For each iteration, the algorithm identifies a single suspect line in the net list and injects an appropriate stuck-at fault on the line so as to bring the function of the net list closer to that of the faulty implementation. Fey et al (2004) evaluated different

optimization techniques for BDDs, based on variable reordering with respect to the path delay fault testability of the resulting circuit. It was found that the reduction of the number of paths in the BDD can significantly reduce the number of test patterns needed to test the circuit with respect to the Path Delay Fault Model. Hence the reduction in test complexity. Maria et al (2005) designed a function to represent Path Delay Faults (PDFs) together with their non-robust test cubes. The function was manipulated effectively using ZBDDs and Irredundant Sum of Products (ISOPs). In addition to compact test generation, the function formulation and representation introduced in this paper was important for a variety of applications that ranged from test pattern generation to timing analysis. All the existing diagnostic test generation process concentrate on generating vectors which include a large search space, thereby increasing the complexity.

This new function presented in this paper can be stored efficiently using ISOPs/ZBDD data structure. Zhongliang et al (2006a) proposed a neural network approach where a neural network was used to characterize the circuit. A constraint circuit was created which consisted of a faulty circuit, fault free circuit and an interface circuit. The primary outputs of the faulty and fault free circuits were connected through the interface circuit that makes at least one primary output of fault free circuit to differ from the corresponding faulty circuit. After the tests were generated, sample data were built to train the network and to diagnose the faults. Lin and Cheng (2006) proposed a diagnostic test generation method in conjunction with an efficient sequential SAT-based diagnosis procedure to precisely identify multiple defective signals that can jointly explain the circuit's faulty behavior. This method could be applied after any existing state-of-the-art diagnosis process to further improve the diagnosis resolution. This method made use of multiple-capture anti-detecting tests, along with a sequential SAT solver to maximize the effectiveness and efficiency of SAT-based diagnosis and to achieve higher diagnosis resolution.

III. EXISTING AND PROPOSED SYSTEMS

A. Existing System

Notice that single stuck-at 1(0) fault of the CLB output pole is reduced to the corresponding 1(0) fault of the node v of the Shared ROBDD. A single stuck-at 1(0) fault of the CLB input pole corresponding to the internal variable of the combinational circuit C is also reduced to 1(0) fault of the proper node v of the Shared ROBDD. In the last case a test pattern is generated by a path connecting the jth root of the Shared ROBDD with the node corresponding to the output pole of the CLB, the node corresponding to the fault input pole of the CLB and the 0(1) terminal node. Single stuck-at 1(0) fault on the CLB input pole directly connected with the combinational circuit C input xi is reduced to 01(10) faults of the edges coming from the nodes marked with index i. The nodes (fault nodes) are covered with the CLB. It is enough to consider only one pair of such edges (one fault node), and only one path ρ. A ROBDD is a canonical representation of the Boolean function for a chosen order of input variables. There is a fixed order of variables in all paths from root node to terminal nodes. Since every node is a decision-making node, it is synthesized using a decision-making circuit (2:1 mux) for every input variable. Consider a ROBDD shown in Figure 1 which we will be using as a running example. The primary aim of a ROBDD based implementation is to achieve complete path delay testability.

This approach involves covering each ROBDD node with a sub-circuit. Dreschler et.al. Replaces each node by a multiplexer. However an additional input t representing the leaf nodes is used to generate a transition, this is an overhead. In Matrosova et. al. the ROBDD nodes are replaced with Invert-And-Xor circuits. This method eliminates the requirement of additional control input t. The transitions required for delay test are generated through primary inputs. To reduce sub-circuit path lengths caused by XOR gates in, they are replaced by OR gates. Figure represents the implementation based on OR gates (labeled as circuit C). This replacement still allows full delay testability albeit via robust as well as valid table non-robust tests. Any path that connects the BDD root with the 1 terminal node creates one product of the Disjoint Sum of Products (DSoP) of a function f that is represented by the ROBDD. This paper aims to derive test sets for MSAFs in an implementation of a single function ROBDD which can be represented by a DSoP expression. The derived test sets are applicable to all ROBDD based implementations viz.

B. Proposed System

As technology scales, small and dense geometries, and process variations introduce defects that are often not detected by single stuck-at tests. To improve defect coverage, we expand the single stuck-at tests to cover multiple stuck-at faults. This paper investigates multiple stuck-at fault (MSAF) testability of ROBDD (Reduced Ordered Binary Decision Diagram) based fully delay testable combinational circuits. The circuits are derived by covering ROBDD nodes with Invert-And-Or sub-circuits (2:1 muxes). We show that for each sub-circuit which acts as a partition, the multiple stuck-at fault test set needs only four vectors. Additionally we prove that multiple stuck-at fault test set for the complete circuit has an upper bound of 3N test vectors where N is node count of the ROBDD representing the circuit. A combinational circuit is derived with covering the proper Shared ROBDD by CLBs in the frame of FPGA technology. Single stuck-at faults at the CLBs poles and multiple faults constituted from such single stuck-at faults are considered. It is shown that the test pattern as for single stuck-at fault so for multiple fault there always exists. The test pattern for a multiple fault is the special test pattern for the special single stuck-at fault forming the multiple one. Test for all multiple faults is derived from any test for all single stuck-at faults. The length of the multiple faults test is linear function of the single faults test length. A multiple fault test is the one of high quality. In particular SEU and bridge faults may manifest themselves as multiple faults at the CLBs poles. Deriving test for all multiple faults was executed for the certain bench-marks. For them the length of the multiple faults test is about the twice length of the single faults test.

IV. SIMULATION RESULTS

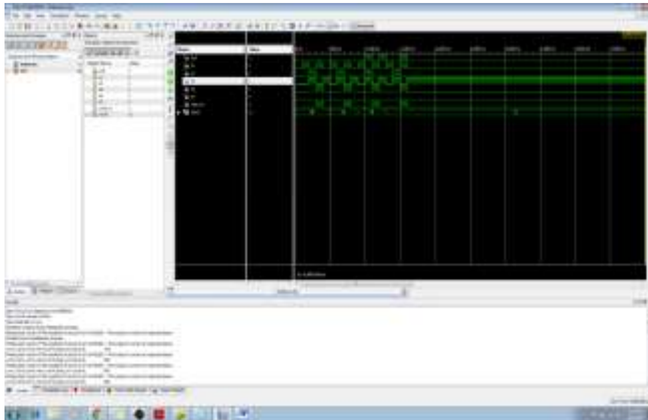

Fig.3

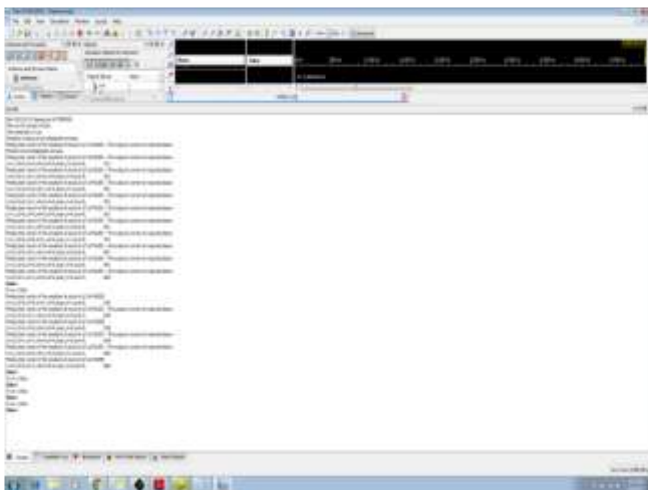

Fig.4. Showing the test vectors which has been passed and which has been failed.

4.1 RTL Schematic

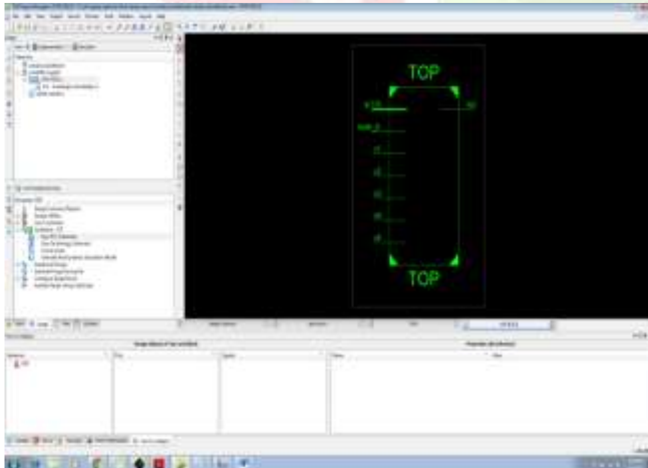

Fig.5

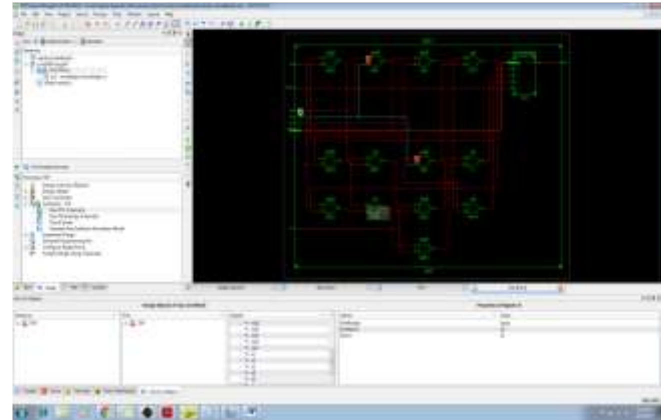

Fig.6

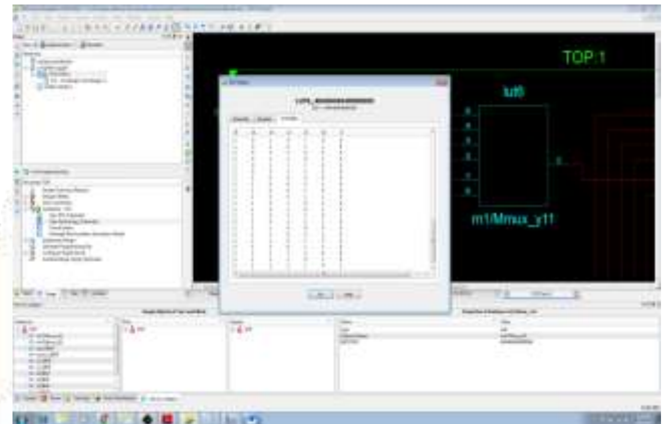

Fig.7

V. CONCLUSIONS AND FUTURE SCOPE

A. Conclusion

This paper has explored MSAF testability of a circuit incorporated utilizing ROBDD, which is completely single stuck-at and postpone blame testable. It is demonstrated that a ROBDD based usage utilizing 2:1 mux is additionally MSAF testable through sharpened parceling. Each segment test set comprises of 4 test vectors which can be inferred in polynomial time. Since the test era exertion is coordinated at MSAFs, all single stuck-at deficiencies are naturally secured. It is shown that the test pattern as for single stuck-at fault so for multiple fault there always exists. The test pattern for a multiple fault is the special test pattern for the special single stuck-at fault forming the multiple one. A multiple fault test is the one of high quality. Test Generation for Single and Multiple Stuck-at Faults of a Combinational Circuit Designed by Covering Shared ROBDD with CLBs.

B. Future Scope

In this proposed system, we designed multiple stuck at faults of ROBDD based combinational circuits. In this we found multiple faults in combinational circuits. In future, we will design faults in sequential circuits like processors design, registers, and counters and also we will design this as an IP core and this will be useful when we will send the transmission data and while receiving the data. By using this technology we can reduce area and power.

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Author's Profile:

Dr. Arvind Kundu, He did B. Tech from H.P. University (SHIMLA) in Electronics & Communication. He did M.Tech from M.D.University (ROHTAK) in Electronics & Communication Engineering. He did Ph.D from Ranchi University and area of research is Adhoc Networks, Embedded System, Cryptography, Message authentication Protocol, Image Processing, Routing protocol etc. He is working as HOD ECE Department at Scient Institute of Technology, Ibrahimpatnam.

Mr. G Naresh, He received the Master Of Technology degree in Electronics And Communication from the Scient Institute of Technology(JNTU Hyderabad), he received the Bachelor of Engineering degree from Vijaya Krishna Institute of Technology And Sciences (JNTU Hyderabad). He is currently working as Assistant Professor in ECE Dept with Scient Institute of Technology, Ibrahimpatnam, Hyderabad, India.

Macha Babu Rao, PG Scholar, Dept of ECE(VLSI & ES), from Scient Institute of Technology, Ibrahimpatnam, Hyderabad, India.