Implementation of Secondary Synchronization in LTE

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***Abstract*- In order to acquire the cell character before partner with the cell, cell search is to be performed in 3GPP Long haul Advancement (LTE) systems. Sending the Primary Synchronization signal (PSS) and the Secondary Synchronization signal (SSS), the cell identity is exchanged. With the utilization of SSS, we get one of 168 conceivable regards for the physical cell identity and from the PSS we get one of the three conceivable regards. On specifically executing SSS area, on account of the sufficient number of required correlators a substantial zone is made. The gear utilization for the area of the SSS and a definite arrangement about it is exhibited in this paper. The usage of the SSS is performed utilizing the Parallel Self Time Adder (PASTA) and compared with that of Carry Select Adder (CSA).**

***Index Terms:* Synchronization in LTE, SSS, Secondary Synchronization, PASTA, SSS detection.**

I. INTRODUCTION

The interest for high information rates which is continually everlasting has been the primary guide for the change of the 3GPP LTE particulars. Different framework data transfer capacities shifting from 1.4MHz to 20MHz are being upheld by LTE. Expecting the transmission capacity of the framework to be 20MHz, the LTE target top for the uplink information rate and downlink information rate are 50Mbits/sec and 100Mbits/sec, separately. LTE uses the Orthogonal Recurrence Division Multiplexing (OFDM) for the downlink information transmission to accomplish such inordinate rates over the recurrence particular channels. We utilize OFDM on account of its power to manage multi-way blurring channels and furthermore it's more noteworthy. Within every 10 ms radio frame, the Synchronisation Signals are broadcasted twice.

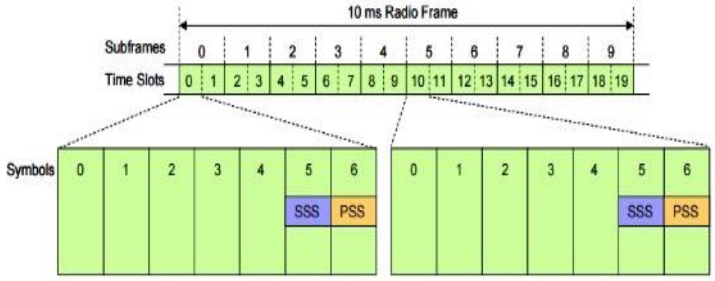

Fig.1 LTE Radio Frame

More prominent range proficiency and furthermore higher client throughput are required for the future versatile correspondence framework. So as to meet these kind of future difficulties, the third Era Organization Task Long Haul Advancement (3GPP-LTE) has been advanced. For downlink transmission, LTE not just uses the Orthogonal Recurrence Division Multiplexing (OFDM) yet additionally bolsters Multi Input Multi Output (MIMO) plan. In LTE, beginning cell seek has dependably been vital to acquire the data, for example, cell-personality gathering, physical-layer ID and furthermore the edge timing for downlink framework. With a specific end goal to get the sub-outline record and the cell-personality gathering (1) ID N, SSS identification is the fundamental assignment to be performed. With the improvement of remote correspondence innovation, the ASICs have been tested by the rapidly changing necessities of remote conventions due to its confinements, for example, over the top plan cost, firmness and delayed advancement cycle. At the point when joined with spatial multiplexing, which is alluded to as Multi Input Multi Output (MIMO) for the downlink, OFDM is a getting decision. We can legitimize this from its trademark insusceptibility to multipath impedance (MPI), on account of the low image rate and furthermore as it utilizes cyclic prefix (CP) and furthermore that it can bolster different transmission data transfer capacity settlements. So as to broaden the assorted variety pick up and to enhance the framework in recurrence particular channels, Multi reception apparatuses are set at the transmitter and collector and MIMO innovation are utilized. Particularly in bigger data transmissions, various potential execution favorable circumstances are offered by OFDM over a framework by utilizing a solitary transporter recurrence, for example, straightforward beneficiary plan, high unearthly effectiveness, MIMO preparing proficiency and strength in a multi-way condition. In view of a few hindrances like the time balances, recurrence balances, and inspecting rate changes, stage balances, orthogonality of OFDM may be gone at the collector. Consequently, keeping in mind, the end goal to perform dependable demodulation and information discovery from the got flag, synchronization estimation of those parameters is fundamental. For foundation of correspondence between the User Equipment (UE) and the base station (improved Hub B), a few procedures must be performed by the UE. The principal procedure is called cell look, amid which the UE needs to check for the most grounded flag originating from the closest base station to perform match up and accomplish cell identity (ID).

II. ARCHITECTURAL OVERVIEW

N_ID_2 is known after the discovery of PSS. The SSS area is also found out, since we got it before obtaining PSS. But the sub frame list of the present SSS area is not yet known. The SSS is recognized by the gotten SSS with all possible SSS hopefuls and picking the candidate with the most extraordinary relationship. There are about 2 sub-outline lists, 168 N_ID_1 esteems and 336 conceivable competitors. The beneficiary should create all the hopefuls. The correlation output obtained is based on the following formula:

$$C(s, q) = \sum_{k=0}^{61} [R(k)Ts, q(k)] \quad \ldots\ldots\ldots 1$$

where q is the hopeful N_ID_1, R(k) is center 62 sub-transporters of the obtained OFDM symbol, s is the competitor sub-outline file, and Ts, q(k) is created SSS for the sub-outline. Since the SSS is genuine, the conjugate transposition for the delivered SSS picture Ts, q(k) is ignored. R(k) is first expelled, tolerating no coarse repeat adjust. The possible SSS contenders are made using the evaluated N_ID_2, the confident N_ID_1, and the candidate sub-outline list. The association yield, C, is then found out. The enormity of Cis figured and the apex regard is perceived to choose the sub-outline record and N_ID_1. To assuage the effect of noise on C, it is discovered the center estimation of over ceaseless SSSs, and thusly a help is required to store it. The help contains 336 sections of the association yield bit-width.

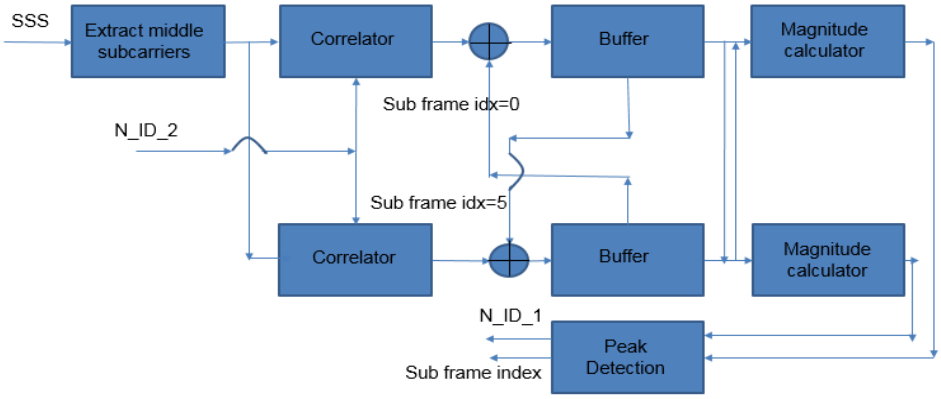

Fig 2. SSS detection block diagram

The SSS substitutes each sub-frame with one of two conceivable esteems. When joining the two connection yields, C (0, q) SSS1 is added soundly to C (5, q) SSS2 and C (5, q). SSS1 is added lucidly to C (0, q) SSS2 where the subscript alludes to either the first or the second SSS. The expansion of the relationship yield of continuous SSS is done intelligibly to diminish the impact of commotion. Each additional SSS adds 5ms to the procurement time. Our reenactments demonstrate that averaging the relationship yield more than two back to back SSS gives the best exchange off amongst execution and obtaining time.

III. HARDWARE IMPLEMENTATION

Clear usage of the location calculation requires a SSS generation unit, 336 parallel correlators, a 336-entry buffers, 336 complex magnitude units, and a peak discovery unit. SSS generation and correlation are finished utilizing:

$$Ts, q(k) = \text{generate\_SSS\_carriers}(N\_ID\_1, N\_ID\_2, s, k) \quad \ldots\ldots\ldots\ldots\ldots 2$$

$$C(s, N\_ID\_1) = C(s, N\_ID\_1) + R(k) * Ts, q(k) \quad \ldots\ldots\ldots\ldots 3$$

For each SSS candidate, Cis found using two operations. The vital operation delivers an example of the hopeful SSS for a particular sub-carrier record k, sub-outline document s, N_ID_1, and N_ID_2. The second operation processes the thing R(k). Ts, q(k) using (2), while gathering the duplication yield with past ones. These two operations are repeated for each candidate sub-outline list (0, 5), each hopeful N_ID_1 (0: 167), and each sub-conveyor record (0:61).

3.1 Correlation core

The correlation yield in (4) for a particular sub-outline rundown and N_ID_1 is found by get-together the expansion of R(k) and the looking at SSS hopeful impetus at a comparative sub-transporter record, Tx_SSS. Cis accumulated for the 62 subcarriers of a SSS and the last yield is sliced and truncated to get the pined for piece width of C. The association focus is outlined in Figure 3.4.Tx_SSS is veritable regarded and is either "1" or '- 1'. Subsequently, the duplication in (4) is executed using a multiplexer (not a honest to goodness multiplier) that picks R(k) or – R(k) in light of Tx_SSS. Changing the sign of R(k) is executed by gaining the 2's supplement by bitwise invalidation took after by the extension of '1'.

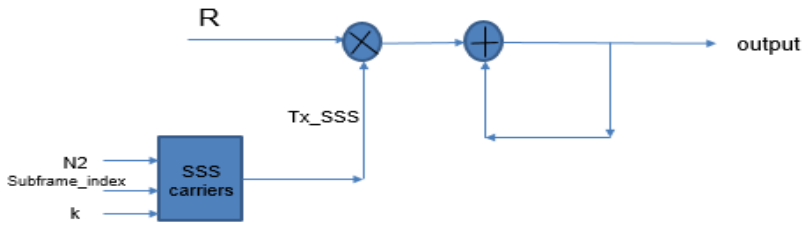

Fig 3. Block diagram of the correlation core

3.2 Magnitude calculation

The correlation yield is unpredictable, since obtained SSS is by and large perplexing. The size of an unpredictable number I+jQ is Mag = sqrt (I 2 + Q 2). For our motivations, just the relative connection between the extents of the correlation esteems is required. The CORDIC iterative calculation can be utilized for greatness estimation. A more straightforward non-iterative calculation is depicted. It assessments of the magnitude as:

$$\text{Mag} \approx \alpha * \max(|I|,|Q|) + \beta * \min(|I|,|Q|) \quad \ldots\ldots\ldots\ldots 4$$

where |. | indicates the genuine outright esteem. Utilizing α=1 and β=3/8 gives an adequate estimation blunder and a straightforward equipment usage. To compute the total estimation of I (or Q), the sign piece of I (or Q) is checked to decide if I (or Q) is sure or negative. Fig. 3.5 demonstrates that the proposed greatness estimation calculation is without multiplier.

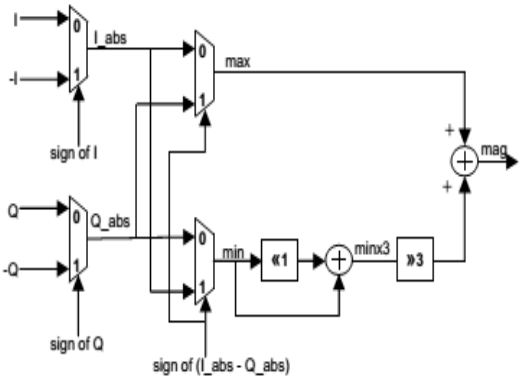

Fig 4. Block diagram of the magnitude calculation module

3.3 Peak detection

The peak detection module computes the sub-outline file and N_ID_1 that relate to the most extreme correlation size as appeared in Figure3.6. This calculation is done in parallel with correlation yield estimation without the need to review the put away yields of the 336 SSS hopefuls. This thus lessens the aggregate number of required clock cycles.

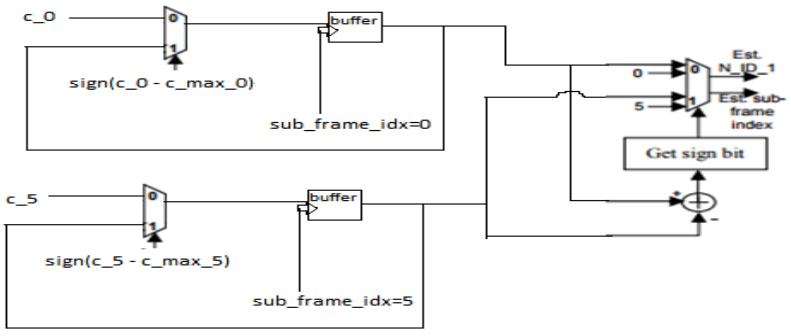

Fig 5. Block diagram of the peak detection module

3.4. Hardware architectures for SSS correlation

Parallel use of these operations is the fastest game plan, however goes to the hindrance of hardware domain and power usage. Four models are proposed and surveyed. The primary outline uses 168 parallel SSS modules and 168 parallel relationship focus modules. This building figures the duplication yield of (4) for the 168 possible estimations of N_ID_1 for a specific sub-conveyor list and a specific sub-outline record in the meantime.

This operation ought to be iterated 124 times for the 62 sub-carrier records and the two hopeful sub-outline documents (0 and 5). The second building discovers C particularly for a specific sub-outline rundown and N_ID_1 using (2). 62 parallel SSS modules

are used to make all sub-transporters for the contender SSS for a specific sub-outline rundown and N_ID_1. The hopeful SSS is copied by the gotten SSS picture, R,in a part adroit outline. The yields of these parallel multipliers (executed using multiplexers) are summed to give the relating relationship yield. This operation is iterated 336 times for all SSS hopefuls. The third plan uses 2 parallel SSS time modules and 2 parallel relationship focus modules to make the duplication yield of (4) for the two sub-outline documents meanwhile. This operation is iterated 10,416 times for the 168 estimations of N_ID_1 and for the 62 sub-bearers. The fourth plan uses a lone SSS time module and a single association focus module as showed up in Fig.4.

This delivers a single increment yield as given by (4) for a particular sub-carrier record, a particular N_ID_1, and a particular sub-outline document. This building is an all-serial plan where it completes only the fundamental operations and ought to be iterated 20,832 times. Examines the number of adders, the total size of LUTs in Kbits, the amount of flip lemon, and the amount of cycles required for each plan. Since the models use adders and no multipliers, the amount of the adders is an OK indication of the domain and the power usage.

The least conceivable system clock is 30.72 MHz, the LTE examining rate. The discovery of a SSS must be finished before the following SSS arrives, which limits SSS identification to a 5msec interim or a sum of 153,600 cycles.

This substantial number of accessible cycles permits choosing the fourth design to limit the territory. Besides, the obtaining time of this design isn't fundamentally bigger than those of alternate models, since the correlation yield is as of now found the middle value of for two images. Since the heap capacitance of a specific design is relative to its multifaceted nature (number of rationale doors), the fourth engineering will likewise bring about the most minimal power utilization for a given clock recurrence.

3.5 Adders:

3.5.1 Carry Select Adder

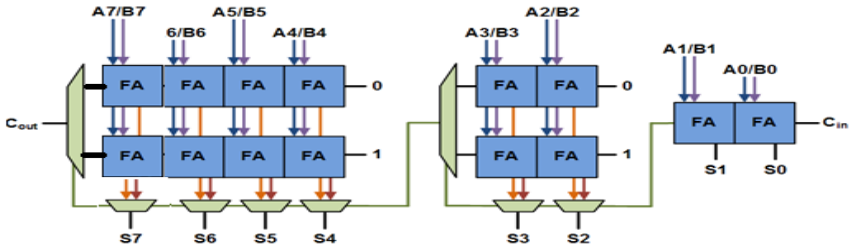

Fig 6. General Structure of CSA.

A carry-select adder is a particular way to implement an adder, which is a logic element that computes the (n+1) bit sum of two n-bit numbers. This adder is rather fast when compared to existing adders. Hence this adder has been chosen for implementation.

3.5.2 Design of PASTA:

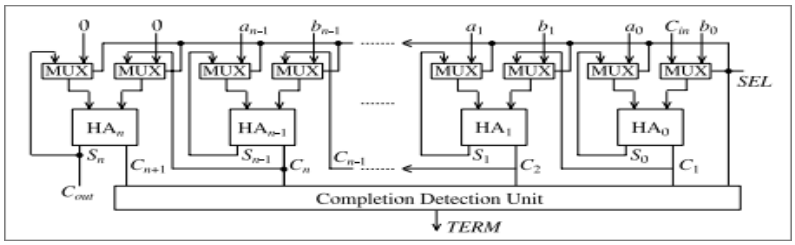

Fig 7. General Structure of PASTA

In this segment, the design and hypothesis behind PASTA is exhibited. The viper initially acknowledges two information operands to perform half augmentations for each piece. Subsequently, it emphasizes utilizing prior created convey and wholes to perform half-augmentations more than once until the point when all convey bits are expended and settled at zero level. A. Design of PASTA The general engineering of the snake is appeared in Fig. 7. The determination contribution for two-input multiplexers relates to the Req handshake flag and will be a solitary 0 to 1 progress meant by SEL. It will at first select the genuine operands amid SEL = 0 and will change to criticism/convey ways for subsequent emphases utilizing SEL = 1. The input way from the HAs empowers the various cycles to proceed until the point that the finish when all convey signs will accept zero esteems.

3.5.2.1 State Diagrams

In Fig. 8, two state outlines are drawn for the underlying stage and the iterative period of the proposed architecture. Each state is given by (Ci+1 Si) pair where Ci+1, Si represent carry out and sum values, respectively, from the ith bit adder block. Amid the underlying stage, the circuit simply acts as a combinational HA working in essential mode. It is clear that because of the utilization of HAs rather than FAs, state (11) can't show up.

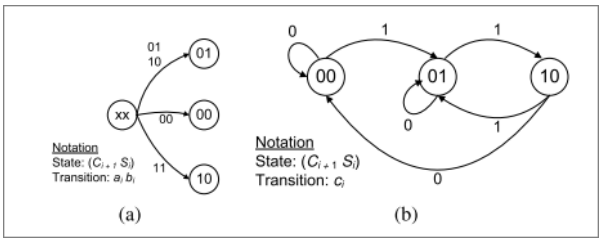

Fig. 8. State diagrams for PASTA. (a) Initial phase. (b) Iterative phase

Amid the iterative stage (SEL = 1), the criticism way through multiplexer square is initiated. The convey changes (Ci) are permitted the same number of times as expected to finish the recursion. From the meaning of key mode circuits, the present plan can't be considered as an essential mode circuit as the input– yields will experience a few advances previously creating the last yield. It isn't a Muller circuit working outside the crucial mode either as inside, a few advances will happen, as appeared in the state outline. This is comparable to cyclic sequential circuits where entryway delays are used to isolate individual states.

C. Recursive Formula for Binary Addition

Let $S^j{}_i$ and $C^j{}_{i+1}$ denote the sum and carry, respectively, for ith bit at the jth iteration. The initial condition (j = 0) for addition is formulated as follows:

$$S_i^0 = a_i \oplus b_i$$
$$C_{i+1}^0 = a_i b_i. \qquad \text{..... 5}$$

The jth iteration for the recursive addition is formulated by

$$S_i^j = S_i^{j-1} \oplus C_i^{j-1}, \quad 0 \le i < n$$
$$C_{i+1}^j = S_i^{j-1} C_i^{j-1}, \quad 0 \le i \le n. \qquad \text{..... 6}$$

The recursion is terminated at kth iteration when the following condition is met:

$$C_n^k + C_{n-1}^k + \cdots + C_1^k = 0, \quad 0 \le k \le n. \qquad \text{..... 7}$$

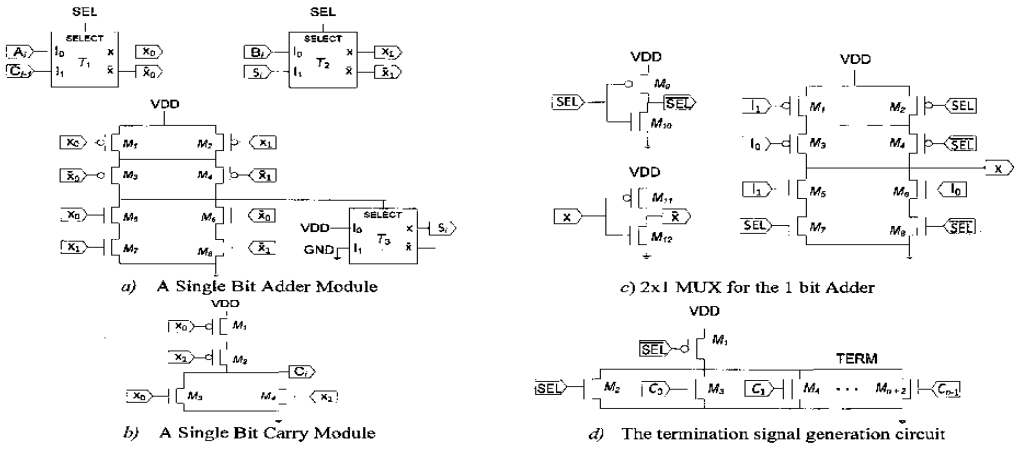

Fig. 9. CMOS implementation of PASTA.

IV. SIMULATION RESULT

4.1 Simulation:

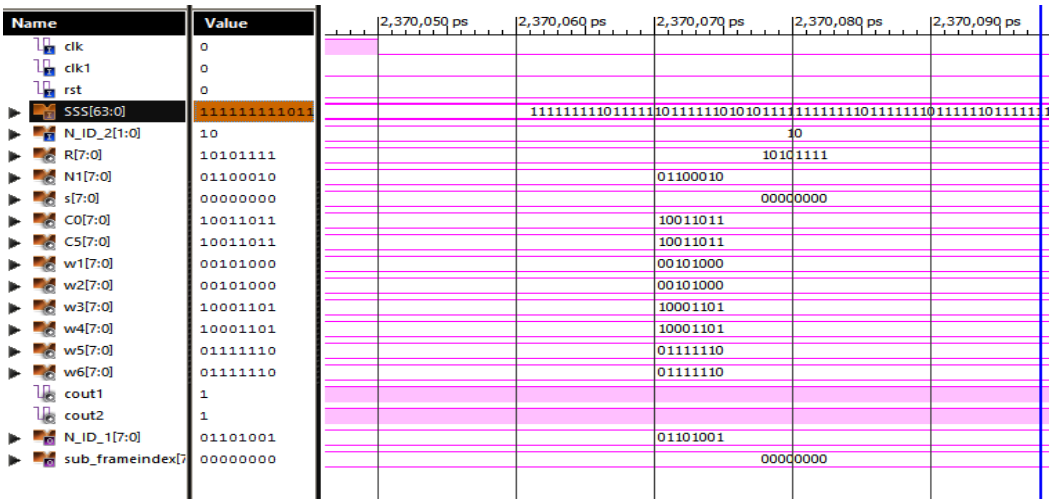

Fig. 10. Simulation results of SSS Architecture.

4.2 RTL Schematic:

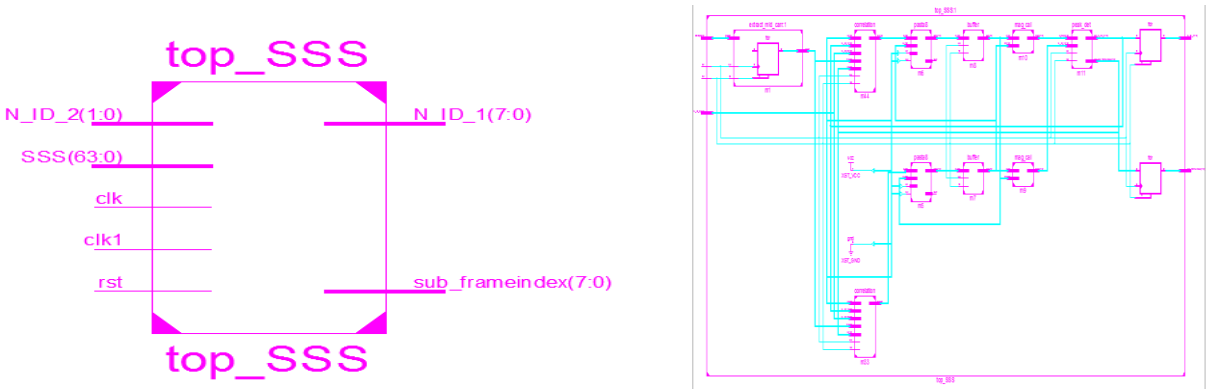

Fig. 11. RTL Schematic of SSS Architecture (left). Schematic of SSS Architecture (right).

4.3 Technology Schematic:

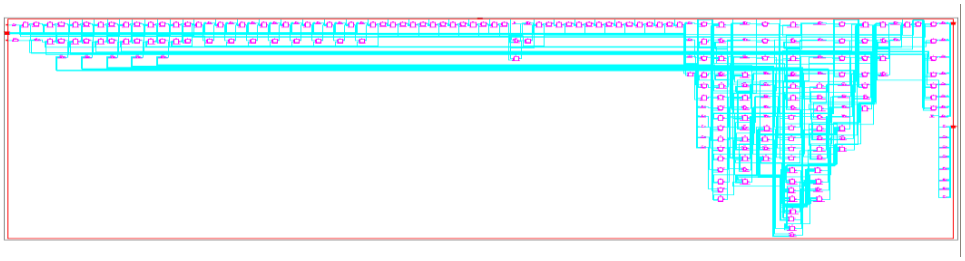

Fig. 12. Technological view of SSS Architecture.

4.4 Comparision between implementation with Carry Save Adder and PASTA:

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	116	4656	2%
Number of Slice Flip Flops	104	9312	1%
Number of 4 input LUTs	201	9312	2%
Number of bonded IOBs	35	232	15%
Number of GCLKs	2	24	8%

Fig. 13. Area utilization of SSS Architecture using CSA

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	107	4656	2%
Number of Slice Flip Flops	104	9312	1%
Number of 4 input LUTs	181	9312	1%
Number of bonded IOBs	34	232	14%
Number of GCLKs	1	24	4%

Fig. 14. Area utilization of SSS Architecture using PASTA

4.5 Timing Report:

```
                          Gate     Net
Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
----------------------------------------  ------------
 FDR:C->Q              2   0.514   0.380  sub_frameindex_0 (sub_frameindex_0)
 OBUF:I->O                 3.169          sub_frameindex_0_OBUF (sub_frameindex<0>)
----------------------------------------
Total                      4.063ns (3.683ns logic, 0.380ns route)
                                   (90.6% logic, 9.4% route)
```

Fig. 15. Timing Report of SSS Architecture using either of the architectures.

V. CONCLUS ION

This paper exhibited a total execution for the discovery of the SSS in 3GPP LTE. As accumulation is the major task in the architecture, we implemented the architecture by using the fast adder Parallel Self Time Adder (PASTA). Thus, we could still more decrease the area of the architecture compared to that using the carry select adder (CSA) by maintaining the same speed i.e., without any change in the timing.

REFERENCES

[1] Efficient Implementation of Secondary Synchronization Symbol Detection in 3GPP LTE, Amr G. Wassal, Ahmed R. Elsherif, IEEE, 2011.

[2] 3rd Generation Partnership Project, “Requirements for Evolved UTRA (E-UTRA) and Evolved UTRAN (E-UTRAN),” 3GPP TR 25.913 V9.0.0, December 2009.

[3] L. J. Cimini, Jr., “Analysis and simulation of a digital mobile channel using orthogonal frequency division multiplexing,” IEEE Trans. Commun., COM-33, pp.665-675, July 1985.

[4] Yinigmin Tsai and Guodong Zhang, “Time and Frequency Synchronization for 3GPP LTE Long Term Evolution Systems,” in IEEE Vehicular Technology Conference, 65th VTC2007, April 2007.

[5] Yinigmin Tsai, Guodong Zhang, Donald Grieco, Fatih Ozluturk, ‘‘Cell Search in 3GPP Long Term Evolution Systems,’’ IEEE Vehicular Technology Magazine, vol. 2, issue 2, June 2007. [5] 3rd Generation Partnership Project, ‘‘Evolved Universal Terrestrial Radio Access (E-UTRA); Physical Channels and Modulation,’’ 3GPP TS 36.211 V9.1.0, March 2010.

[6] E Dahlman, S. Parkvall, J. Sköld, P. Beming, 3G Evolution HSPA and LTE for Mobile Broadband. Academic Press, 2007.

[7] K. Manolakis, D. Est´evez, V.Jungnickel, W. Xu, C. Drewes, “A Closed Concept for Synchronization and Cell Search in 3GPP LTE Systems,” in IEEE Wireless Communications and Networking Conference. Proceedings, WCNC 2009.

[8] 3rd Generation Partnership Project, “Evolved Universal Terrestrial Radio Access (E-UTRA); User Equipment (UE) radio transmission and reception,” 3GPP TS 36.101 V9.3.0, March 2010. [9] Richard. G. Lyons, Understanding Digital Signal Processing. Addison Wesley, 1997