A NOVEL APPROACH TO RESTRAIN VOLTAGE AND POWER BALANCE USING CASCADED H-BRIDGE CONVERTER INSTIGATED FOR A SOLID- STATE TRANSFORMER

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***Abstract*: In this Paper, the designing of the solid-state transformer SST, including ac/dc rectifier, dual active bridge (DAB) converters are developed. The SST is an interconnection device between ac distribution grids and dc distribution systems. The SST has a cascaded multilevel ac/dc rectifier stage, a dual active bridge (DAB) converter stage with high-frequency transformers, and an obligatory dc/ac stage. On the other hand, due to dc-link voltage and power unbalance in the cascaded modules, the unbalanced dc-link voltages and power intensify the pressure of the semiconductor devices and set off overvoltage or over-current issues.**

***Keywords*: Cascaded H-Bridge converter, DQ vector restrain, Solid-state transformer (SST), Voltage and power balance.**

I INTRODUCTION

In the role of the interconnection between power transmission grids and the consumers, the distribution power system currently requires 60 Hz transformers for voltage transformation. These ordinary copper- and-iron based transformers acquire many undesirable properties including bulky size, ecological concerns and especially power quality susceptibility. The solid-state transformer (SST) is the interconnection device between the distribution system and the electricity consumer's in future smart grid systems. In the schemed electric configuration of the smart grid system shown in Fig. 1, low voltage (120 V), residential class distributed renewable energy resource (DRER), distributed energy storage device (DESD), and loads are connected to the 400-V dc distribution bus and then to distribution bus through a SST. The SST is used to enable active management of DRER, DESD, and loads, rather than a 60-Hz ordinary transformer.

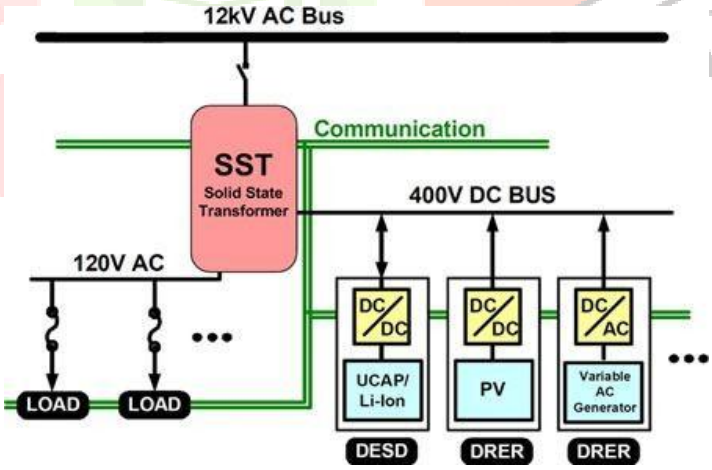


Fig.1. SST at one residential home

This paper intends a 20-KVA cascaded H-Bridge multilevel converter-based SST to directly interconnection with 7.2-kV single-phase distribution voltage level. As shown in Fig. 2, the SST subsist of a cascaded multilevel ac/dc rectifier, dual active bridge (DAB) converters with high-frequency transformers. The regulated 400-V dc bus is distributed for easier connection of battery and other distributed resources.

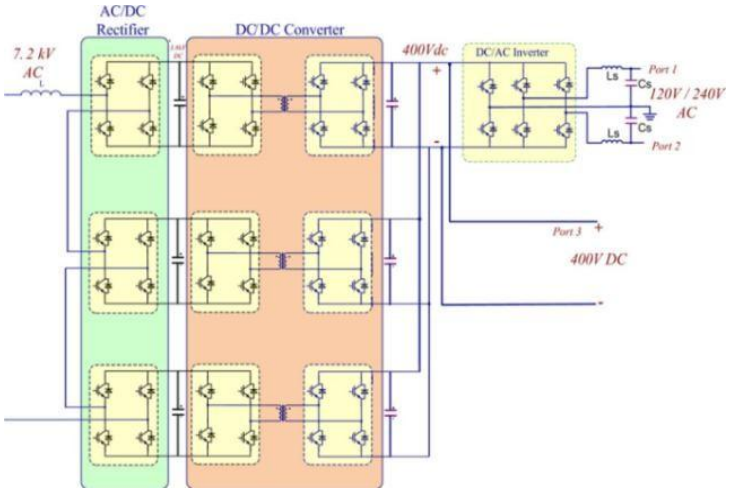


Fig. 2. Topology of the schemed SST.

II SST DESIGNING AND RESTRAIN

The designing and restrain of the SST, including the cascaded multilevel ac/dc rectifier, DAB converters with high-frequency transformers are developed in this section.

The fundamental configuration of the schemed 20- kVA SST is shown in Fig. 2.

A. Rectifier Single-Phase dq Vector Restrain

The ac/dc rectifier stage transfers the single-phase 7.2-kV ac voltage to three dc-link voltages while restraining the reactive power at the input side. The average unusual equations of the rectifier are

$$\frac{di_a}{dt} = \frac{3E}{L_s}d_a - \frac{V_{pcca}}{L_s} - \frac{R_s}{L_s}i_a$$

$$\frac{dE}{dt} = -\frac{E}{R_L C} - \frac{d_a i_a}{C}$$

Where, im is the input current of the imaginary phase, V is the input voltage of the imaginary phase, E is the dc-link voltage of the imaginary phase, dm is the rectifier PWM duty cycle.

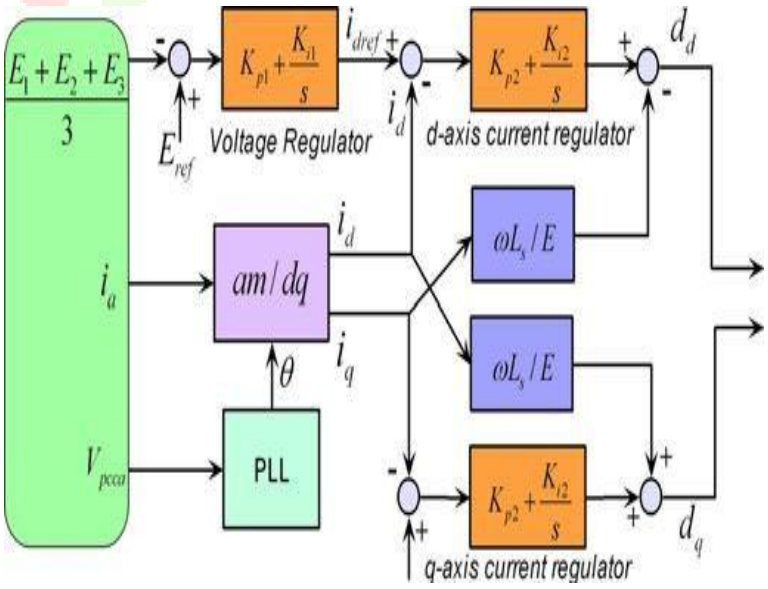


Fig. 3. Rectifier single-phase dq decoupled controller.

The decoupled dq vector controller for each H-bridge is shown in Fig. 3. The three sinusoidal pulse width modulation (SPWM) carriers for the cascaded H- Bridge are phase shifted. Depending on the reactive power base in the SST controller I, the SST can generate or captivate reactive power to the power grid.

B. Designing and Restrain of DAB

The DAB is shown in Fig. 4. The rectifier regulates the high-voltage dc-link voltage and manipulates the input current to be sinusoidal from the ac input. The low-voltage dc link is regulated by the DAB converter.

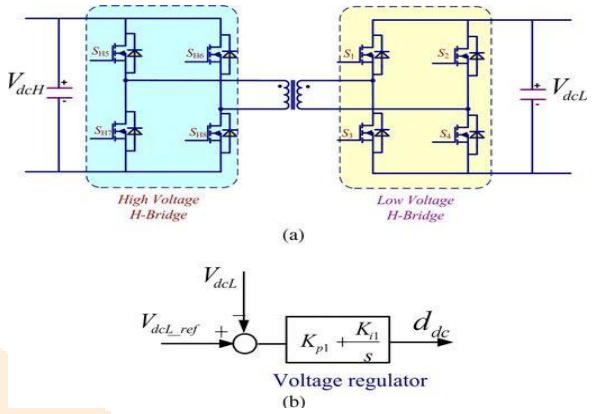


Fig. 4. (a) DAB circuit and (b) DAB voltage controller.

The DAB scheme presents zero voltage switching, relatively low-voltage pressure for the switches, low passive component. Real power flows from the bridge with leading phase angle to the bridge with lagging phase angle, the amount of transferred power is controlled by the phase angle difference and the magnitudes of the dc voltages at the two ends.

III VOLTAGE AND POWER BALANCE RESTRAIN

Because the rectifier stage of the SST subsist of three H-Bridges in series, the voltage unbalance could appear on the dc-link voltages due to the device loss mismatching and H-Bridge real power differences. The unbalanced voltage will set off the capacitor or IGBT device overvoltage in the H-Bridge and trigger the system overvoltage fortification.
The DAB stage subsist of three DAB modules in parallel. The power unbalance (P1, P2 and P3, as shown in Fig. 5) can be set off by the transformer parameter mismatching (such as leakage inductance or turns ratio) and dc-link voltage differences. The power unbalance will set off a device overcurrent issue and result in unbalance heat distributions.

A. Voltage Balance Restrain

The single-phase dq vector controller for the rectifier stage regulates the total dc-link voltage and manipulates the reactive power. Fig. 6 illustrates the schemed voltage balance controller. The individual dc-link voltages of the first two H-Bridges, E1 and E2 are compared with the dc-link voltage base E3 to generate d-axis compensation Δdd1 and Δdd2 by a PI regulator. Fig. 7 shows the three dc-link voltages without voltage balance restrain. The three H-Bridge dc-link voltages become unbalanced after the power change. The H-bridge that transfers more power has the highest dc-link voltage. Fig. 8 shows the three dc- link voltages with voltage balance restrain. With the voltage balance controller, the three dc-link voltages are equally regulated in the steady state.

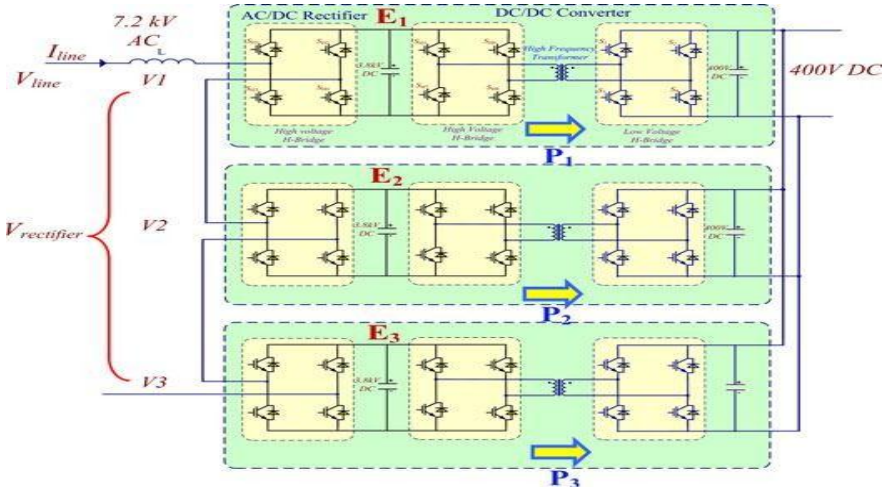


Fig. 5. Voltage and power unbalance in SST topology.

B. Voltage Balance Constraints

The schemed voltage controller can maintain the evenhanded dc-link voltage while the real power is unusual for each H- Bridge. The derivations are based on the assumption of a unity power factor at the SST rectifier input

$$V_1 + V_2 + V_3 = V_{\text{line}} - j\omega L I_{\text{line}}$$
$$V_1 = (d_1 + jq_1)E,\ V_2 = (d_2 + jq_2)E$$
$$V_3 = (d_3 + jq_3)E$$

where, Vn is the Nth H-Bridge voltage vector, V is the single phase input ac voltage, I line is the input ac current, dn and qn are the d-axis and q-axis duty cycle generated by the controller, and E is the dc-link base voltage of each H-Bridge.

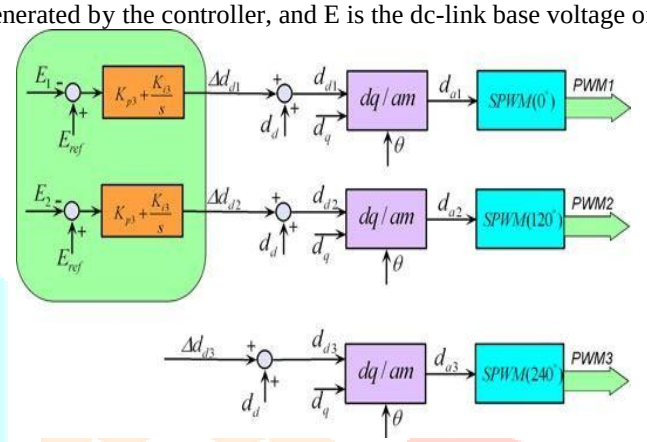


Fig. 6. Schemed voltage balance restrain based on the single- phase dq

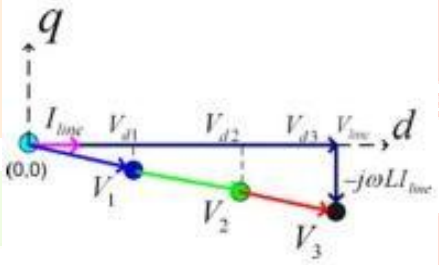


Fig. 7. Rectifier voltage vector constrains.

The real power PN and reactive power QN of the Nth H-Bridge is calculated as

$$P_1 + jQ_1 = I_{\text{line}}V_1 = I_{\text{line}}(d_1 + jq_1)E$$
$$P_2 + jQ_2 = I_{\text{line}}V_2 = I_{\text{line}}(d_2 + jq_2)E$$
$$P_3 + jQ_3 = I_{\text{line}}V_3 = I_{\text{line}}(d_3 + jq_3)E.$$

So from above equations the total input power

$$P_1 = I_{\text{line}} d_1 E \qquad (18)$$
$$P_{\text{in}} = \sum_{1}^{N=3} P_n = I_{\text{line}} V_{\text{line}}, \text{ so}$$
$$I_{\text{line}} = \frac{P_{\text{in}}}{V_{\text{line}}}. \qquad (19)$$

From above equations, d1, d2, and d are derived as

$$d_1 = \frac{P_1}{P_{\text{in}}}\frac{V_{\text{line}}}{E},\quad d_2 = \frac{P_2}{P_{\text{in}}}\frac{V_{\text{line}}}{E},\quad d_3 = \frac{P_3}{P_{\text{in}}}\frac{V_{\text{line}}}{E}. \qquad (20)$$
$$d_1 \geq d_2 \geq d_3$$

Without loss of generality, assume, the reactive power is equally distributed and no over modulation. In contract to balance the dc-link voltages, the real power of each H-Bridge has to be within the range conferred in (21).

$$d_1^2 + q_1^2 \leq 1.$$

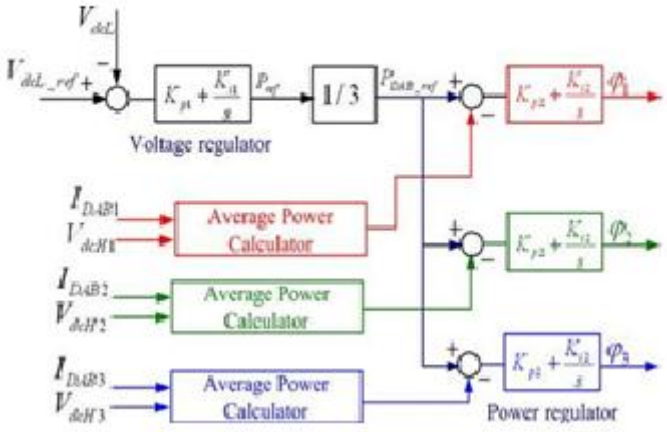


Fig. 8. Power balance controller.

C. Power Balance Restrain

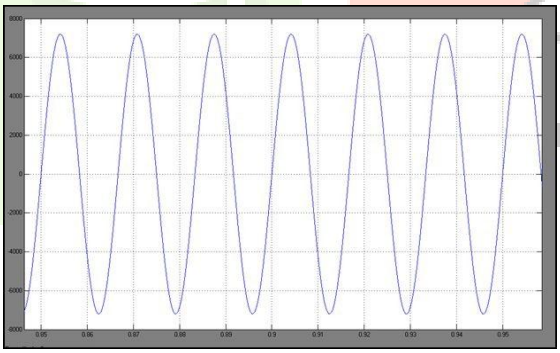
A power balance restrain procedure is schemed to regulate the real power transferring through the DAB parallel modules. As shown in Fig. 8, the voltage regulator compares the low-voltage dc voltage Vdc L with the base Vdc L ref and generates the power bases Pre f for the three DAB modules. Then, the power regulator compares the calculated average power of each DAB module with Pre f and generates the phase-shift angles □1, □2, and □3 for the three calculates the average power in each switching cycle. In the calculation,

$$P = \int_0^{\pi} V_{dcH} i_p dt,$$

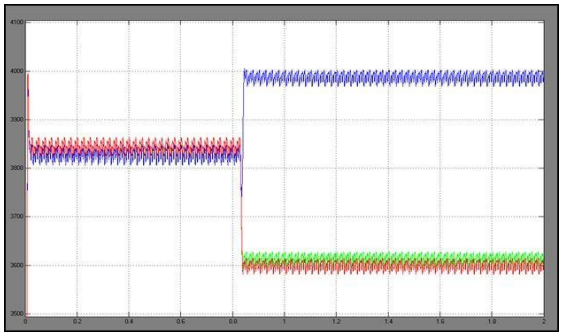
The primary dc voltage V_{dcH} module is even handed. So the power calculation involves only the summation of current.

I. SIMULATION RESULTS

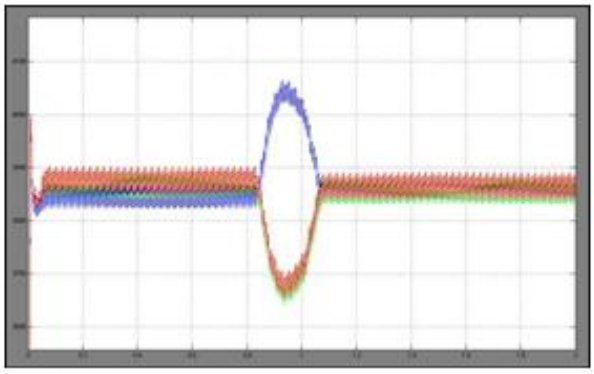
The simulation results confirm the study of maximum power unbalance threshold; then the proposed power controller is necessary to assure the power unbalance is always restricted within the essential range so that the dc-link voltages can be balanced.



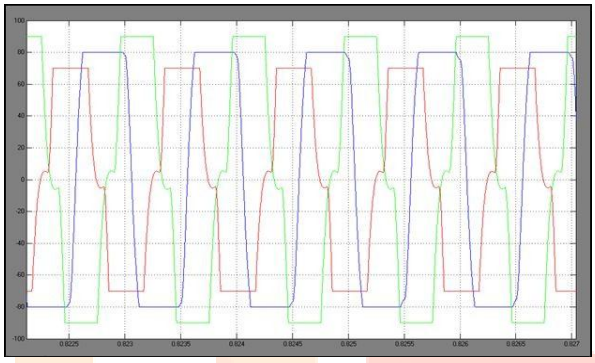
Input voltage



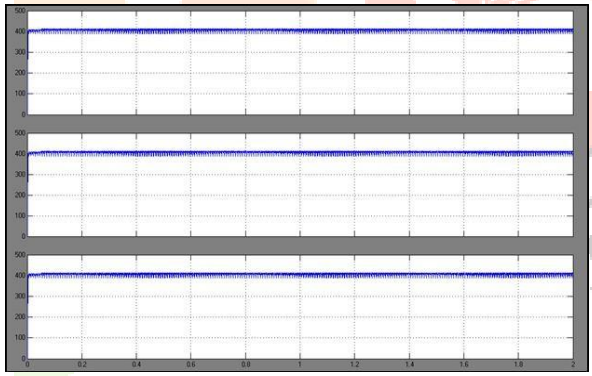
DC-link voltages without voltage balance control



DC-link voltages with voltage balance control



DAB current without power balance control



DC bus voltages

In the proposed model, PI controller is used but in the extension the PI controller is replaced by the P+R controller and the results obtained shown that the steady state achievement is faster than that of PI controller. The results with P+R controller is shown below:

CONCLUSION

In this paper, a cascaded H-Bridge converter-based SST is schemed to interconnection between 7.2-kV ac grid and a 400-V dc distribution in smart grid systems. The single-phase dq vector designing and restrain of the SST, including ac/dc rectifier, DAB converter is developed. A new voltage balance restrain procedure is schemed to resolve the voltage unbalance of the dc links in different H-bridges. The power intrinsic unbalance constraints of the voltage balance restrain for the cascaded H-Bridge rectifier is derived and verified by simulations. Mean-while, a power balance restrain procedure is schemed to regulate the real power transferring through the parallel modules. Finally, the switching model simulation and SST scale-down prototype are instigated with the schemed controller. The results confirm the performance of the SST, including power factor correction, real and reactive power restrain, voltage sag compensation, and the schemed voltage balance restrain.

REFERENCES

[1] Voltage and Power Balance Control for a Cascaded H-Bridge Converter-Based Solid-State Transformer, Tiefu Zhao, Senior Member, IEEE, Gangyao Wang, Student Member, IEEE, Subharshish Bhattacharya, Member, IEEE, and Alex Q. Huang, Fellow, IEEE

[2] J.S.Lai and F. Peng, "Multilevel converters—A new breed of power con- verter," IEEE Trans. Ind. Electron., vol. 32, no. 3, pp. 509–517, May/Jun.1996.

[3] E. R. Ronan, S. D. Sudhoff, S. F. Glover, and D. L. Galloway, "A power electronic-based distribution transformer," IEEE Trans. Power Del., vol. 17, no. 2, pp. 537–543, Apr. 2002.

[4] J. S. Lai, A. Maitra, A. Mansoor, and F. Goodman, "Multilevel intelligent universal transformer for medium voltage applications," in Proc. Conf. Rec. Ind. Appl. Conf., 40th IAS Annu. Meeting., Oct. 2005, vol. 3, pp. 1893–1899.

[5] T. Zhao, J. Zeng, S. Bhattacharya, M. E. Baran, and A. Q. Huang, "An average model of solid state transformer for dynamic system simulation," in Proc. IEEE Power Energy Soc. Gen. Meeting, Jul. 2009, pp. 1–8.

[6] Q. Song, W. Liu, Z. Yuan, W. Wei, and Y. Chen, "DC voltage balancing technique using multi-pulse optimal PWM for cascade H-bridge inverters based STATCOM," in Proc. IEEE 35th Annu. Power Electron. Spec. Conf.,2004, pp. 4768–4772

[7] C. Cecati, A. Dell'Aquila, M. Liserre, and V. G. Monopoli, "Design of H-bridge multilevel active rectifier for traction systems," IEEE Trans. Ind. Appl., vol. 39, no. 5, pp. 1541– 1550, Sep./Oct. 2003

[8] J. A. Barrena, L. Marroyo, M. A. R. Vidal, and J. R. T. Apraiz, "Individual voltage balancing strategy for PWM cascaded h-bridge converter-based STATCOM," IEEE Trans. Ind. Electron, vol. 55, no. 1, pp. 21–29, Jan.2008.

[9] H. Iman-Eini, J.-L. Schanen, S. Farhangi, and J. Roudet, "A modular strategy for restrain and voltage balancing of cascaded H-bridge rectifiers," IEEE Trans. Power Electron., vol. 23, no. 5, pp. 2428–2442, Sep. 2008.

[10] J. I. Leon, R. Portillo, S. Vazquez, J. J. Padilla, L. G. Franquelo, and J. M. Carrasco, "Simple unified approach to develop a time-domain mod- ulation strategy for single-phase multilevel converters," IEEE Trans. Ind. Electron., vol. 55, no. 9, pp. 3239–3248, Sep. 2008.

[11] J. A. Barrena, L. Marroyo, M. A. Rodriguez, and J. R. Torrealday, "A novel PWM modulation strategy for DC voltage balancing in cascaded H- bridge multilevel converters," in Proc. EUROCON, 2007, pp. 1450–1456.

[12] C. Han, A. Q. Huang, Y. Liu, and B. Chen, "A generalized restrain strat- egy of per-phase DC voltage balancing for cascaded multilevel converter based STATCOM," in Proc. IEEE Power Electron. Spec. Conf., Jun. 2007, pp. 1746– 1752.

[13] R. Zhang, M. Cardinal, P. Szczesny, and M. Dame, "A grid simulator with restrain of single-phase power converters in D-Q rotating frame," in Proc. IEEE 33rd Annu. Power Electron. Spec. Conf., 2002, vol. 3, pp. 1431–1436.

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