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Analysis Of Power Performance Of Class E Amplifier For High Frequency Radio Applications

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Abstract: We present a fully integrated single-stage power amplifier operating. Among all non-linear power amplifier classes, the class-E power amplifier stands out for its simplicity and high efficiency. In order to create the suggested power amplifier at 1.8V, this class was selected. Using the same transistors at the same frequency and output power, class-E amplifiers often operate with power losses that are around 2.3 lower than those of traditional class-B or class-C amplifiers. Because of the input waveform's strong driving, the common source transistor functions as a basic switch when in use. As long as the cascode bias voltage Vb is high enough to place transistor M2 in the triode region, the voltage can rise to a point where the common gate transistor is also switched. This configuration improves the amplifier's dependability by allowing for less swing in the drain-gate voltage.

Our solution improves gain, bandwidth stability, and linearity over the operational spectrum by utilizing an inductively degraded common-source CMOS power amplifier in conjunction with a cascode topology. While noise figure typically holds less relevance in power amplifier design, we optimize the matching network to minimize noise figure and maximize power gain The suggested circuit has been successfully designed and implemented using Cadence Virtuoso tools at 45nm, 90nm & 180nm technology. This paper depicts a comparison of power of the RF Amplifier of Class E with respect to 180nm technology with the referenced paper[1] where the power consumption is observed as 10.69mWatts for 180nm where in our paper power consumption is reduced to 3.669uWatts.

Keywords –CMOS (Complementary Metal Oxide Semiconductor), RF Amplifier (Radio Frequency Amplifier), SNR (Signal to noise ratio), comparison, performance evaluation

I.INTRODUCTION

In RF front-end circuits, gallium arsenide (GaAs), silicon bipolar, and BiCMOS are widely used technologies that provide benefits over CMOS technology reduced substrate voltage and increased breakdown voltage loss, and improved monolithic inductors and capacitors. These technologies cost a lot more money, though. RF front-end circuits using CMOS technology enable a single-chip solution, which significantly reduces costs. CMOS RF circuits can now be produced with performance close to those of advances in CMOS technologies as well as silicon bipolar, GaAs, and BiCMOS. CMOS techniques have been used to produce receiver essentials including as IF filters, frequency synthesizers, mixers, and LNAs. Despite these advancements, not much is known about CMOS power amplifiers, particularly when the supply voltage is low and performance suffers. CMOS circuits for RF front-end.

II.LITERATURE SURVEY

[1]Wael Abdullah, Emad Hegazi "Dynamic Supply RF Power Amplifier"

Since RF power amplifiers typically consume the most power in portable communication devices, it is important to design them to be as power-efficient as possible in order to prolong battery life. They ought to remain sufficiently linear to maintain the transmitted signal's integrity. Efficient PA classes are intrinsically non-linear, whereas linear PAs are usually not power efficient. In recent years, numerous books and studies have examined the trade-off between PA efficiency and linearity; it is unusual to attain both high linearity and high efficiency at the same time. The goal of this study is to design and build a radio frequency (F) power amplifier (P A) operating at 2.14GHz and 24dBm class-A. The next step to enhance efficiency is to use a DC-DC converter to dynamically regulate the constant supply voltage to manage the voltage.

[2]Anh-Vu Pham, Duy P. Nguyen, and Mohammad Darwish "High Efficiency Power Amplifiers for 5G Wireless Communications"

In this paper, we will present the overview of 5G wireless communications.We then discuss the trend and performance of millimeter-wave power amplifiers reported in the field. We will review the performance of power amplifiers in different semiconductor technologies in terms of output power,power added efficiency and linearity. Doherty power amplifiers are attractive candidates for 5G wirelesscommunications. Doherty power amplifiers and linearization techniques to achieve high efficiency and linearity in millimeter-wave frequencies. The presented power amplifiers have applications in the 5G wireless communications. Here we demonstrate that E-mode GaAs pHEMT Doherty power amplifiers are attractive candidates for 5G wireless communications. They can be designed and developed in a very compact size toreduce the cost of a die area. In addition, the presented millimeter-wave have high efficiency at peak andpower back-off that are comparable to those at low frequencies. In recent years, the development of 5G wireless communications has created challenges and opportunities for millimeter-wave circuits and components.

[3] Ahsan Javed Awan and Peter Wilson "Low Power High Speed Operational Amplifier Design Using Cadence"

The design space that optimizes the performance of operational amplifier in terms of current consumption and unity gain band width product has been explored using Cadence. A two-stage indirect compensated active load cascade operational amplifier with a current consumption of 335uA and a speed as high as 23MHz has been presented. The parasitic effects decrease the slew rate and unity gain bandwidth so it is better to add a safety margin of 5 to 10% on the original specifications in order to reduce the probability of iterating through the simulation phase again. Three designs have been presented all of which meet minimum design criteria and three stage opamp design provides an optimum solution for higher speed and low power consumption. Moreover, it is also optimized with respect to area. Though the three stage opamp design meets the minimum design criteria even with 15% supply voltage variations, its robustness can be increased by the cascaded version of beta multiplier.

[4] A D-band CMOS PowerAmplifier for Wireless Chip-to-Chip Communications with 22.3 dB Gain and 12.2 dBm P1dB in 65-nm CMOS Technology" by H. S. Son, C. J. Lee, D. M. Kang, T. H. Jang, H. S. Lee, S. H. Kim, C. W. Byeon, and C. S. Par

D-band linearized power amplifier (PA) covering 114 to 131 GHz, featuring on-chip current combining transformer, utilizing a conventional 65nm CMOS technology. This work describes a D-band linearized power amplifier (PA) covering 114 to 131 GHz that uses a typical 65nm CMOS technology. It also includes an on-chip current combining transformer. Every stage features a common source (CS) amplifier with a cross-coupled capacitor (Cc) neutralization to reduce the parasitic gate-drain capacitance feedback. The peak PAE of the PA is 10.2%. Its small-signal gain is 22.3 dB, and its 3-dB bandwidth (BW) is 17 GHz. Its 1-dB compressed power (P1dB) is 12.2 dBm, and its saturated output power (PSAT) is 14.5 dBm. The core chip area is 0.103mm2, and the PA chip area, with the pads included, is 0.343mm2.

[5] Awakhare, Manoj Sharadrao, "A CMOS class-E cascode power amplifier for GSM application," International Journal of Recent Technology and Engineering (TJRTE), Volume 3, Issue 2, May 2014..

A Class E cascode power amplifier (PA) topology intended for GSM applications is proposed in the paper "A CMOS Class-E Cascode Power Amplifier for GSM Application" by Manoj Sharadrao Awakhare, which was published in the International Journal of Recent Technology and Engineering (TJRTE) in May 2014. The single-stage design of this topology is intended to reduce device stress issues. To improve efficiency and mitigate the impact of parasitic capacitances at the drain node, a parallel capacitor is connected across the transistors. The paper's importance in the field of wireless communication systems is demonstrated by the numerous research works that quote it. It has been brought up, for example, in conversations concerning the linearity of the circuit with a 50-ohm load—a crucial consideration when building modules for wireless communication systems. By introducing the idea of mode-locking, the work also advances knowledge of the CMOS implementation of Class E power amplifiers for wireless communications.

[6] In September 2010, the International Journal of Electronics and Communications published a paper by Dr. Sohiful Anuar Zainol Murad titled "A 2.4-GHz 0.18-11m CMOS class E single-ended switching power amplifier with a self-biased cascode."

The design and development of a 0.18-µm process-based CMOS-based PA operating in the 2.4 GHz frequency spectrum are discussed in the study. One notable innovation that aims to increase the PA's performance and efficiency is the self-biased cascode setup. For wireless applications, where maintaining signal quality and range requires high output power and power economy, this strategy is essential. Contributions of the research include comprehensive analysis and simulation results showing the effectiveness of the suggested PA architecture. It is an invaluable tool for engineers and academics working on wireless communication systems because it sheds light on the amplifier's efficiency, power gain, and other crucial performance metrics. A thorough experimental setup and analysis, including measurements of the amplifier's output power, efficiency, and other performance parameters, bolster the paper's conclusions. This meticulous methodology guarantees that the suggested design satisfies the demanding specifications of Class E power amplifiers, which are necessary to achieve high performance in wireless communication applications and to comply with regulatory norms.

III.METHODOLOGY

BLOCK DIAGRAM

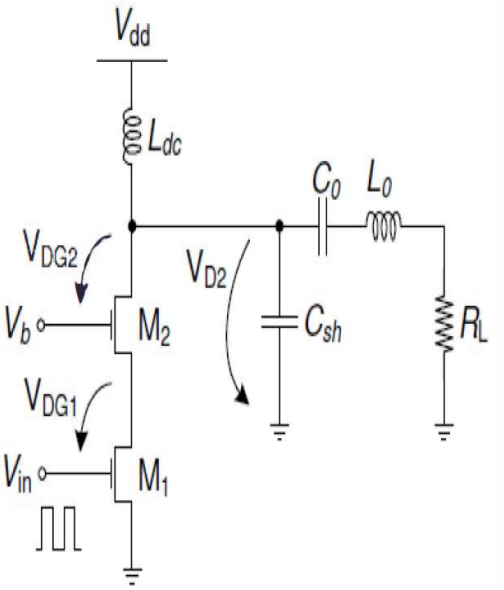


FIG 1: Cascode Class-E Amplifier

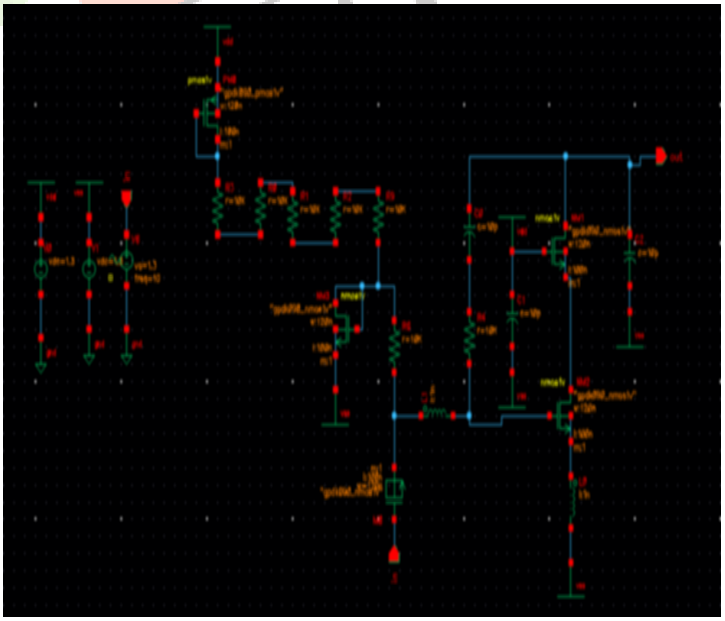


FIG 2: Proposed PA design in Cadence Virtuoso

EXPLANATON OF BLOCK DIAGRAM

The class-E power amplifier is the most straightforward and efficient of all the non-linear power amplifier classes. In order to create the suggested power amplifier at 1.8V, this class was selected. Using the same transistors at the same frequency and output power, class-E amplifiers often operate with power losses that are around 2.3 lower than those of traditional class-B or class-C amplifiers. The figure shows a conventional cascade architecture class-E amplifier. Because of the input waveform's strong driving, the common source transistor functions as a basic switch while in use. As long as the cascode bias voltage Vb is high enough to place transistor M2 in the triode region, the voltage can rise to a point where the common gate transistor is also switched. This configuration improves the amplifier's dependability by allowing for less swing in the drain-gate voltage.

Furthermore, by lowering the Miller multiplication effect, this approach improves the input-output isolation and stability of the amplifier. One significant benefit of the common-source, common-gate (CS, CO) architecture is that it allows for independent optimization of linearity and noise by focusing on the CS and CO transistors independently. Reverse isolation and stability are enhanced by the CO amplifier's drain-gate capacitance of the CG transistor, which is not linked between the amplifier's input and output like it is in the CS amplifier. Additionally, if the transconductance of the CS and CG is equal, the voltage gain of the CS is almost unity due to the modest input resistance of the CO. As a result of its drain-to-gate parasitic capacitance, the Miller capacitance that appears at the CS's input is extremely modest. The suggested PA in this study uses the similar topology.

As seen in Figure 2, a self-biasing cascode amplifier makes it possible to construct a PA in which the maximal gate-drain voltage is reached by both transistors. This leads to an RF swing at D2, which is followed by the deterioration of hot carriers. Rb-Cb supplies the bias for G2, and the DC voltage applied to 02 is equal to the DC voltage applied to D2. The low-pass characteristic of Rb-Cb attenuates the RF swing. For best results, Rb-Cb values that are equivalent to M1's gate-drain swing can be selected.

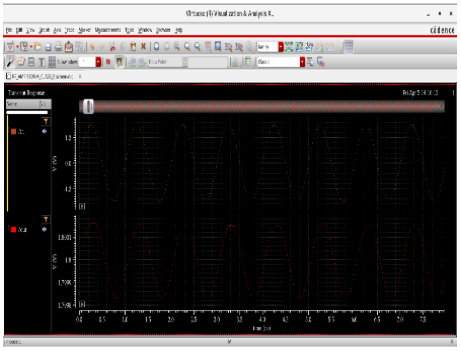
IV. COMPARISON TABLE

Class	Ideal Efficiency	Linearity	Practical Efficiency	Process
Class A	50%	Good	35%	SOI0.5umCMOS
Class AB	50%-78.5%	Good	45%	0.35umCMOS
Class B	78.5%	Moderate	49%	PHEMT
Class C	78.5%-100%	Poor	55%	0.6umCMOS
Class E	100%	Poor	62%	0.35umCMOS
Class F	100%	Poor	80%	PHEMT

1. Class A
   - Class A amplifiers are characterized by continuous conduction of output devices throughout the entire input cycle.
   - Ideal Efficiency: Around 50% due to constant power dissipation.
   - Linearity: Excellent due to low crossover distortion.
   - Practical Efficiency: Typically around 35% due to continuous operation.
   - Process: Often implemented using technologies like SOI (Silicon-on-Insulator) CMOS for low-power applications where linearity is critical.

2. Class AB
   - Class AB amplifiers operate primarily in Class A but transition to Class B operation at low output levels to improve efficiency.
   - Ideal Efficiency: Typically between 50% and 78.5%, depending on biasing.
   - Linearity: Good, balancing between efficiency and linearity.
   - Practical Efficiency: Higher than Class A, often around 45%.
   - Process: Implemented using advanced CMOS processes for better efficiency and linearity.

3. Class B
- Class B amplifiers conduct for only half of the input cycle, reducing power dissipation but introducing crossover distortion.
- Ideal Efficiency: Around 78.5% due to reduced conduction losses.
- Linearity: Moderate due to crossover distortion.



- Practical Efficiency: Typically around 49%.
- Process: Often implemented using technologies like PHEMT (Pseudomorphic High Electron Mobility Transistor) for applications where efficiency is crucial, such as in power amplifiers.

4. Class C
- Class C amplifiers conduct for less than half of the input cycle, resulting in high efficiency but poor linearity.
- Ideal Efficiency: Ranges from 78.5% to 100%.
- Linearity: Poor due to high levels of distortion.
- Practical Efficiency: Typically around 55%, making them suitable for RF (Radio Frequency) applications where high efficiency is paramount.
- Process: Implemented using processes optimized for RF performance, such as 0.6µm CMOS.

5. Class E
- Class E amplifiers operate as switch-mode amplifiers, achieving theoretical maximum efficiency by minimizing switching losses.
- Ideal Efficiency: 100%.
- Linearity: Poor due to operating in a non-linear switching mode.
- Practical Efficiency: Typically around 62%, making them ideal for high-frequency power amplifiers.
- Process: Implemented using advanced CMOS processes optimized for high-frequency operation, such as 0.35µm CMOS.

6. Class F
- Class F amplifiers optimize efficiency by shaping the output waveform to reduce power dissipation.
- Ideal Efficiency: 100%.
- Linearity: Poor due to waveform shaping.
- Practical Efficiency: Typically around 60%, making them more efficient than Class C amplifiers.
- Process: Often implemented using technologies like PHEMT for high-frequency applications.

V. RESULTS AND DISCUSSION

1. Transient Response

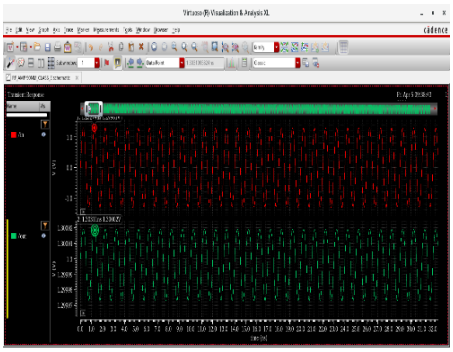


FIG 3: Transient Response of 45nm FIG 4: Transient Response of 90nm FIG 5:Transient Response of 180nm

2 Power Consumption:

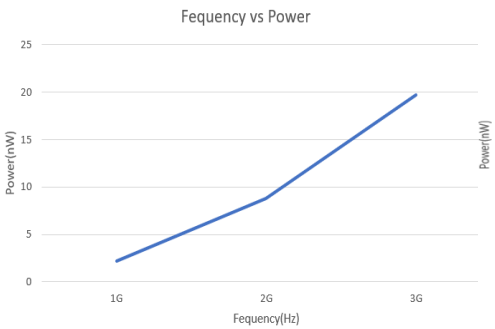


FIG 6:45nm Power Consumption

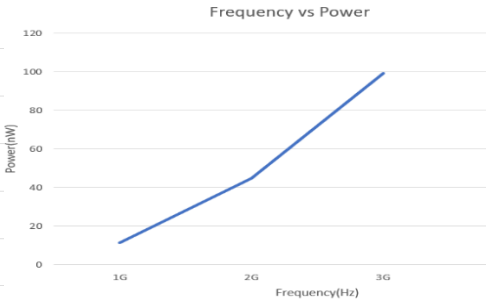


FIG 7: 90nm Power Consumption

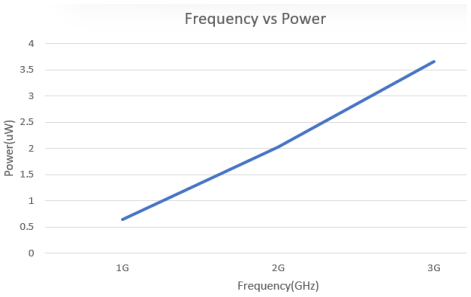


FIG 8: 180nm Power Consumption

The Below table gives the comparison of results of 180 nanometer technology.

Parameters	This work	[1]	[6]	[8]	[9]	[10]	[7]	[3]
Frequency	3GHz	2.4GHz	3.1-4.8GH	2.4GHz	2.4GHz	3.1-4.8	3.0-4.0	3.1-4.8
Supply voltage(V)	1.8	1.8V	1	3.3	2.5	0.18	....	1.9
Power Consumption	3.669uW	10.69mW	22mW	....	....	25mW	....	....

The Below table gives the comparison of results between 45nm, 90nm and 180nm technology.

Parameters	This work								
Nanometer technology	45nm			90nm			180nm		
Frequency	1G	2G	3G	1G	2G	3G	1G	2G	3G
Supply voltage(V)	1	1	1	1.3	1.3	1.3	1.8	1.8	1.8
Power Consumption	2.209nW	8.803nW	19.69nW	11.32nW	44.84nW	99.43nW	650.2nW	2.021uW	3.669uW

VI. CONCLUSION

Power Consumption

A comparison of performance parameters for a 180 nm technology node at different frequencies and supply voltages is shown in the data. The supply voltages of 1.8V and 1.9V correspond to the frequency range of 2.4GHz to 3.1-4.8GHz. The power usage, which ranges from 3.669uW to 22mW, fluctuates greatly depending on the working circumstances.

- Power consumption tends to increase with technological advancements. For example, at 45nm technology, power consumption ranges from 2.21X10-9nw (1G) to 650X10-9nw (3G), showing a significant increase from 1G to 3G.
- This trend suggests that while newer technologies offer improved performance, they may require more power to operate.

Overall, the data suggests that as the technology node decreases (from 180nm to 45nm), there's a reduction in power consumption across different frequencies and supply voltages.

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