IJCRT.ORG ISSN : 2320-2882

INTERNATIONAL JOURNAL OF CREATIVE RESEARCH THOUGHTS (IJCRT)

An International Open Access, Peer-reviewed, Refereed Journal

A Review On Design Of Low Power And High Speed ALU Using Finfet And CMOS

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Abstract: This paper shows a comparison of power requirement and delay consumed between the 4 - bit ALU that is designed using a fin-shaped field-effect transistor [FinFET] and the traditional CMOS to demonstrate a better and efficient 4 – bit ALU in terms of delay and power consumption. The aim of this work is provide a Comparative Analysis of Arithmetic Logic Unit (ALU) Performance using CMOS and FinFET Technologies. ALU is a fundamental component in digital circuits, performing arithmetic and logic operations. The transition from CMOS to FinFET technology has brought significant advancements in terms of power efficiency, speed, and scalability.

Keywords – ALU (Arithmetic Logic Unit), CMOS (Complementary Metal Oxide Semiconductor), FinFET (Fin Field Effect Transistor), technology, comparison, performance evaluation

I. INTRODUCTION

The incessant pursuit of enhanced performance and energy efficiency in digital circuits has led to the exploration of novel transistor technologies beyond the conventional Complementary Metal-Oxide-Semiconductor (CMOS) architecture. One such promising alternative is the Fin Field-Effect Transistor (FinFET) technology, which has garnered significant attention due to its superior electrostatic control and reduced leakage currents. In this context, the design and implementation of critical components like the Arithmetic Logic Unit (ALU) have become pivotal in evaluating the efficacy of these emerging technologies.

In the realm of digital computing, the Arithmetic Logic Unit (ALU) stands as a cornerstone component, orchestrating fundamental arithmetic and logical operations essential for executing computational tasks. Its design and implementation hold paramount importance in shaping the performance and efficiency of digital circuits. With the relentless pursuit of heightened performance and energy efficiency, the exploration of novel transistor technologies beyond the traditional Complementary Metal-Oxide-Semiconductor (CMOS) architecture has garnered significant attention. One such promising alternative is the Fin Field-Effect Transistor (FinFET) technology, celebrated for its superior electrostatic control and reduced leakage currents. Against this backdrop, this paper embarks on a comprehensive comparative analysis of ALU designs realized using both CMOS and FinFET technologies. By scrutinizing key performance metrics such as power consumption and speed utilization, this study aims to illuminate the distinctive attributes and trade-offs associated with each technology, offering insights vital for future endeavors in digital circuit design and semiconductor technology advancement.

This paper aims to provide a comprehensive comparative analysis of ALU designs realized using CMOS and FinFET technologies. By examining key performance metrics such as power consumption and speed utilization, this study endeavors to elucidate the distinctive attributes and trade-offs associated with each technology. Through simulation-based evaluations and empirical investigations, insights into the relative merits and challenges of CMOS and FinFET-based ALU designs will be elucidated, thereby informing future endeavors in digital circuit design and semiconductor technology advancement.

II. LITERATURE SURVEY

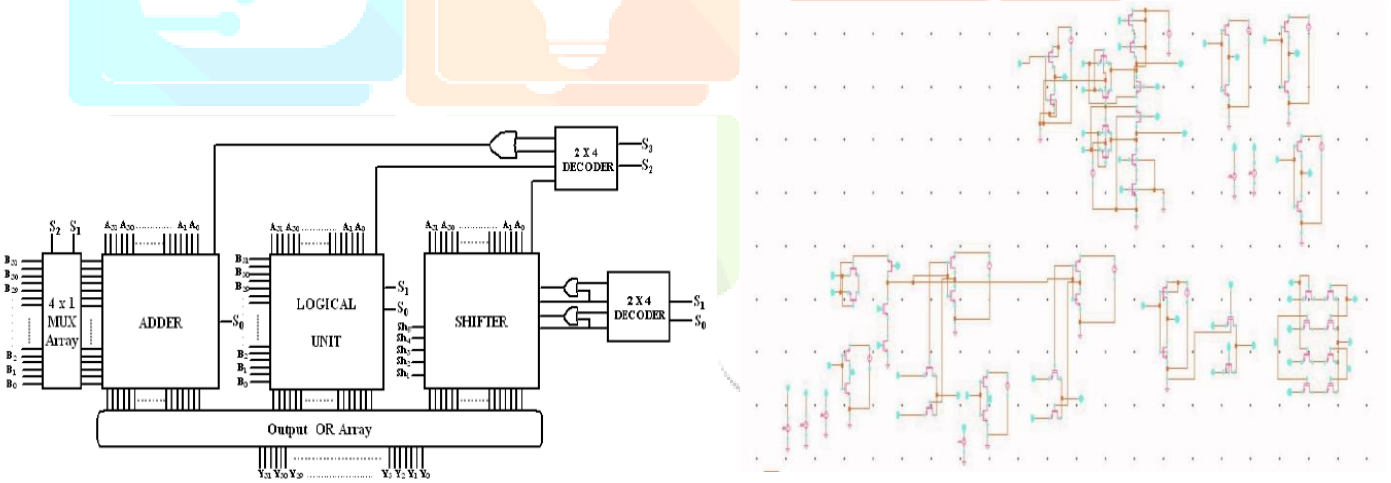
A detailed circuit-level simulations and performance evaluations to validate the effectiveness of the proposed design methodology, showcasing significant reductions in power consumption without compromising on ALU functionality or speed is described by Patanjali Prakash Et.Al [1] in their paper. The work of Shubham Anand Et.Al [2] introduces a novel approach to designing an efficient 8-bit arithmetic logic unit (ALU) with a focus on low power consumption and high operational speed. The proposed ALU architecture utilizes a 17T Full Adder circuit, which significantly reduces power dissipation while maintaining high-speed operation. Through detailed circuit-level simulations and performance evaluations, the authors demonstrate the effectiveness of their approach in achieving remarkable improvements in power efficiency without compromising ALU performance. The authors B Keerthi Priya, Et.Al [3] in their paper " a 16-bit Arithmetic Logic Unit (ALU) designed using FinFET technology in the 7nm process node" focus lies on optimizing the ALU for both high performance mode and low standby power mode. Leveraging FinFET technology offers

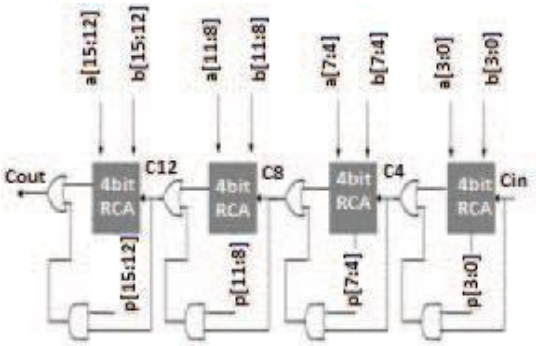
advantages in terms of performance and power efficiency. The ALU design targets 16-bit precision to accommodate various computing tasks effectively. Special attention is given to achieving high performance while minimizing standby power consumption, which is crucial for energy-efficient computing systems. The paper likely presents simulation results and performance analyses to demonstrate the effectiveness of the proposed ALU design in balancing performance and power requirements, showcasing its potential for applications demanding both high performance and low standby power consumption. The pursuit of low-power and area-efficient design methodologies for arithmetic and logic units (ALUs) has been a focal point in contemporary semiconductor research, driven by the demand for energy-efficient computing systems[3].

Leveraging nanoscale FinFET technology, Deshpande Et.Al [4] present a noteworthy contribution with their design of a 4-bit ALU. By exploiting the unique attributes of FinFETs, such as improved gate control and reduced leakage current, they achieve remarkable gains in power efficiency and silicon area utilization. Building upon this foundation, Rahil Kumar Et.Al [5] further explored the potential of FinFETs in ALU design. Their investigation sheds light on the intricacies of utilizing FinFETs to enhance the performance and efficiency of ALUs, providing valuable insights into the practical implementation of FinFET-based digital circuits. Additionally, historical perspectives on high-speed logic design offer valuable insights into the evolution of digital circuitry. John Bond Et.Al [6] discusses the importance of careful design considerations in achieving high-speed logic operation, emphasizing the relevance of efficient circuit architectures and optimization techniques.

Furthermore, Kapoor Et.Al [7] present an improved single-poly bipolar technology tailored for linear and digital applications, highlighting the significance of technological advancements in addressing specific design challenges. By synthesizing insights from these diverse sources, this literature survey provides a holistic understanding of the research landscape surrounding low-power and area-efficient ALU design, encompassing both contemporary innovations and historical perspectives. The in-depth implementation begins with an in-depth exploration of the underlying principles of FSL and its applicability in ALU architectures. By leveraging the inherent advantages of FSL, such as reduced switching activity and enhanced signal integrity, the proposed ALU design achieves notable improvements in both power efficiency and computational speed. Through a comprehensive analysis and rigorous experimentation, the authors demonstrate the efficacy of their approach in mitigating power dissipation while maintaining competitive performance metrics. Furthermore, the paper elucidates the intricacies of the ALU's architectural design, highlighting key optimizations and trade-offs made to achieve the desired balance between power consumption and speed.

III. METHODOLOGY BLOCK DIAGRAM





EXPLANATON OF BLOCK DIAGRAM

The block diagram in fig1 illustrates the systematic arrangement of FSL-based components within the ALU architecture, highlighting their roles in facilitating efficient data processing and manipulation. The effective use of feedback switch logic which is implemented wherein a clock less differential circuit that provides output is complemented from the gate at a single side. By minimizing unnecessary switching activities and optimizing signal propagation paths, the proposed design aims to strike a fine balance between power consumption and computational throughput. The methodology in fig2 begins with a comprehensive analysis of existing ALU architectures and their associated limitations, particularly in terms of power efficiency and speed. Building upon this understanding the integration of a 17T Full Adder circuit into the ALU design is done. Through a series of detailed simulations and performance evaluations, the methodology evaluates the effectiveness of the 17T Full Adder in reducing power dissipation while maintaining high-speed operation. By carefully optimizing the ALU's architecture and circuitry, the methodology aims to strike a balance between power efficiency and computational performance. Parallel adder which is the main block of Arithmetic and Logic unit (ALU) plays crucial role in deciding the speed and power.16-bit ALU is designed using carry skip adder as shown in fig.3. In an Nbit carry skip adder, N bits are divided into groups of k bits. The adder propagates all the carries simultaneously through the groups. Each group I computes group P_i using the following relationship:

$$P_i = p_i\, p_{i+1}\, p_{i+2}\, p_{i+3}\, p_{i+4}\, p_{i+k}$$

Where pi is computed for each bit location i as pi = ai ^bi. Carry Skip Adders take advantage both of the generation or the propagation of the carry signal. The strategy is that, if any group generates a carry, it passes it to the next group; but if the group does not generate its own carry owing to the arrangements of individual bits in the block, then it simply bypasses the carry from the previous block to its next block. This bypassing of a carry is handled by Pi. For a 16-bit adder divided into groups of 4 bits each is implemented in ALU Design as shown in fig.3, the worst case is when the first group generates its carry out and the next two subsequent groups due to the arrangements of bits do not generate their own carries but simply skip the carry from the first group to the last group. The last group makes use of this carry and then generates its own carry. The worst case carry delay of a carry skip adder is less than the corresponding carry delay of an equal width.

IV COMPARISON OF PREVIOUS RESULTS

After understanding and analysis we obtain the following discussion**,**

Table-1: Comparison of the previous results on delay and power

Shifting Operation	Shifter Arch.	Power Consumption (in µW)		Delay (in ps)	
		CMOS	FSL	CMOS	FSL
Logical Left Shift	Array	229.4	245.7	390.7	381.3
	Log	237.3	252	360.7	358.2
Logical Right Shift	Array	268.4	288.5	385.9	383.1
	Log	300.4	314.9	365.6	361.7
Circular Left Shift	Array	415.9	453.3	510.3	507.4
	Log	436.3	478.2	495.6	483.5
Circular Right Shift	Array	483.6	530	515.2	509.5
	Log	512.7	562.9	501.1	497.4

Table-2: Comparison of previous simulation results for 1- bit ALU and 8-bit ALU

Design	**Power**	**Delay**	**PDP**
FA-11T	16	64 ps	1024
HFA-22T	4.08	59.1 ps	241.1
*FA-17T	**1.16**	**9.52** ps	**11.04**
1-bit ALU [2]	4.47	20.33 ns	90.87
*1-bit ALU	**3.82**	**15.58** ns	**59.51**
8-bit ALU [2]	32.9	6.95 ns	228.65
*8-bit ALU	**26.30**	**4.18** ns	**109.93**

Table-3: Comparison of difference in power along with delay

Design	Power in Low Standby Power [LTSP] mode (in um)	Power in High Performance [HP] Mode (in um)	Delay (in ns)
Alu design 1	24	45	25
Alu design 2	3.5	4.7	50
Proposed ALU Design With CD Logic	**1.75**	**3.25**	**15**

V CONCLUSION

In conclusion, a groundbreaking approach to designing a low-power, high-speed arithmetic logic unit (ALU) using Feedback Switch Logic (FSL) is foreseen. The conclusion highlights the practical implications of the research, emphasizing its potential applications in real-world scenarios. The detailed analysis of the ALU's architecture and functionality provides valuable guidance for future research endeavors in the field of VLSI design, paving the way for the development of advanced computing platforms optimized for low power consumption and high performance. It also introduces a methodology for designing an 8-bit arithmetic logic unit (ALU) with a focus on low power consumption and high operational speed. The study showcases the effectiveness of integrating a 17T Full Adder circuit into the ALU architecture, demonstrating significant improvements in power efficiency without compromising computational performance. Through meticulous circuit-level optimizations and architectural considerations, the proposed methodology offers a promising solution for realizing energy-efficient computing systems. The conclusion underscores the practical significance of the research, highlighting its potential impact on various applications requiring low-power computing solutions. By offering valuable insights into the design and optimization of ALUs, the paper sets the stage for the development of next-generation digital systems tailored to meet the demands of energy-conscious environments. The research compares ALU designs, with the FinFET-based ALU by emerging as the most promising. Leveraging FinFET technology, it excels in performance and power efficiency, particularly in the 7nm process node. This design strikes a balance between high performance and low standby power, crucial for modern computing demands.

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