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SRAM Cell Design Using Finfet For Low Power And Delay

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Abstract: This paper introduces an approach utilizing a fin-shaped field-effect transistor to illustrate the structure of a 6T SRAM cell. The primary goal is to enhance the presentation's competitive edge while concurrently reducing the power usage and read/write delay inherent in conventional 6T SRAM cell designs. Given the increasing demand for rapid mobile computing, traditional CMOS SRAM cell configurations face performance constraints and significant power demands. This research undertakes a thorough examination of power consumption and read/write delay parameters associated with low-power SRAM cell designs. Furthermore, an exhaustive comparative analysis is performed between 45nm nano-scaled technologies and the emerging FinFET-based 6T SRAM cells, with a particular emphasis on their respective power efficiency and operational speed characteristics.

I. Introduction

The 6T SRAM unit serves as a foundational component within contemporary memory architectures, celebrated for its equilibrium between compactness and durability. Comprised of six transistors arranged in a cross-coupled latch configuration, this cell design enables robust storage of binary data. The stability of the cell stems from the bistable nature of its latch, which retains its state as long as power is supplied, making it ideal for caching frequently accessed data in processor caches and other memory-intensive applications. Its compact size and moderate power usage make it a preferred choice in integrated circuits, particularly for applications where high-speed access and low standby power are essential considerations. In recent years, progress in semiconductor manufacturing technologies has spurred innovations in 6T SRAM cell designs aimed at further enhancing performance metrics. These advancements include the integration of novel transistor structures such as FinFETs, which offer improved electrostatic control and reduced leakage currents compared to traditional planar CMOS transistors. Additionally, efforts to optimize cell layouts and minimize parasitic capacitances have led to improvements in read and write access times, contributing to overall system performance gains.

As the desire for faster, more energy-efficient computing solutions continues to rise, ongoing research and development efforts in the realm of 6T SRAM cell design remain crucial for advancing the capabilities of modern electronic systems. The pursuit of faster and more efficient memory technology is incessant in the field of contemporary semiconductor design. One of these endeavors is exploring FinFET technology, which holds potential in reducing power consumption and read/write latency in SRAM (Static Random Access Memory) cells. The primary aim of this project is to showcase the benefits of incorporating FinFET technology

into the design of a 6T SRAM cell over the conventional CMOS SRAM cell, particularly in terms of power efficiency and operational speed. This endeavor aims to bolster ongoing endeavors to enhance memory performance while mitigating energy consumption, a critical imperative in modern semiconductor design, by leveraging the unique characteristics of FinFETs. The significance of this undertaking lies in addressing the growing need for memory systems capable of meeting the expanding requirements of a diverse array of applications, ranging from data centers to mobile devices. Advancements in semiconductor technologies present challenges for conventional CMOS-based SRAM cells, including escalating power usage and read/write latency, which impede the overall efficiency of computer systems. There exists an opportunity to overcome these obstacles and usher in a new era of memory architecture with reduced energy footprints and improved performance metrics by transitioning to FinFET-based SRAM cells. To tackle the critical issues facing modern memory architectures, this study endeavors to present empirical evidence supporting the feasibility of FinFET technology. Six transistors constitute the SRAM cell, hence its designation as a 6T-SRAM cell. Two NMOS pass gate transistors (PG) are utilized to access the cell. Pass gate transistors linked to the bit lines facilitate data reading or writing using the word line (BL and BLB). The input/output lines BL and BLB facilitate data reading and writing[1]. When designing the cell using CMOS, two inverters are configured and connected such that the output of the first inverter serves as the input of the second inverter, and vice versa. These inverters are linked to a complementary bit line using two pass transistors. The function of the word line is to read and write data from the memory cell, with its input terminals connected to the access transistors. The bit lines play the role of transferring data in and out of the memory cell to the sense amplifier[2].

II. LITERATURE SURVEY

The author "Rohit Kumar Sah" has cited within their work "Performance Analysis of a 6T SRAM Cell in 180nm CMOS Technology", A traditional 6T SRAM cell consists of two inverters connected in a back-to-back configuration. These inverters latch the data that needs to be stored. The process of storing data is called a Write operation, while retrieving the data is called a Read operation. Writing involves uploading content into the SRAM cell, while reading entails fetching the content. Sensing circuits assist in the read operation by detecting the BL and BLB data lines before fully discharging them[3]. As stated by the authors "Shikha Saun, Hemant Kumar" in their study "Design and Performance analysis of 6T SRAM Cell on different CMOS Technologies with Stability Characterisation", Delay refers to the variation between the time input is applied and the time the response is obtained. The primary aim of designing any system is to minimize delay, thereby enhancing system speed. In SRAM, speed is gauged by read access time and write access time[4]. Abhishek Agal, Pradeep and Bal Krishan as per the authors' assertions in "6T SRAM Cell Design and Analysis", For projects with power constraints such as space exploration and satellites, it's advisable to utilize SRAM cells that consume minimal power. Conversely, devices requiring very fast processing should opt for SRAM cells with minimal time delay. SRAM cells with maximum SNM are suitable for use in noisy environments. Optimizing the design of an SRAM cell involves balancing various performance parameters. While no new designs are being introduced currently, future proposals may focus on SRAM cell designs or schematics aimed at reducing read/write delay and power consumption[5].

Meenakshi Devi, Charu Madhu, Nidhi Garg as analysed for commercial applications, SRAM as cache memory, necessitating faster SRAM for direct CPU interface. SRAM cells find application in various devices such as digital cameras, cell phones, and industrial and scientific equipment[6]. Gurmohan Singh has outlined in his work that during read operations, the minimum voltage reached is termed as read voltage, determined by the division of voltage between the pull-down transistor and access transistor. Read stability is ensured by low access transistor driving strength, which reduces the read voltage. In write operations, the maximum voltage reached is called write voltage, determined by the division of voltage between the access transistor and pull-up transistor. Write stability is confirmed by strong access transistor driving strength, reducing the write voltage[7]. A CMOS SRAM cell comprises six MOSFETs, offering lower power consumption in standby mode and greater immunity to transient noise and voltage variation compared to a 4T resistive load cell. This preference originates from its suitability for highspeed, low-power operation. The storage cell has two stable states denoted by 0 and 1. In addition to the two inverters, a pair of access transistors control accessing a storage cell during read and write operations. Access to the cell is enabled by the word line (WL), which

controls the two access transistors (M5 and M6), determining whether to connect the cell to the bit lines: BL and BLB. Though not strictly necessary, having two bit-lines aids in maintaining cell stability and reducing voltage swing, thus impacting power dissipation. Another advantage is the reduced complexity of the SRAM cell[8].

The author K.Dhanumjaya posit in their research, the aim of this paper is to explore transistor sizing of the 6T SRAM cell for optimal power and delay. Proposed schemes such as bit line balancing and transmission gate scheme aim at enhancing the effectiveness of SRAM cells. Cadence simulation results validate that the proposed scheme achieves approximately 40% power savings compared to other designs[9]. J. Lohstroh, K. Anami, and F. J. List analyzed SRAM cell stability using static noise margin. E. Sevinch, in 1987, determined the margin of static noise of SRAM cells through analytical and simulated results. In 2006, Evelyn Grossar demonstrated the stability of the N curve for assessing read and write stability. In 2008, Zheng derived various methods for calculating read and write stability. Jiajing Wang, Satyanand Nalam, and Benton H. Calhoun analyzed various parameters affecting SRAM performance, such as power consumption, static noise margin, process effects, temperature, and power supply. Benton H. Calhoun illustrated how transistor scaling and modulation of word line voltage impact stability[10].

This work by Mr.S.Mohammed Sulaiman, B.Jaison, M.Anto Bennet, M.Vijay, V.Pandi Selvam, P.Anandakumar explores methods to introduce flexibility into low-power system circuits and architecture. SRAMs are widely utilized as cache memories in microprocessors due to their high-speed operation and low power dissipation. The standard architecture of 6T SRAM cells continues to be pivotal in VLSI systems due to their short access times and compatibility with FinFET technology. The relentless scaling of transistor sizes as per Moore's Law has propelled integrated circuits into a power-limited era[11]. The authors Syed Samsuz Zaman, Pankaj Kumar, Manash Pratim Sarma, Ashok Ray and Gaurav Trivedi articulate in their paper, FIN-shaped field-effect transistor technology has evolved due to the continuous scaling of conventional MOSFETs. Modern IC chips comprise billions of transistors, aiming for technology with higher drive current, low sub-threshold slope, low drain-induced barrier lowering, high packing density, and longer battery lifetime, facilitating high-energy-efficient electronics in low-power, high-performance operations[12]. In the context of authors' Sourindra Chaudhuri, Niraj K. Jha Multi-gate transistors, such as FinFETs, have become mainstream, offering decreased current leakage along with better performance, and diverse implementation styles. Despite early obstacles in cost and manufacturing complexity, these issues have largely been resolved, making FinFET fabrication cost comparable to bulk CMOS. The availability of various FinFET styles enables the implementation of novel circuits and the advancement in new optimization techniques[13]. With the progress in the VLSI domain, the authors Jigyasa panchal, Dr.Vishal Ramola elucidate that FINFET SRAM has emerged as a groundbreaking technology, offering transistor designs as small as 7nm to meet the demand for advanced storage systems. The fundamental rationale behind this groundbreaking technology lies in its three-dimensional gate design, which reduces its reliance on traditional drain and source terminals. The conventional transistor design encounters challenges such as the short channel effect, all of which are effectively eliminated by the current principles of FINFET design. Moreover, conventional MOSFETs suffer from issues stemming from variations in arbitrary dopants, a concern that is mitigated by FINFETs due to the absence of a channel doping mechanism. In FINFET circuits, lower levels of supply voltage are observed compared to planar CMOS circuits, attributed to the reduced number of energy points and the delay and energy product. Consequently, we achieve enhanced voltage stability with FINFET technology14].

III. METHODOLOGY

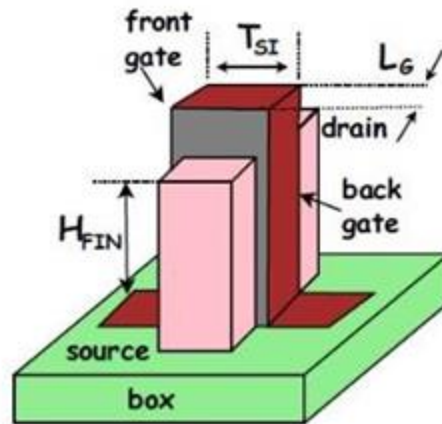

Fig 1: Typical n/p FinFET device

Choice to utilize FinFET technology over the conventional CMOS due to its compelling advantages in power efficiency and delay reduction. FinFET, with its three-dimensional transistor structure, offers a substantial improvement in controlling leakage currents and gate control compared to CMOS. This translates into tangible benefits in power consumption, a critical consideration in contemporary electronic design where energy conservation is paramount. Moreover, FinFET's enhanced electrostatic control enables us to achieve significant power savings without compromising performance.

Beyond power efficiency, FinFET technology also presents advantages in terms of delay reduction, which is crucial for achieving high-speed operation in integrated circuits. The unique design of FinFET transistors contributes to minimizing signal propagation delays, thereby enhancing overall system performance. By harnessing these benefits, we anticipate achieving a more efficient and responsive design for our project. Additionally, the adoption of FinFET technology aligns with current trends in semiconductor manufacturing, reflecting our commitment to leveraging cutting-edge advancements in our research and development endeavours. Through meticulous consideration of technological choices, we aim to ensure the optimal performance and effectiveness of our project outcomes.

The classic 6T SRAM cell utilizes two interconnected inverters in conjunction with two access transistors, as illustrated in figure 2. Acting as the repository, these inverters maintain the authenticity of the data bit within the cell for as long as there is a power supply (VDD) available.

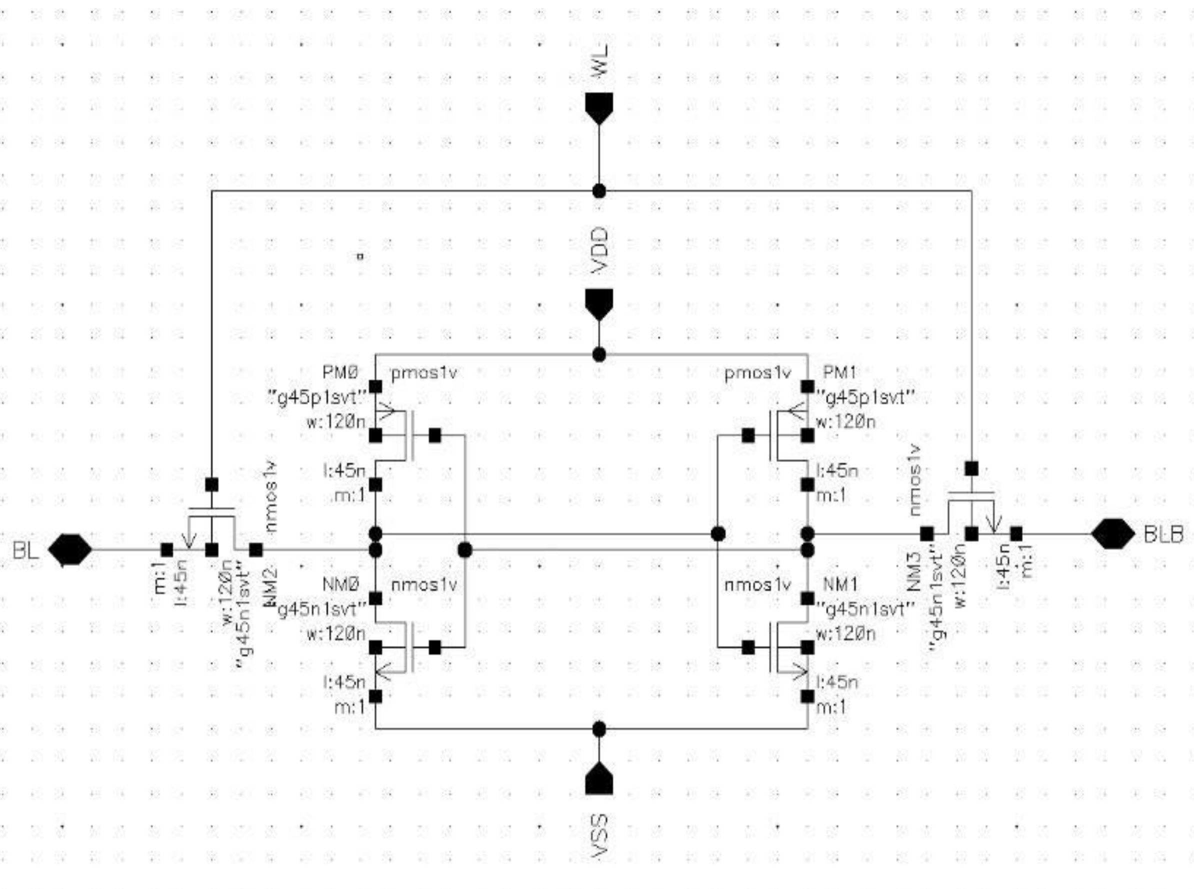

FIG 2: Schematic of SRAM using FinFET

- **Hold/Standby Mode**

When the Word Line (WL) is set to logic ‘0’, the access transistors disengage the cell from the Bit Lines, BL and BL0. Meanwhile, the two cross-coupled inverters within the cell diligently uphold the integrity of the data bit displayed within, provided that a power supply (VDD) is maintained.

- **Write Operation**

During a write operation, the Word Line (WL) is configured to logic ‘1’, facilitating the activation of the access transistors and establishing a connection between the cell and the external circuitry (BL and BL0). Subsequently, data from BL (BL & BL0) is transmitted into the cell via the access transistors. Following a successful write operation, the Word Line (WL) is returned to logic ‘0’. For instance, to write a logic ‘0’ into the cell, BL is set to logic ‘0’ while BL0 is set to logic ‘1’. The WL is then set to logic ‘1’, thereby allowing the access transistors to transfer the logic states via BL and BL0 into the cell. Once the data bit has been successfully written into the cell, the Word Line (WL) is reverted to logic ‘0’, effectively disconnecting the cell from the external circuitry (BL and BL0). The write waveform is illustrated in figure 3.

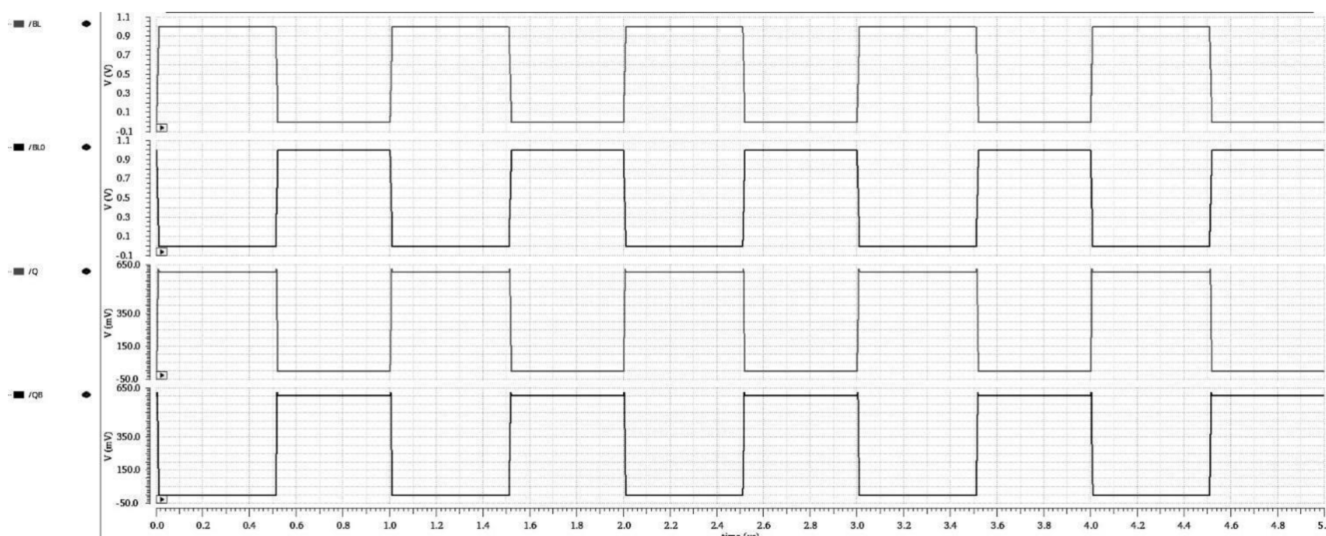

FIG 3: Write Operation

- **Read Operation**

To retrieve the data bit stored within the cell, BL (BL & BL0) is initially pre-charged to VDD, indicating logic ‘1’. Subsequently, the Word Line (WL) is activated by setting it to logic ‘1’. Depending on the data bit stored within the cell, one of the Bit Lines (BL and BL0) undergoes a slight and gradual discharge through an access transistor and pull-down transistor, thereby generating a discernible differential voltage drop across BL and BL0. This minute differential voltage drop is then discerned by a Sense Amplifier, that determines the data bit stored within the cell. The Sense Amplifier is responsible for managing the charging and discharging of significant capacitive loads. For swift read operations, the sensitivity of the Sense Amplifier is crucially maximized. Hence, the magnitude of the differential voltage must be carefully regulated to prevent any inadvertent flipping of the state of the interconnected inverters. The read waveform of the 6T SRAM Cell is detailed in figure 4

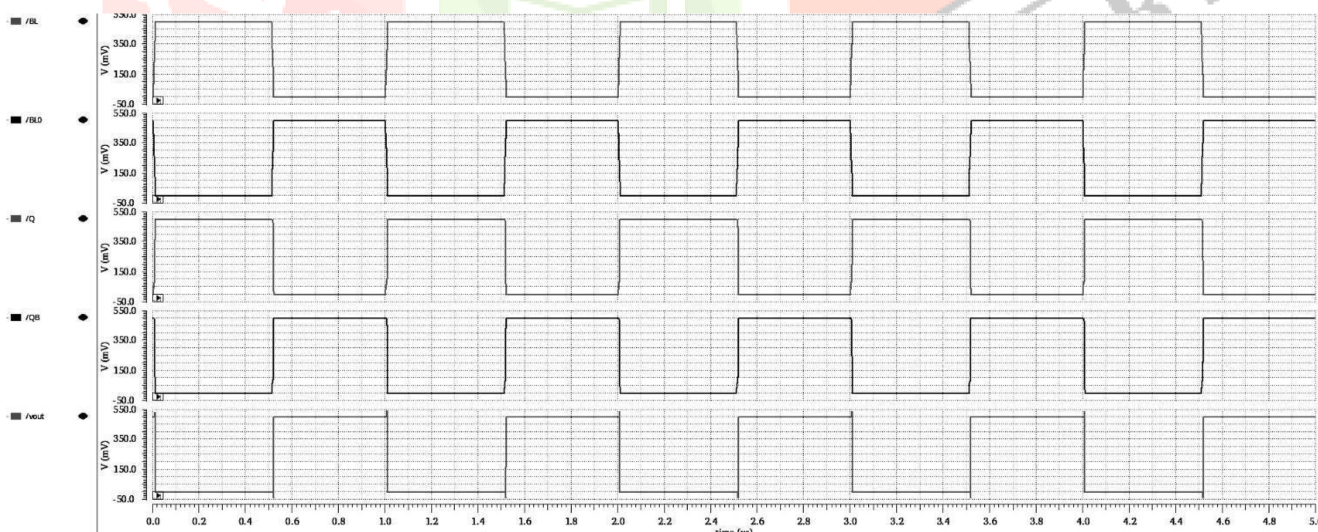

FIG 4: Read Operation

IV. RESULT AND DISCUSSION

Simulation of the 6T SRAM Cell was conducted using Cadence tools, employing 45nm technology and a nominal supply voltage of Vdd = 1V for CMOS and 18nm technology and supply voltage of vdd = 0.5V for FinFET

The summary of comparison results between the 6T SRAM Cell utilizing CMOS technology and the 6T SRAM Cell employing FINFET technology is presented in Table 1 below.

Table 1: Comparison of CMOS Inverter and SRAM with FinFET Inverter and SRAM

PERFORMANCE PARAMETER	CMOS INVERTER	FINFET INVERTER
POWER	537.93nW	12.512nW
DELAY	60.72ms	12.844ms
	CMOS SRAM	FINFET SRAM
POWER	7.38uW	2.71uW
DELAY	WRITE: 4.429ms READ: 4.427ms	WRITE: 0.508ms READ: 0.878ms

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