IJCRT.ORG ISSN : 2320-2882

INTERNATIONAL JOURNAL OF CREATIVE RESEARCH THOUGHTS (IJCRT)

An International Open Access, Peer-reviewed, Refereed Journal

DESIGN AND OPTIMIZATION OF SERDES IN CMOS 45NM TECHNOLOGY

[1]Ravi Kumar M, [2]Sanjai S, [3]Shilpashree S, [4]Shreyas N Kulal, [5]Tinu M

[1]Assistant Professor,[2,3,4,5] Student,

[1,2,3,4] Department of Electronics and Communication Engineering,

[1,2,3,4] Cambridge Institute of Technology, Bangalore, India.

Abstract: With the miniaturization of electronic devices, interconnects (the pathways for data flow) are not shrinking as fast as the devices themselves. This inefficiency leads to problems with power consumption, area usage, and signal interference (crosstalk). To address this issue, the paper explores the use of serial links, which transmit data one bit at a time, as a replacement for traditional parallel buses that send multiple bits simultaneously. Serial links offer several advantages, including fewer connection points (pins), lower power use, smaller physical connectors, and better resistance to noise. The proposed architecture is simulated using a standard CMOS technology and industry-recognized simulation tools. The simulations are set up to evaluate factors like power consumption and data processing speed (throughput) under realistic operating conditions. The paper then compares the performance of this new design with previously reported architectures, highlighting improvements in power savings, area usage, and overall functionality. By analyzing the simulation results and comparisons, the paper demonstrates the significant benefits of the proposed architecture in terms of reduced power consumption, efficient chip area utilization, and improved data processing. Finally, the paper concludes by summarizing the key findings and advancements achieved with this design.

Keywords **– SerDes, CDR, Serializer, De-serializer, TSPC Flip Flop.**

I. INTRODUCTION

The need for high-speed data communication networks has increased due to the growing usage of the internet for the transmission of audio and video. Input/output, or I/O, has always been crucial to contemporary high-speed applications. Traditional parallel communication is unsuitable as integrated circuits (ICs) get smaller and quicker because of issues with signal integrity, data skew, and electronic packaging. The receiver must sample the data by simultaneously recovering the clock from the transmitter, which transmits the data without a corresponding clock. Various sounds, both internal and external to the transmitter and receiver, can contaminate data in high-speed systems. Jitter and skews result at the receiver as a result. Therefore, a CDR circuit is required in order to both recover the data that was received from the distorted signal and to extract the clock information that went along with it. The receiver does this by phase matching the reference clock with the incoming data transitions. Phase lock loops are used to implement the CDR in this case. In essence, a PLL is a negative feedback loop that locks the input data's clock phase and frequency to the reference signal. [1]. Serial I/O has the supremacy of faster speed, less interference between adjacent links, fewer pin counts and thus lower packaging costs. A Serializer/De-serializer (SerDes) is such a device that takes the parallel data link input and compress it into fewer lines of serial stream which would then be deserialized and output original parallel data is recovered. SerDes is very beneficial because it solves the problems of many traditional parallel data links and reduces the number of I/O pins and cost for connectors and cables. Designing a robust, lower power SerDes that

functions properly at high speed is very challenging and requires knowledge of various domains.[2]

II. EXISTING ARCHITECTURE

Inspired solutions for dependable low power on-chip SerDes links have already been put proposed in recent papers. These solutions include resistive terminated single ended transmission lines or a novel self-timed signalling mechanism along differential transmission lines. The design employs two level Manchester encoding with resistive termination and power-efficient circuitry, while the design gives a variation-tolerant driving technique for all digital self-timed three levels signalling.

For a supply voltage of 1.8V, Cadence Spectre simulator is used for simulation, while UMC 180 nm CMOS technology is used to build the Serializer and Deserializer architecture. The architecture uses clock frequencies of 625 MHz, 312.5 MHz, and 156.25

MHz to serialize 8-bit parallel data at 156.25 MHz into a 1.25 Gbps serial data stream. With a clock frequency of 625 MHz, the architecture deserializes a 1.25 Gbps serial data stream to 8-bit parallel data at 156.25 MHz [3].

III. PROPOSED ARCHITECUTURE

This Design uses Serializer built from TSPC (True Single-Phase Clock) D-Flip Flop and a Multiplexer. The Reference design uses Double edge triggered DFF which uses both clock and clock bar signal which causes signal overlap and causes race around condition. At various frequencies the circuit would result in unstable signal due to overlapping clocks. The suggested design uses UMC 45nm CMOS technology. With input pulses at a voltage of 1.2V, the serializer ensures compatibility with incoming data signals, enabling reliable data transmission while maintaining signal integrity. The 8-data line serializer serves in converting parallel data from eight input lines into a serial data stream. Its operation relies on precise clock timing, with support for clock frequencies of 1GHz, 500MHz, and 250MHz, offering users flexibility in data transmission speeds to suit various application requirements as shown in Figure 1.

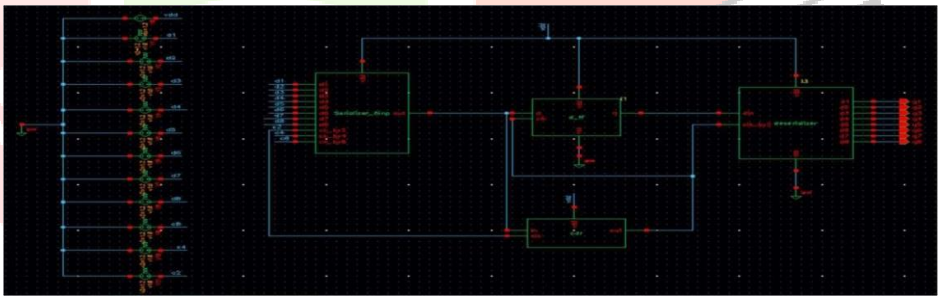

Figure 1. SerDes Design

IV.IMPLEMENTATION

Three primary blocks comprise a Serializer/De-serializer (SerDes) system: Serializer, De-serializer, and Clock and Data Recovery (CDR). The Clock and Data Recovery (CDR) block recovers the clock signal to ensure correct sampling of the serial data stream. The Serializer block turns parallel data inputs into a serial data stream. The De-serializer block converts the incoming serial data stream back into parallel data. These three blocks work together to create the fundamental parts of a SerDes system, allowing for dependable and fast serial interface communication.

4.1 SERIALIZER

Three flip-flops (FF1, FF2, and FF3), a 2-to-1 multiplexer (MUX), and an inverter makes up the serializer circuit. While D2 is connected to the data input (D) of FF2, input signal D1 is directly connected to the data input (D) of FF1. Two routes are created from the clock signal: one goes straight to the clock inputs (CLK) of FF1 and FF3, while the other goes via an inverter to create the inverted clock signal (CLK'), which is then linked to FF2's clock input (CLK). This configuration guarantees that FF2 is activated on the falling edge of the clock, and FF1 and FF3 are triggered on the rising edge. When the clock signal is rising during operation, FF1 samples the input D1 and holds its state until the subsequent clock cycle. Accompanied by the inverted clock signal, FF2 samples input D2 concurrently on the clock signal's falling edge. In order to synchronize the output of FF2 with the clock, FF3 records it on the rising edge of the clock. The clock signal acts as the control input (SEL) and the outputs of FF1 and FF3 are coupled to the two data inputs of the multiplexer. A clock cycle begins when the clock signal is high, and the multiplexer chooses the output of FF1, which is the sampled value of D1. On the other hand, the multiplexer chooses the output of FF3, which represents the sampled value of D2, when the clock signal is low, signifying the middle of a clock cycle. With this configuration, the clock signal is used to serialize the inputs D1 and D2, and the serialized output is accessible at the multiplexer's output. The serializer design is shown in Figure 1.

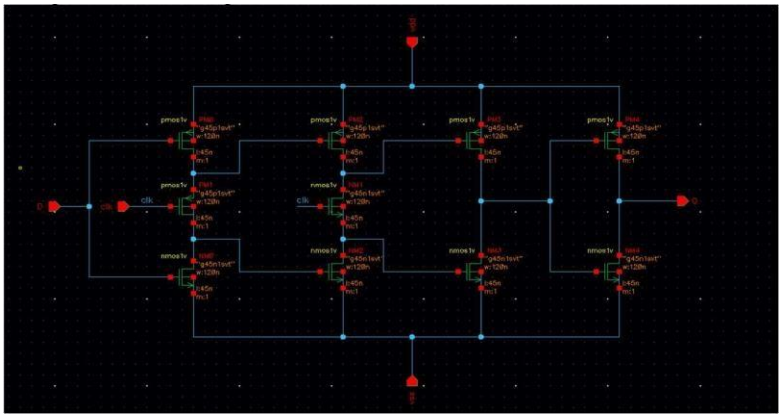

Figure 2. TSPC Flip Flop

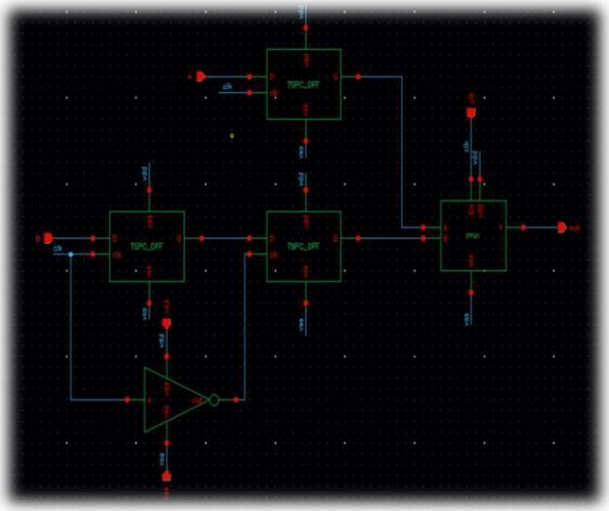

Figure 3. 2:1 Serializer

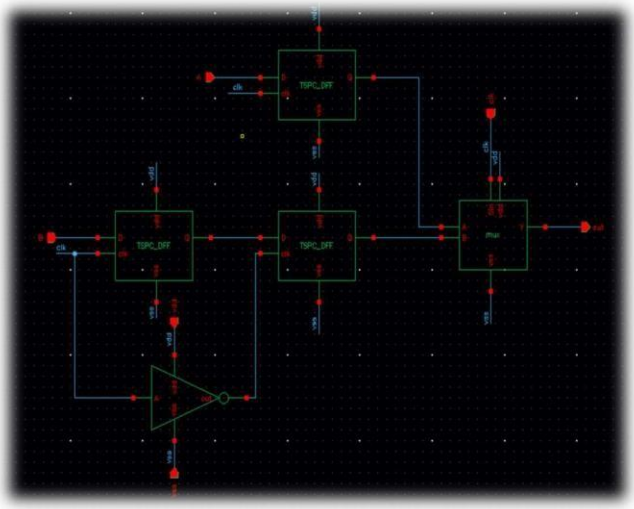

Figure 4. 8:1 Serializer

The flip-flop samples input d1 when the clock signal changes from low to high (positive edge). The flip-flop sets its output to high if d1 is high during the clock's positive edge. The flip-flop sets its output to low if d1 is low at the moment of the clock's positive edge. Till the following positive edge of the clock, the flip-flop keeps its output state intact.The positive edge flip-flop and the negative edge flip-flop take input d2 first. The flip-flop samples input d2 when the clock signal changes from high to low (negative edge).The flip-flop sets its output to high if, at that point of the clock's negative edge, d2 is high. The flip-flop sets its output to low if, at that point of the clock's negative edge, d2 is low. The flip-flop remains in its output state until the subsequent clock negative edge.The delayed output of d1 and d2, known as s1 and s2, is the output of the positive and negative edge ff's and it is sent as an input to the mux. Two flip-flops' outputs are fed into a 2-to-1 multiplexer. The multiplexer uses the clock signal as its control input. This indicates that depending on the clock signal's state, the multiplexer chooses one of the two inputs (the flip-flops' outputs).The multiplexer chooses the positive edge-triggered flip-flop's (attached to s1) output when the clock signal is high. The multiplexer chooses the negative edge-triggered flip-flop's (attached to s2) output when the clock signal is low. These parts work together to effectively serialize the input data (d1 and d2) according to the clock signal in the serializer circuit. The circuit alternately samples and outputs the data from D1 and D2 when the clock signal toggles, transforming the parallel data inputs into a serial data stream at the multiplexer's output.

4.2 DESERIALIZER

Positive edge-triggered flip-flops capture the input data on the ascending edge of the clock signal. When the clock signal change from low to high (positive edge), the data at the input is sampled and stored in each flip-flop in the series. These flip-flops are connected in series, so that one flip-flop's output becomes next flip-

flop's input. Negative edge-triggered flipflops capture the input data on the descending edge of the clock signal. When the clock signal changes from high to low (negativeedge), the data at the input is sampled and stored in each flip-flop in the series. Similar to positive edge-triggered flip-flops, theseflip-flops are also connected in series.

The serial input data stream contains the information that needs to be deserialized, i.e., converted back into parallel data. Each flipflop in the series has its output connected to a separate output line. The outputs of these flip-flops represent the parallel data obtained from the serialized input stream. Depending on the number of flip-flops used, there will be multiple output lines, each corresponding to a bit of the parallel data. All flip-flops, both positive edge-triggered and negative edge-triggered, share the same clock signal. This clock signal controls the timing of when the flip-flops sample the input data.

In the oscillating clock signal, each flip-flop captures the input data at the appropriate edge (either rising or falling) and stores it. The data stored in the flip-flops propagates through the series of flip-flops, effectively shifting the serialized data stream. At eachclock cycle, the next bit of the serialized input data is captured and stored in the flip-flops. By examining the outputs of the flipflops, the original parallel data can be reconstructed.

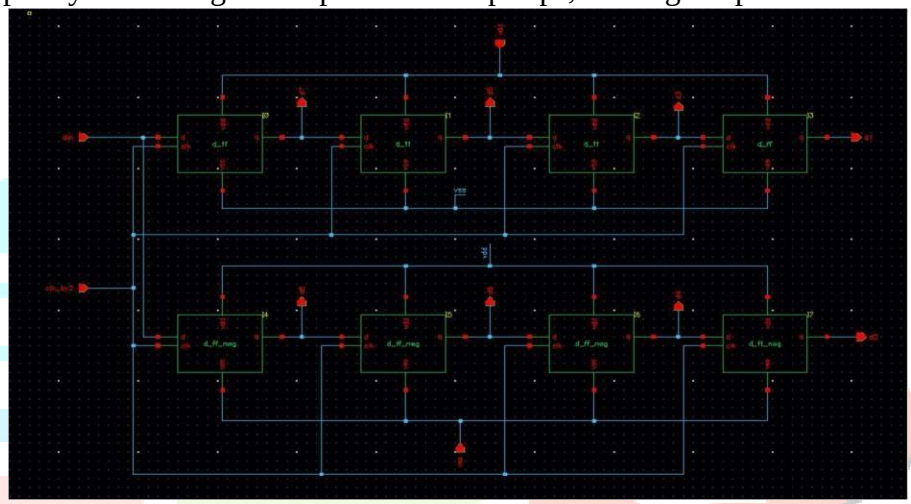

Figure 5. De-serializer

V. RESULTS AND DISCUSSION

Figure 6. Shows the output waveform of SerDes in 45nm.

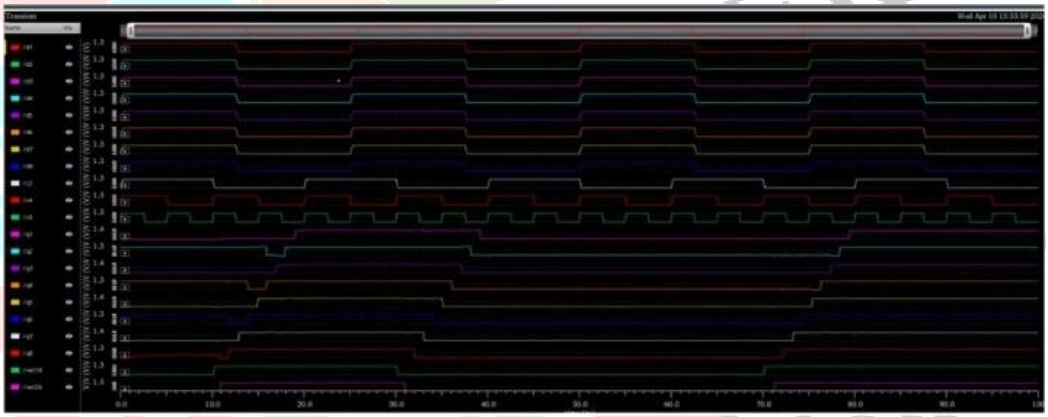

Figure 6. Output Waveform

Results of the simulation

Design	Operating Voltage (V)	Serializer Power (W)	Deserializer Power (W)
Ref 3	1.8	2.19m	3.34m
Ref 20-23	1.8	8.21m	3.02m
Design 1(TSPC)	1.2	455u	105u
Design 2(DETFF)	1.2	99u	105u

The proposed design operates at a voltage of 1.2V and the power is significantly reduced in comparative with the current design. Since 45nm CMOS library is used, the power efficiency, performance and signal integrity of the SerDes is enhanced.

VI. CONCLUSION

In this project, we have designed two SerDes designs along with CDR block in 45nm technology through Cadence Virtuoso software. The delay and power dissipation have been used in this architecture. The power is greatly reduced with area trade-off. The designs operate at 1.2V and consume a power of 276-455uW.The delay on the signals depends on the sizing of the transistors. The frequency deviation can be greatly varied by choosing appropriate transistor sizing.

REFERENCES

[1] Vanditha, S., et al. "Design and Implementation of Clock and Data Recovery Circuits for High Speed Serial Data Communication Links."

[2] YANG, JERRY. *HIGH SPEED CMOS SERDES DESIGN AND SIMULATION USING CADENCE VIRTUOSO AND HSPICE*. Diss. University of Illinois at Urbana-Champaign, 2013.

[3] Jaiswal, Nivedita, and Radheshyam Gamad. "Design of a new serializer and deserializer architecture for on-chip SerDes transceivers." *Circuits and Systems* 6.3 (2015): 81-92.

[4] Matey, Chaitali V., Shraddha K. Mendhe, and Sandip A. Zade. "A Novel Design of Counter Using TSPC D FLIP-FLOP for High performance and low power VLSI design applications using 45NM CMOS technology." *International Journal of Science Technology & Management* 4.1 (2015): 63-66.

[5] Waghela, Sagar. *Phase locked loop (PLL)-based clock and data recovery circuit (CDR) using calibrated delay flip flop (DFF)*. San José State University, 2014.

[6] Singhal, Neha, and R. K. Sharma. "Design of Clock and Data recovery circuit using current starved VCO working with less jitter." *2018 3rd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT)*. IEEE, 2018.

[7] Chen, Fan-Ta, Jen-Ming Wu, and Mau-Chung Frank Chang. "40-Gb/s 0.7-V 2: 1 MUX and 1: 2 DEMUX with transformer-coupled technique for SerDes interface." *IEEE Transactions on Circuits and Systems I: Regular Papers* 62.4 (2015): 1042-1051.

[8] Design of PLL Using CSVCO in 45N m Technology Dr. D. R. V. A. Sharath Kumar1 , Mr. J. Nageswara Reddy2 , Mr. A. Dileep3 1 Professor, Department of ECE, St. Martins Engineering College, Hyderabad, Telangana, India

[9] Mehrabi, Taha, and Kaamran Raahemifar. "Design of a time mode SerDes using differential pulse position modulation (DPPM)." *2017 IEEE 30th Canadian Conference on Electrical and Computer Engineering (CCECE)*. IEEE, 2017.

[10] Song, Shengyu, et al. "A low-noise and fast transient response LDO design for high-speed SerDes." *Journal of Physics: Conference Series*. Vol. 2187. No. 1. IOP Publishing, 2022.

[11] Jeong, Yong-Un, et al. "A low-power and low-noise 20: 1 serializer with two calibration loops in 55-nm CMOS." *2019 IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*. IEEE, 2019.

[12] Mishra, Ashutosh, Pulak Mondal, and Swapna Banerjee. "VLSI-assisted nonrigid registration using modified demons algorithm." *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* 23.12 (2015): 2913-2921.

[13]

[14] Alser, Mohammed H., and Maher M. Assaad. "Design and modeling of low-power clockless serial link for data communication systems." *2011 National Postgraduate Conference*. IEEE, 2011.

[15] Geurts, Tomas, et al. "A 2.5 Gbps-3.125 Gbps multi-core serial-link transceiver in 0.13/spl mu/m CMOS." *Proceedings of the 30th European Solid-State Circuits Conference*. IEEE, 2004.

[16] Park, JunYoung, et al. "A 9-Gbit/s serial transceiver for on-chip global signaling over lossy transmission lines." *IEEE Transactions on Circuits and Systems I: Regular Papers* 56.8 (2009): 1807-1817.

[17] Philpott, Rick A., et al. "A 20Gb/s SerDes transmitter with adjustable source impedance and 4-tap feed-forward equalization in 65nm bulk CMOS." *2008 IEEE Custom Integrated Circuits Conference*. IEEE, 2008.

[18] Chen, Dianyong. "SerDes Transceivers for High-speed Serial Communications." *Department of Electronics, Carleton University, Ottawa* (2007).

[19] Bhatti, Rashed Zafar, Monty Denneau, and Jeff Draper. "2 Gbps SerDes design based on IBM Cu-11 (130nm) standard cell technology." *Proceedings of the 16th ACM Great Lakes symposium on VLSI*. 2006.

[20] Ghoneima, Maged, et al. "Serial-link bus: A low-power on-chip bus architecture." *IEEE Transactions on Circuits and Systems I: Regular Papers* 56.9 (2008): 2020-2032.

[21] Safwat, Sally, et al. "A 12Gbps all digital low power SerDes transceiver for on-chip networking." *2011 IEEE International Symposium of Circuits and Systems (ISCAS)*. IEEE, 2011.

[22] Hussein, Ezz El-Din, et al. "A 16gbps low power self-timed serdes transceiver for multi-core communication." *2012 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2012.

[23] Tadros, Ramy N., et al. "A variation tolerant driving technique for all-digital self-timed 3-level signaling high-speed SerDes transceivers for on-chip networks." 2014 IEEE International Symposium on Circuits and Systems (ISCAS). IEEE, 2014.

[24] Elsayed, Abdelrahman H., et al. "Low-power all-digital manchester-encoding-based high-speed serdes transceiver for on-chip networks." *2014 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2014.