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A LOW POWER IMPLEMENTATION OF FSM BASED VENDING MACHINE USING VERILOG.

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Abstract:
Our project is design of a controller for a vending machine, which sells candy bars for five rupees. The implementation of this project was done by using a finite state machine (FSM) model. In a normal vending machine we insert some coin of a specific amount and we get the item from the vending machine. But in this project it is not the same. The vending machine designed here is for a five rupees candy, so as per a normal vending if you insert five rupees in the machine you will receive a candy from the machine, but suppose you insert more than five (in a combination of one rupee or two rupees or five rupees) then if it would be a normal vending machine then it would not work, but in this project we designed a vending machine which give you the candy and the remaining money.

Key Words:

FSM ,VLSI , HDL ,RTL,ASIC

INTRODUCTION:

But in this project, it is not the same. The vending machine designed here is for a five rupees candy, so as per a normal vending if you insert five rupees in the machine you will receive a candy from the machine, but suppose you insert more than five (in a combination of one rupee or two rupees or five rupees) then if it would be a normal vending machine then it would not work, but in this project we designed a vending machine which give you the candy and the remaining money. Now as you have got the basic idea about the project we will see how to design such a vending machine controller. A Finite State Machine (FSM) is a well-established design methodology for modeling sequential operations in digital systems. FSMs allow designers to represent system behavior in terms of states and transitions, making them particularly suitable for vending machines where operations such as idle waiting, coin insertion, product selection, and dispensing must be carefully coordinated. The FSM approach ensures accuracy, predictability, and ease of implementation. However, conventional FSM-based designs often suffer from excessive power consumption due to redundant switching activity, clock distribution overhead, and inefficient logic utilization. This becomes a major concern in systems like vending machines that spend a significant portion of time in idle states, waiting for user input.

Finally, the organization of this report reflects the logical progression of the project. Following this introduction, the literature review will examine existing vending machine designs, highlight their strengths and limitations while identifying opportunities for improvement. The methodology section will detail the

FSM modeling process, state diagrams, and VLSI implementation strategies. Results and analysis will present simulation outcomes, power consumption metrics, and performance evaluations, providing evidence of the design's efficiency. The conclusion will summarize the findings and suggest directions for future work, such as integrating cashless payment systems or IoT-based monitoring into the FSM-VLSI framework.

EXISTING SYSTEM:

The existing system of vending machines is generally based on conventional digital logic or microcontroller-driven designs that focus primarily on functionality rather than power efficiency. In such systems, the vending operation—accepting coins, validating input, selecting products, and dispensing items—is implemented using either basic combinational logic circuits or embedded controllers programmed without specific attention to power optimization. These machines often remain fully active regardless of user interaction, leading to continuous power consumption even during idle conditions. As a result, they are not ideal for energy-constrained environments.

In many traditional FSM-based vending machine implementations, although a Finite State Machine (FSM) is used to control the sequence of operations, the design does not incorporate advanced low-power techniques. The states are often not optimized, and unnecessary transitions or redundant logic can increase switching activity, which directly contributes to higher dynamic power consumption. Additionally, the absence of techniques like clock gating, power gating, or efficient state encoding leads to inefficient utilization of hardware resources. These systems may perform correctly but are not designed with scalability or energy efficiency in mind.

Overall, the existing systems provide a functional but power-inefficient solution for automated vending operations. While they successfully handle user inputs and product delivery, they lack optimization strategies that are crucial in modern digital design. This limitation highlights the need for improved designs—such as low-power FSM-based implementations using Verilog—that can reduce energy consumption, enhance performance, and make the system more suitable for portable and large-scale deployment.

PROPOSED SYSTEM:

The proposed system introduces a low-power vending machine design based on a Finite State Machine (FSM) implemented using Verilog, with a strong emphasis on energy efficiency and optimized hardware utilization. Unlike traditional designs, this system carefully organizes the vending process into well-defined states such as idle, coin insertion, amount verification, product selection, dispensing, and change return. Each state is designed to activate only the required components, ensuring that unnecessary circuitry remains inactive during operation. This structured FSM approach improves reliability while also reducing redundant operations within the system.

A major enhancement in the proposed system is the incorporation of low-power design techniques. Methods such as clock gating are used to disable the clock signal to inactive modules, thereby reducing switching activity and dynamic power consumption. Efficient state encoding techniques, such as Gray coding or one-hot encoding (depending on optimization goals), are applied to minimize transitions between states. Additionally, the design reduces combinational path complexity and avoids redundant logic, which helps lower both power consumption and area usage. These optimizations make the system suitable for deployment in environments where power efficiency is critical, such as portable or battery-operated machines.

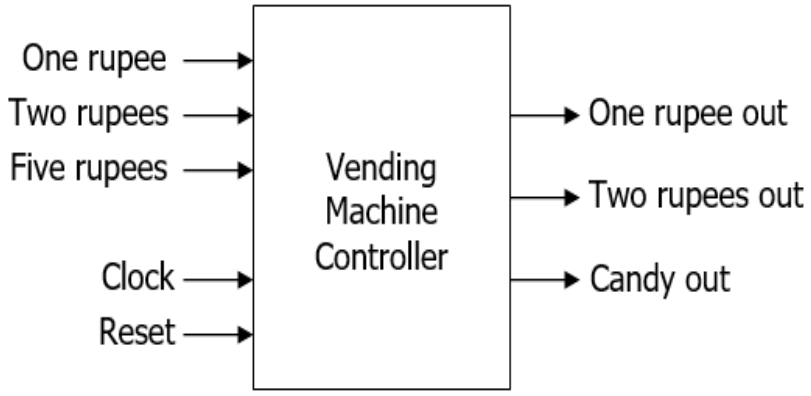
Overall, the proposed system provides a highly efficient, scalable, and reliable solution for automated vending operations. By leveraging Verilog for hardware description, the design can be easily synthesized, tested, and implemented on FPGA or ASIC platforms. The combination of FSM-based control with power optimization strategies ensures improved performance compared to existing systems. This approach not only reduces energy consumption but also enhances the system's longevity and adaptability, making it a modern solution aligned with current trends in low-power digital system design.

METHODOLOGY:

The methodology of this project begins with a clear specification of the vending machine requirements, including the types of inputs (coins, selection buttons), expected outputs (product dispensing, change return), and operating conditions. Based on these requirements, the system is modeled using a Finite State Machine (FSM), where each state represents a specific stage of operation such as idle, coin collection, verification, selection, and dispensing. A state transition diagram is first developed to visualize the behavior of the system, followed by a state table that defines inputs, outputs, and transitions.

This structured approach ensures that the design is logically organized and easy to implement in hardware.In the next phase, the FSM model is implemented using Verilog HDL, where each state and transition is coded using sequential and combinational logic blocks. The design is modularized to separate key components such as input handling, state control, and output generation. To achieve low power consumption, techniques such as clock gating are applied to disable inactive modules, and efficient state encoding methods (like one-hot or Gray encoding) are selected to minimize switching activity. Simulation is then performed using tools like ModelSim or similar HDL simulators to verify functional correctness under various test cases, ensuring the system behaves as expected.

Finally, the verified design is synthesized and implemented on hardware platforms such as FPGA. During synthesis, optimization settings are applied to reduce logic utilization and power consumption. Post-synthesis analysis is carried out to evaluate parameters like power usage, timing performance, and resource utilization. If necessary, iterative refinements are made to further optimize the design. This systematic methodology—from specification and modeling to implementation and testing—ensures the development of a reliable, efficient, and low-power FSM-based vending machine system.



Vending Machine Controller Block Diagram

APPLICATIONS:

- Retail & Shopping Malls: Used in snack, beverage, or ticket vending machines where energy efficiency reduces operational costs.
- Public Transport Systems: Ticket vending machines at bus stations, metro stations, and railway platforms benefit from low-power designs, especially in areas with high usage.
- Educational Institutions: Automated vending machines for books, stationery, or refreshments inside campuses, where low power consumption helps reduce electricity bills.
- Hospitals & Offices: Compact vending machines for medicines, masks, or refreshments that can run continuously with minimal energy usage.
- Smart Cities & IoT Integration: FSM-based vending machines can be integrated into smart kiosks, powered by solar or battery systems, making them suitable for outdoor environments.
- Rural & Remote Areas: Low-power designs are crucial for vending machines deployed in areas with limited electricity supply, often running on renewable energy sources

HARDWARE DETAILS:

1. FPGA / ASIC Board (Main Hardware Platform):

The FPGA or ASIC serves as the main hardware platform where the entire vending machine design is implemented using Verilog HDL. It contains programmable logic blocks, flip-flops, and routing resources that allow the FSM to be realized in hardware. The FSM controller, input processing, and

output generation are all synthesized and executed on this board. FPGA is commonly preferred because it supports easy reprogramming, debugging, and low-cost prototyping.

2. Clock Circuit:

The clock circuit provides a continuous timing signal that synchronizes all operations of the FSM. Every state transition in the vending machine occurs based on clock pulses. It ensures that inputs are sampled and outputs are updated in a controlled and sequential manner. In low-power design, the clock may be gated so that unused modules do not receive unnecessary clock signals, reducing power consumption.

3. Reset Circuit:

The reset circuit is used to initialize the vending machine into a known starting state, usually the idle state. When the reset signal is activated, all registers and state memory are cleared, ensuring that the system starts fresh without errors. This is important for stable operation, especially after power-on or system faults.

4. Input Unit (Push Buttons / Switches):

The input unit consists of push buttons or switches used to simulate coin insertion and product selection. Each button represents a specific coin value or product choice. These inputs are fed into the FSM controller, which processes them to update the current balance and determine the next operation. Debouncing may be used to avoid false triggering due to mechanical noise.

5. FSM Controller (Core Processing Unit):

The FSM controller is the heart of the system and is implemented using Verilog. It consists of state registers (flip-flops) and combinational logic. It manages all vending operations such as idle state, coin detection, credit accumulation, product selection, validation, dispensing, and change return. The controller ensures that operations follow a defined sequence based on inputs .

SOFTWARE DETAILS:

The software design of the project "A Low Power Implementation of FSM Based Vending Machine Using Verilog" involves the development, simulation, verification, and synthesis of the hardware logic using specialized digital design tools. The entire system is written in Verilog HDL (Hardware Description Language), which allows the behavior and structure of the FSM-based vending machine to be described in code form. The software implementation ensures that each hardware component, such as the FSM controller, inputs, outputs, and registers, is properly defined and functionally verified before hardware deployment.

The main software used in this project includes HDL design and simulation tools such as Xilinx Vivado, ModelSim, or Quartus Prime, depending on the target FPGA platform. These tools are used to write Verilog code, compile it, and simulate the functionality of the vending machine under different test conditions. Testbenches are created to apply various input scenarios such as coin insertion sequences and product selection cases. The simulation results help verify whether the FSM transitions correctly between states and whether outputs like product dispensing and balance updates work as expected.

After successful simulation, the design undergoes synthesis and implementation, where the Verilog code is converted into a hardware netlist that can be programmed into an FPGA. The software tools also perform optimization to reduce logic usage and support low-power techniques such as clock gating and efficient state encoding. Finally, timing analysis and functional verification are carried out to ensure the system meets performance and power requirements. Overall, the software design plays a crucial role in transforming the Verilog-based FSM model into a real, working low-power vending machine system.

CONCLUSION:

The vending machines that are popularly used till date are operated by receiving specific denomination i.e. the cost of the product and deliver it. They doesn't work when a combination of coins are inserted or more or less amount is given. But this vending machine is a solution for the above problems. It will deliver the product even if we insert more than the cost of the product and gives the remaining change. It also delivers the product if we insert the amount in combination of coins. Some further developments are to be made to accept the currency notes also.

The design and implementation of a low-power vending machine using a Finite State Machine (FSM) in Verilog successfully demonstrate the efficiency of hardware-based control systems. By structuring the vending machine's operations into well-defined states—such as idle, coin detection, product selection, dispensing, and reset—the system achieves predictable behavior, reduced complexity, and improved reliability. The FSM approach ensures minimal switching activity, which directly

contributes to lower dynamic power consumption. Optimizations such as clock gating, state minimization, and efficient encoding further enhance energy efficiency without compromising performance. The modular Verilog design also provides scalability, allowing easy extension to support additional products or payment methods.

Overall, the project validates that FSM-based architectures are highly suitable for embedded applications requiring low power, deterministic control, and cost-effective hardware implementation. This vending machine design not only meets functional requirements but also highlights the importance of power-aware digital design in modern systems.

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