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CMOS-BASED DESIGN AND REVIEW OF A 4-BIT NUMERICALLY CONTROLLED OSCILLATOR WITH DUAL FREQUENCY SELECT WORD CAPABILITY

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Abstract: Numerically Controlled Oscillators (NCOs) play a crucial role in modern digital communication systems due to their flexibility, precision, and ease of integration with digital architectures. With the advancement of complementary metal–oxide–semiconductor (CMOS) technology, the implementation of compact, low-power, and high-speed NCOs has become feasible for System-on-Chip (SoC) applications. This paper presents a comprehensive review of CMOS-based NCO architectures, focusing on design methodologies, key building blocks, and performance trade-offs. Special emphasis is given to low-bit architectures such as 4-bit NCOs and the concept of dual frequency select words for multi-frequency generation. The study highlights recent advancements, design challenges, and future research directions in CMOS-based digital oscillators.

Index Terms - NCO, CMOS, Phase Accumulator, Digital Oscillator, Dual Frequency Word, Low Power Design, FPGA/ASIC Implementation

I. INTRODUCTION

Oscillators are fundamental components in communication and signal processing systems. Traditional analog oscillators, such as Voltage-Controlled Oscillators (VCOs), have limitations in terms of noise sensitivity, process variation, and scalability. In contrast, digital oscillators such as NCOs provide superior frequency resolution and stability.

An NCO generates discrete-time sinusoidal signals using digital techniques, making it highly suitable for integration in CMOS-based digital systems. With increasing demand for compact and power-efficient designs, CMOS technology has become the preferred platform for implementing digital oscillators.

Recent research shows that CMOS-based oscillators can achieve low power consumption and wide tuning ranges by leveraging digital control mechanisms and optimized circuit techniques. Furthermore, digital-controlled oscillators (DCOs), closely related to NCOs, have gained popularity due to their scalability and compatibility with all-digital phase-locked loops (ADPLs **)**

II.FUNDAMENTALS OF NUMERICALLY CONTROLLED OSCILLATOR

2.1 Basic Principle

A Numerically Controlled Oscillator (NCO) is a digital signal generation system that produces periodic waveforms by iteratively updating a discrete phase value. The core principle of operation relies on a phase accumulator, which increases its stored phase value at every clock cycle by a predefined increment known as the

frequency control word (FCW). This accumulated phase is then mapped to amplitude values to generate the desired waveform.

The relationship between the generated output frequency and system parameters can be expressed as:

$$Fout = K * \frac{Fclk}{2^N}$$

Where;

Fclk represents the system clock frequency and N denotes the bit-width of the phase accumulator.

This mathematical relation indicates that the output frequency is directly proportional to the selected control word, thereby enabling precise and programmable frequency synthesis through purely digital means.

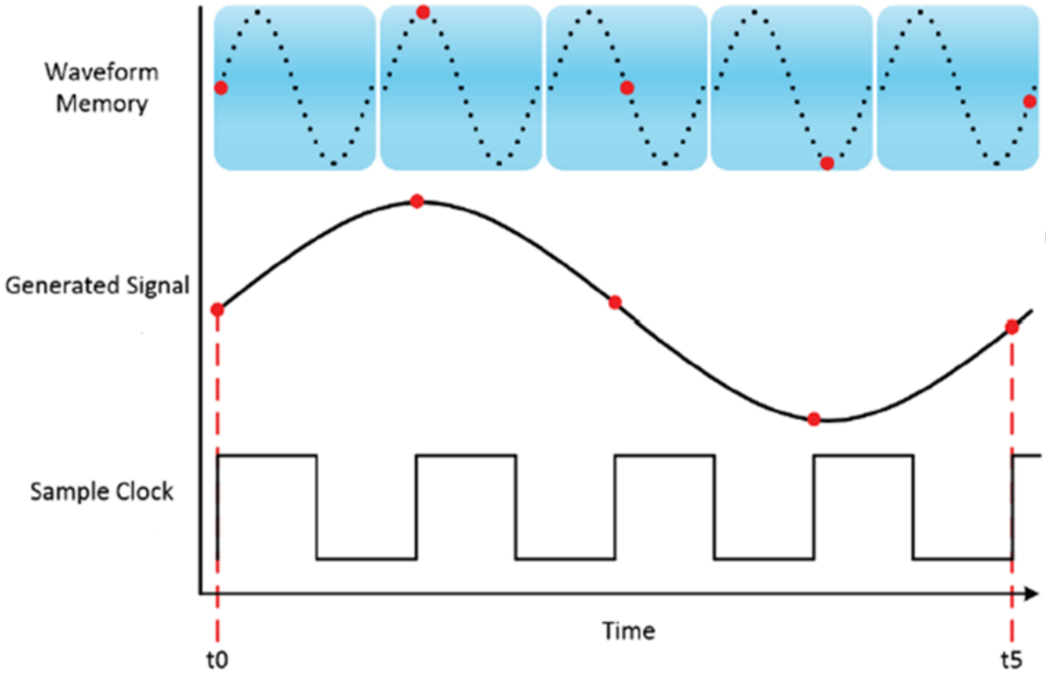

Figure 1: Illustration of the operation of NCO

The concept of NCO can be bitterly understanding by drawing a sine wave by putting the numerical values as a structure to sine signal.

Total **sine wave one cycle is of 360 degree**. So we divide it into 16 samples by 22.50 degree each. Values are shown in table below;

Table 1: Sine values generations using excel sheet

Sr. No.	Degree	Radian Value	Sine value
1	0	0	0
2	22.5	0.392699082	0.382683432
3	45	0.785398163	0.707106781
4	67.5	1.178097245	0.923879533
5	90	1.570796327	1
6	112.5	1.963495408	0.923879533
7	135	2.35619449	0.707106781
8	157.5	2.748893572	0.382683432
9	180	3.141592654	1.22515E-16
10	202.5	3.534291735	-0.382683432
11	225	3.926990817	-0.707106781
12	247.5	4.319689899	-0.923879533
13	270	4.71238898	-1
14	292.5	5.105088062	-0.923879533
15	315	5.497787144	-0.707106781
16	337.5	5.890486225	-0.382683432
17	360	6.283185307	-2.4503E-16

By selecting the sine values, form the table and by inserting the **shape from the insert menu of the excel sheet**, we will get a sinusoidal waveform as shown.

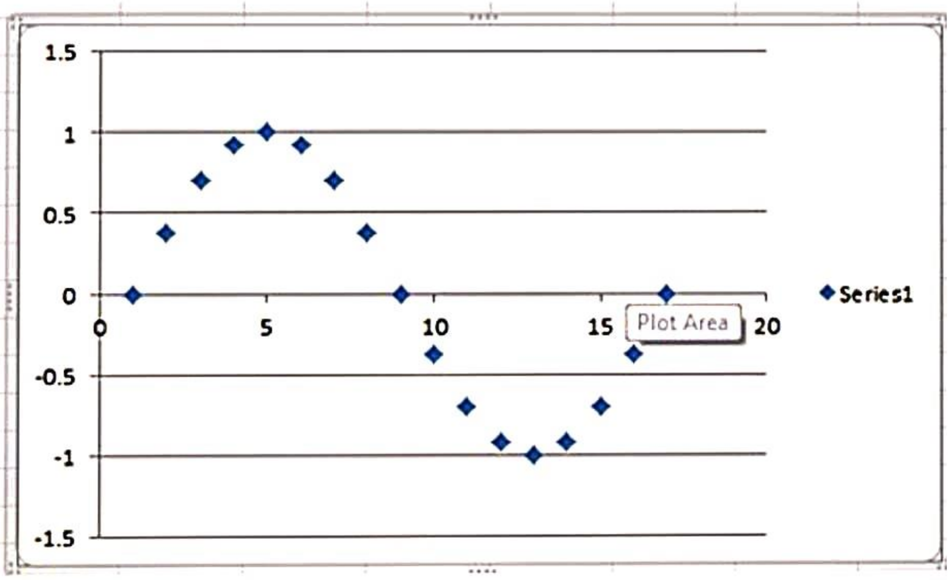

Figure 2: Sine wave generator using dots in excel sheet

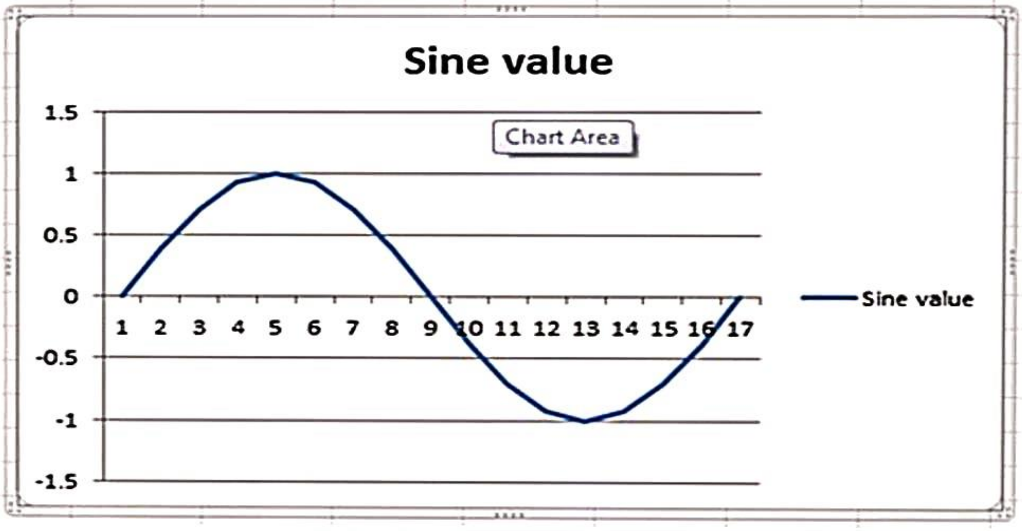

Figure 3: Sine wave generator using line in excel sheet

2.2 NCO Architecture

A conventional NCO architecture is composed of three essential functional blocks: the phase accumulator, the phase-to-amplitude conversion unit, and, in certain cases, a digital-to-analog converter. The phase accumulator acts as the central element responsible for generating a linearly increasing phase sequence. This phase information is then translated into corresponding amplitude values through the phase-to-amplitude converter, which is commonly implemented using either lookup tables or iterative computational methods such as the Coordinate Rotation Digital Computer (CORDIC) algorithm. When an analog output is required, a digital-to-analog converter is employed to convert the digitally generated waveform into a continuous-time signal.

III. CMOS IMPLEMENTATION OF NCO

3.1 Advantages of CMOS Technology

Complementary Metal–Oxide–Semiconductor (CMOS) technology has become the dominant platform for implementing digital systems, including NCOs, due to its inherent advantages. One of the most significant benefits of CMOS is its extremely low static power consumption, as current flows only during switching events. Additionally, CMOS circuits exhibit strong immunity to noise, which enhances reliability in high-speed digital environments. The scalability of CMOS technology to deep submicron levels allows designers to achieve higher integration density and improved performance. These characteristics collectively make CMOS an ideal choice for implementing compact, power-efficient, and high-speed digital oscillators.

3.2 CMOS-Based Oscillator Techniques

Within CMOS technology, several oscillator architectures have been developed, each offering distinct advantages depending on the application requirements. Ring oscillators are widely adopted due to their simple structure, small area footprint, and ease of integration. In contrast, LC oscillators provide superior phase noise performance, making them suitable for high-frequency and precision applications. Digitally controlled oscillators (DCOs) represent another important class, where frequency tuning is achieved through digital control signals, enabling seamless integration with digital systems.

To further enhance performance, modern CMOS oscillator designs incorporate advanced techniques such as current reuse, which improves power efficiency by sharing bias currents among circuit elements, and adaptive biasing, which dynamically adjusts operating conditions to optimize performance. Additionally, fine and coarse tuning mechanisms are often employed to achieve a wide frequency tuning range while maintaining stability and low phase noise. These innovations contribute to improved efficiency, broader tuning capability, and enhanced signal quality in CMOS-based oscillator systems.

IV. LOW-BIT (4-BIT) NCO DESIGN CONSIDERATION

4.1 Motivation for 4-bit Design

The design of low-bit NCOs, particularly 4-bit architectures, is motivated by the need for simplicity, reduced hardware requirements, and low power consumption. Such designs are especially relevant in educational environments, where they provide a clear understanding of fundamental concepts, as well as in prototype systems and embedded applications where resource constraints are significant. By limiting the bit-width of the phase accumulator, the overall circuit complexity is minimized, leading to faster operation and reduced silicon area.

4.2 Design Trade-offs

Despite their advantages, low-bit NCO designs inherently involve certain trade-offs. The most prominent limitation is the reduced frequency resolution, as a smaller number of phase levels leads to larger frequency steps. However, this reduction in precision is compensated by benefits such as compact implementation, lower power consumption, and simplified design complexity. A 4-bit phase accumulator cycles through only sixteen discrete states, resulting in coarse phase progression. Nevertheless, this characteristic enables faster computation and efficient hardware utilization, making such designs suitable for applications where ultra-high precision is not a primary requirement.

V. DUAL FREQUENCY SELECT WORD CONCEPT

5.1 Concept Overview

The Dual Frequency Select Word (DFSW) concept extends the functionality of a conventional NCO by enabling the generation of multiple frequencies within a single system. Instead of relying on a single frequency control word, the DFSW approach incorporates two predefined control words, allowing the oscillator to switch between different output frequencies dynamically. This capability is particularly beneficial in modern communication systems that require rapid frequency transitions and multi-band operation.

5.2 Implementation Approach

In a DFSW-based NCO, two separate frequency control words are defined, each corresponding to a specific output frequency. A control signal determines which of the two control words is applied to the phase accumulator at any given time. This selection mechanism is typically implemented using a multiplexer, which ensures seamless switching between the two frequencies. The transition occurs without interrupting the operation of the oscillator, thereby maintaining signal continuity and stability.

5.3 Applications

The ability to switch between multiple frequencies makes DFSW-based NCOs highly suitable for advanced communication systems. In software-defined radio, such flexibility allows dynamic adaptation to different communication standards and frequency bands. Similarly, digital modulation techniques benefit from rapid frequency changes for encoding information, while spread spectrum systems utilize frequency hopping to enhance security and resistance to interference. These applications highlight the practical significance of incorporating dual frequency control mechanisms in NCO design.

VI. LITERATURE SURVEY / REVIEW OF EXISTING WORK

The development of Numerically Controlled Oscillators (NCOs) has evolved significantly over the years, driven by the increasing demand for high-speed, low-power, and highly accurate frequency synthesis in digital communication systems. Early research in this domain primarily focused on improving the architectural efficiency of NCOs, particularly the phase accumulator, which forms the core of the system.

One of the notable contributions in this direction introduced a pipelined architecture for the phase accumulator, demonstrating that segmentation of arithmetic operations could substantially improve the operational speed while maintaining moderate hardware complexity. This approach enabled higher clock frequencies and became a foundational technique for modern high-performance NCO designs.

With the advancement of programmable logic devices, several researchers shifted their focus toward FPGA-based implementations of NCOs to validate architectural concepts before ASIC realization. In such studies, lookup table (LUT)-based phase-to-amplitude conversion emerged as a preferred approach due to its simplicity and deterministic performance. These implementations demonstrated that digital NCOs could achieve high accuracy and stability with relatively straightforward hardware mapping. Furthermore, the flexibility of FPGA platforms allowed designers to explore various trade-offs between memory utilization and computational complexity, especially when implementing sinusoidal waveform generation.

A significant area of investigation within NCO design has been the comparison between LUT-based and algorithmic approaches such as the Coordinate Rotation Digital Computer (CORDIC). While LUT-based designs offer rapid output generation due to direct memory access, they tend to consume considerable memory resources, particularly for higher resolution systems. On the other hand, CORDIC-based architectures reduce memory dependency by employing iterative shift-add operations to compute trigonometric functions. However, this comes at the cost of increased latency and control complexity. These contrasting characteristics highlight the importance of selecting an appropriate architecture based on application-specific constraints such as area, speed, and power consumption, especially in CMOS implementations where silicon real estate is a critical factor.

As CMOS technology continued to scale into deep submicron regimes, researchers began to explore the direct implementation of NCOs using optimized digital circuits. CMOS-based NCO designs demonstrated significant improvements in power efficiency, integration density, and operational speed. In particular, designs implemented in advanced technology nodes incorporated optimized phase accumulators, efficient memory structures for waveform generation, and minimized interconnect delays. Some of these works also introduced the concept of multi-frequency generation using programmable frequency control words, thereby enhancing the functional flexibility of the oscillator without significantly increasing hardware overhead.

Further advancements led to the development of dual-mode and multi-frequency NCO architectures, which are particularly relevant for modern communication systems requiring dynamic frequency switching. These designs enabled the oscillator to operate at multiple predefined frequencies by selecting between different frequency control words. Such architectures are highly beneficial in applications such as frequency hopping spread spectrum systems and software-defined radios, where rapid and reliable frequency transitions are essential. The integration of control logic to manage frequency selection added a new dimension to NCO design, emphasizing both flexibility and responsiveness.

High-resolution NCO implementations have also been extensively studied, with several designs employing large bit-width phase accumulators to achieve fine frequency resolution and reduced quantization noise. These systems often incorporate advanced techniques such as pipelining, ROM compression, and segmentation to manage the increased hardware complexity. While these approaches improve signal quality and spectral purity, they also result in higher power consumption and larger silicon area, making them less suitable for compact and low-power applications.

An important design consideration that has emerged from the literature is the impact of phase accumulator bit-width on overall NCO performance. Increasing the bit-width enhances frequency resolution and reduces phase truncation errors, thereby improving output signal quality. However, this improvement comes at the expense of increased circuit complexity and power consumption. Consequently, there is a growing interest in exploring low-bit NCO designs that can achieve acceptable performance while minimizing hardware requirements. Such designs are particularly relevant for embedded systems and educational applications, where simplicity and efficiency are of paramount importance.

In parallel, advancements in CMOS oscillator design, including voltage-controlled and digitally controlled oscillators, have indirectly contributed to the evolution of NCO architectures. Improvements in phase noise reduction, frequency stability, and power efficiency in these oscillators provide valuable insights for the design of high-performance digital frequency synthesizers. The integration of these techniques with digital NCO architectures opens new avenues for hybrid designs that leverage the strengths of both analog and digital domains.

Despite the extensive body of research, it is evident that limited attention has been given to the implementation of low-bit CMOS-based NCOs with enhanced functional capabilities such as dual frequency select words. Most existing works focus either on high-resolution designs or general-purpose architectures without specifically addressing the challenges associated with compact, low-complexity implementations. This gap highlights the need for further investigation into efficient low-bit NCO designs that can support multi-frequency operation while maintaining minimal hardware overhead and power consumption.

6.2 Summary of Literature Findings

From the above survey, the following key observations can be made:

- Pipeline architectures improve NCO speed and efficiency
- LUT and CORDIC represent fundamental design trade-offs
- CMOS scaling enhances integration and reduces power
- Dual-frequency and multi-mode NCOs enable flexible communication systems
- Bit-width significantly impacts accuracy and noise performance
- There is limited work specifically focused on **low-bit CMOS NCO with dual frequency select capability**
- ecent literature highlights several trends:
- **Area and Power Optimization:** A CMOS-based NCO implemented in deep submicron technology demonstrates reduced area and improved speed using optimized digital architectures.
- **High-Speed Digital Oscillators:** Digital-controlled oscillators (DCOs) are widely studied for high-speed applications, offering better integration with digital systems and reduced analog complexity.
- **Wide Tuning Range:** Modern CMOS oscillator designs employ variable capacitance and bias control techniques to achieve wide tuning ranges and improved efficiency

6.3 Research Gap Identified

Despite extensive research, the following gaps remain:

- Limited studies on **4-bit CMOS-based NCO implementations**
- Lack of optimized **dual frequency select word architectures** in low-bit designs
- Need for **compact, low-power CMOS NCO suitable for embedded applications**

VII. PROPOSED METHODOLOGY

The proposed work presents a **CMOS-based implementation of a 4-bit Numerically Controlled Oscillator (NCO)** incorporating a **dual frequency select word (DFSW) mechanism** to enable flexible and efficient multi-frequency generation. The design focuses on achieving a balance between hardware simplicity, power efficiency, and functional adaptability, making it suitable for compact embedded and communication applications.

7.2 Overall Architecture

The proposed NCO architecture consists of four primary functional blocks: a dual frequency control unit, a phase accumulator, a phase-to-amplitude conversion unit, and an output generation stage. The novelty of the design lies in the integration of two independent frequency control words, allowing dynamic switching between two discrete output frequencies without requiring reconfiguration of the system.
The overall operation is governed by a system clock fclkf which synchronizes all internal operations. Based on the selection control signal, one of the two frequency control words is fed into the phase accumulator.

7.3 Block Diagram of Proposed Dual-FCW NCO

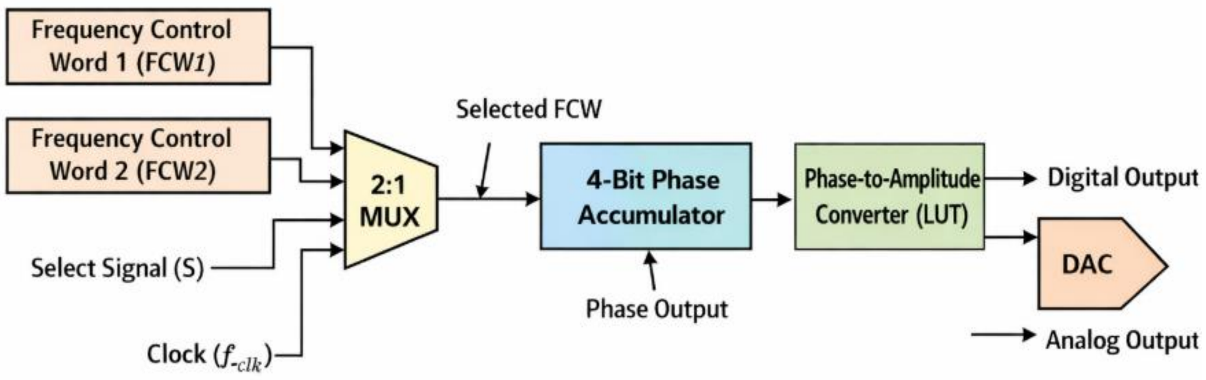

Figure 4: Block Diagram of Proposed Dual-FCW NCO

The block diagram illustrates the dual frequency control words (FCW1 and FCW2) connected to a multiplexer. The selected FCW is applied to the phase accumulator. The output of the phase accumulator is provided to the phase-to-amplitude converter (LUT-based), which generates the corresponding digital waveform samples. The final output is obtained either as a digital signal or through a DAC for analog waveform generation.

7.4 Dual Frequency Control Word (DFSW) Unit

The DFSW unit is responsible for selecting between two predefined frequency control words, denoted as FCW1FCW_1FCW1 and FCW2FCW_2FCW2. A control signal S determines the active frequency:

$$FCW = \begin{cases} FCW_1, & \text{if } S = 0 \\ FCW_2, & \text{if } S = 1 \end{cases}$$

This approach enables real-time frequency switching without interrupting system operation. The selection logic is implemented using a CMOS-based 2:1 multiplexer, optimized for low propagation delay and minimal switching power.

7.5 Phase Accumulator Design

The phase accumulator is implemented as a **4-bit register with an adder,** forming the core of the NCO. At every clock cycle, the selected frequency control word is added to the current phase value:
CC

$$\Phi[n] = (\Phi[n-1] + FCW) \mod 2^N$$

where:

- Φ[n]\Phi[n]Φ[n] is the current phase value
- FCWFCWFCW is the selected frequency control word
- N=4 (bit-width of the accumulator)

Due to the 4-bit implementation, the phase wraps around after 2^4=16 states, resulting in a discrete phase progression. The simplicity of the 4-bit design ensures reduced hardware complexity and faster operation, though at the cost of limited frequency resolution.
The output frequency is given by:

$$Fout = K * \frac{Fclk}{2^N}$$

This expression clearly establishes how the output frequency varies as a function of the control word, thereby allowing flexible and programmable frequency synthesis.

7.6 Phase Accumulator Operation

Phase Accumulator Operation provide the cyclic increment of the phase value from 0 to 15 (for 4-bit implementation). Upon reaching the maximum value, the accumulator wraps around to zero. Different FCW values produce different step sizes, resulting in varying output frequencies.

7.7 Phase-to-Amplitude Conversion (PAC)

The phase-to-amplitude conversion is implemented using a **lookup table (LUT)** approach due to its simplicity and suitability for low-bit designs. The LUT stores precomputed amplitude values corresponding to discrete phase inputs.
Given the limited number of phase states (16), the LUT size remains small, which significantly reduces memory requirements. The output amplitude A[n]A[n]A[n] is obtained as:

$$A[n] = \sin\left(\frac{2\pi \cdot \Phi[n]}{2^N}\right)$$

7.8 CMOS Implementation Strategy

The entire NCO is designed using CMOS logic to ensure low power consumption and high integration capability. The following design considerations are adopted:

- The phase accumulator uses ripple-carry or carry-look ahead adders depending on speed requirements
- The multiplexer for DFSW is implemented using transmission gate logic to minimize power and delay
- The LUT is realized using static CMOS memory structures
- Clock gating techniques may be incorporated to reduce dynamic power consumption.

7.9 Timing and Frequency Switching Behavior

The inclusion of dual frequency control words allows instantaneous switching between two frequencies. The transition occurs at the next clock edge without introducing glitches, provided that proper synchronization is maintained.

VIII. CONCLUSION

This paper has presented a comprehensive review of CMOS-based Numerically Controlled Oscillator (NCO) architectures with particular emphasis on low-bit implementations and the incorporation of dual frequency select word functionality. The study examined the fundamental operating principles of NCOs, including phase accumulation and digital waveform generation, along with various architectural approaches such as LUT-based and CORDIC-based designs. The role of CMOS technology in enabling compact, low-power, and highly integrable oscillator implementations has also been critically analyzed.

From the literature, it is evident that while high-resolution NCO designs offer superior spectral performance and frequency precision, they often involve increased hardware complexity and power consumption. In contrast, low-bit designs, such as the 4-bit NCO considered in this work, provide a practical trade-off by significantly reducing circuit complexity and resource utilization, making them suitable for embedded and educational applications. Furthermore, the introduction of dual frequency select words enhances the functional capability of the oscillator by allowing dynamic switching between multiple frequencies, which is particularly beneficial in modern communication systems requiring adaptability and real-time control.

Despite the progress reported in existing research, there remains a noticeable gap in the development of optimized low-bit CMOS-based NCO architectures that effectively integrate multi-frequency operation with minimal hardware overhead. The insights gathered from this review highlight the importance of balancing resolution, power efficiency, and flexibility in oscillator design. Future work in this area can focus on improving waveform accuracy, reducing quantization effects, and exploring hybrid architectures that combine digital precision with analog performance advantages.

Overall, CMOS-based NCOs continue to be a promising solution for digital frequency synthesis, and the integration of simplified architectures with enhanced control features represents a meaningful direction for further research and development.

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