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Design And Analysis Of A CMOS Ring Oscillator For 5G Wireless Communication

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Abstract: This paper presents a CMOS-based ring oscillator designed to function as a Voltage-Controlled Oscillator (VCO) for 5G mobile communication systems. The proposed architecture combines a current-starved ring oscillator with a negatively skewed delay element to enhance performance, efficiency, and tuning capabilities. Operating at a control voltage of 1.15 V and a supply voltage of 2 V, the oscillator achieves a high output frequency of 9.35 GHz with a harmonic distortion of 13.82%.

The design focuses on low power consumption, compact size, and wide tuning range—key requirements for modern 5G applications. With carefully selected passive components and an optimized circuit layout, this oscillator is a promising solution for next-generation wireless devices requiring high speed and energy efficiency.

Keywords: 5G Communication, Low Power design, High Frequency Oscillator, VLSI Design.

I. INTRODUCTION

Radio Frequency (RF) circuits play a key role in modern communication systems, as they operate at high frequencies required for sending and receiving signals over long distances. These circuits are found in a wide range of technologies, including mobile phones, satellite systems, radar, and wireless networks. Unlike analog circuits, which typically operate at lower frequencies, RF circuits are designed to handle fast signal changes and high-speed data transmission. To properly design and analyse RF circuits, engineers use frequency domain techniques such as the Fast Fourier Transform (FFT). These techniques help in understanding how signals behave at different frequencies and reveal important performance factors such as phase noise, harmonic distortion, interference, and signal accuracy. This information is essential for optimizing circuit performance and ensuring reliable operation in high-frequency environments. One of the most important components in any communication system is the oscillator. Oscillators generate stable clock signals that keep the system synchronized and control timing. These circuits rely on positive feedback and must satisfy a condition known as the Barkhuizen Criterion. According to this rule, the product of the amplifier gain and the feedback factor must equal one, and the total phase shift around the loop must be 360 degrees (or 2π radians) to maintain continuous oscillation. A basic type of oscillator is the LC tank oscillator, which uses inductors and capacitors to set the oscillation frequency. While simple, LC oscillators tend to be bulky and consume more power, making them less suitable for compact and energy-efficient applications such as smartphones and other 5G-enabled devices. As mobile technology advances toward 5G, there is a growing need for oscillators that are not only high-frequency but also small in size and low in power consumption. To address these challenges, this project proposes a CMOS-based ring oscillator architecture tailored for 5G communication. CMOS (Complementary Metal-Oxide-Semiconductor) technology allows for efficient, scalable integration in VLSI circuits. The proposed oscillator design combines the advantages of a current-starved ring oscillator with a negatively skewed delay element, improving both frequency control and power efficiency.

Simulation results show that the oscillator operates at a dominant frequency of 9.35 GHz, with a control voltage of 1.15 V, a supply voltage of 2 V, and a harmonic distortion of 13.82%. These results demonstrate its potential for use in high- speed, low-power 5G communication systems.

II. Literature Survey

1. Routh et al.

KEY ASPECTS: VOLTAGE-CONTROLLED OSCILLATOR (VCO) DESIGN, LOW POWER CONSUMPTION, OPTIMIZED OUTPUT SWING.

APPROACH: USED A CURRENT MIRROR TO ENHANCE DRAIN CURRENT. ACHIEVED 6.71 MW POWER USAGE AND -112
DB/HZ PHASE NOISE AT 180 NM TECHNOLOGY.

2. Kavyashree et al.

KEY ASPECTS: COMPARISON OF CMOS RING OSCILLATOR TYPES (STANDARD, CURRENT-STARVED, NEGATIVELY SKEWED).

APPROACH: HIGHLIGHTED NOISE PERFORMANCE AND EFFICIENCY ADVANTAGES OF EACH DESIGN.

3. Shekar and Qureshi

KEY ASPECTS: FIVE-STAGE CMOS INVERTER-BASED VCO, LINEAR FREQUENCY TUNING, REDUCED JITTER, BROAD TUNING RANGE, COMPACT SIZE.

APPROACH: USED RESISTOR-LOADED NMOS CHAIN; CONSIDERED TEMPERATURE, SUPPLY VOLTAGE, AND PROCESS VARIATIONS.

4. Kompella and Abdul Rajak

KEY ASPECTS: HYBRID CMOS RING OSCILLATOR, LOW OUTPUT NOISE, WIDE TUNABILITY.

APPROACH: ACHIEVED 2.52 GHZ FREQUENCY, -111 DB/HZ PHASE NOISE, AND 8.69 PS SETTLING TIME.

5. Caram et al.

KEY ASPECTS: VCOS WITH INDUCTIVE LOADS FOR IMPROVED PHASE NOISE AND POWER HANDLING.

APPROACH: COMPARED INDUCTIVE LOAD OSCILLATORS TO TRADITIONAL INVERTER-BASED TYPES**.**

6. Hara et al.

KEY ASPECTS: 3.5 GHZ VCO BASED ON THIN-FILM BULK ACOUSTIC RESONATOR (FBAR), HIGH ACCURACY AND STABILITY.

APPROACH: AVOIDED SYNCHRONIZATION ISSUES; TARGETED APPLICATIONS LIKE ROBOTICS AND REAL-TIME SENSOR NETWORKS.

III. Ring Oscillator

3.1 Ring Oscillator

A Ring Oscillator Is formed by connecting an Odd number of Inverting Amplifiers in a loop. The output of the last inverter is fed back into the first, creating a positive feedback loop. However, because this kind of positive feedback is inherently unstable, a self-regulating element is always used alongside the amplifiers to maintain stable oscillation.

Take, for example, a simple three-stage ring oscillator (like the one shown in Figure 4.1.2). Each stage consists of an amplifier (A), a capacitor (C), and a resistor (R). Zooming into one amplifier stage, it's usually made from CMOS transistors typically a combination of a PMOS and an NMOS transistor working together in a common-source configuration.

The capacitors in each stage play an important role by introducing delay. They temporarily hold the input signal for a short period as they charge and discharge, which ensures that the signal is delayed properly as it passes through each inverter stage.

Because of this delay, the overall oscillation frequency depends on the total delay introduced by all the stages combined. If there are 'n' stages, and each stage introduces a delay of t _delay, the frequency of oscillation (f) can be calculated by the formula:

$$f = \frac{1}{n \times t_{delay}}$$

Equation. 1

This means the oscillation frequency is inversely proportional to the total delay across all stages.

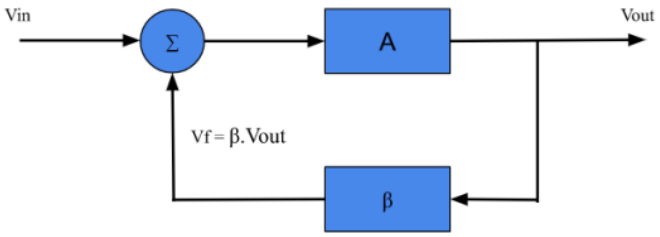

Figure 3.1: Positive Feedback network

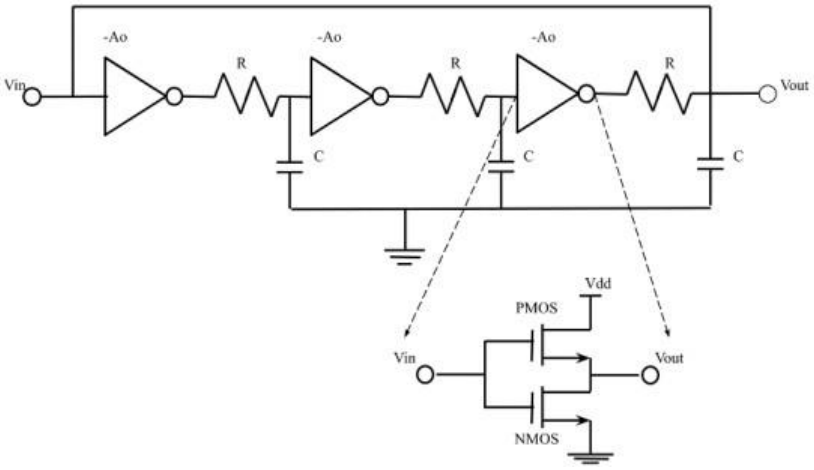

Figure 3.1.2: 3Stage CMOS Ring Oscillator

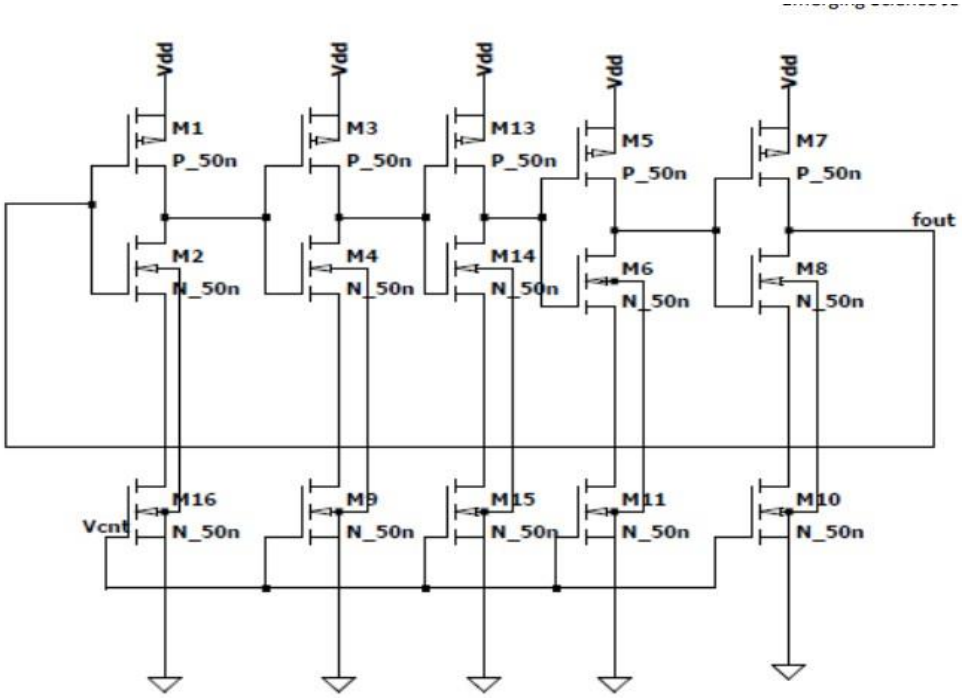

Figure 3.1.3: Conventional Ring Oscillator

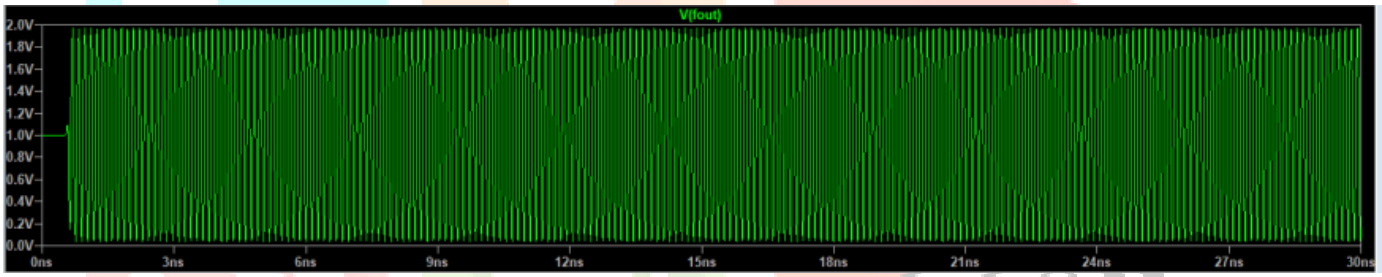

Figure 3.1.4: Output waveform of Conventional Ring Oscillator

3.2 Negative Skewed CMOS Ring VCO.

One of the primary limitations of conventional ring VCOs is their relatively large delay time, which negatively impacts performance. To mitigate this issue, a negatively skewed VCO architecture has been introduced, wherein only the PMOS transistor in the CMOS configuration experiences a delay. This selective delay mechanism allows the system to achieve faster response times and improved overall performance. However, implementing this approach requires a higher oscillation frequency and a modest increase in power consumption. To evaluate the effectiveness of this design, a prototype was implemented using a standard 50 nm technology node, without initially considering the oscillation frequency or waveform shape. The schematic of the two-stage delay structure, incorporating the negatively skewed delay, along with the standard ring oscillator configuration for the negatively skewed CMOS ring VCO, is illustrated in Figure 6. The corresponding output waveform, shown in Figure 3.2.2 , demonstrates an oscillation frequency of 3.35 GHz.. The simulation results clearly indicate that this design offers improved response characteristics and reduced delay compared to traditional configurations, although it still contends with the typical ring VCO issue of elevated phase noise. Notably, a total harmonic distortion (THD) of 36.62% was observed in the output signal.

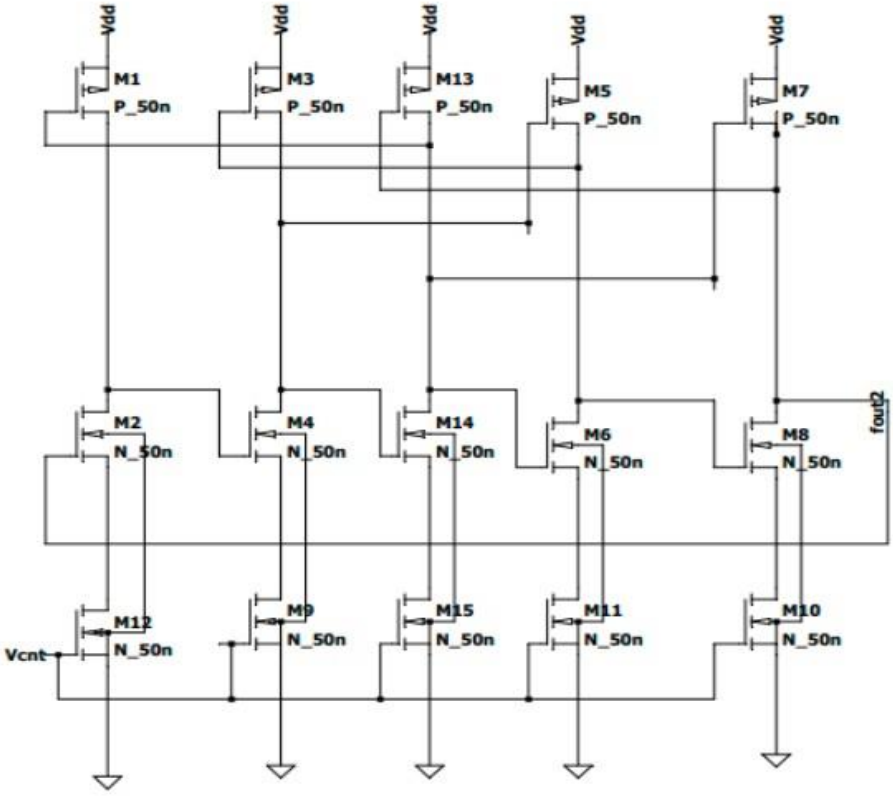

Fig.3.2.1 Negative Skewed CMOS Ring Oscillator Simulated

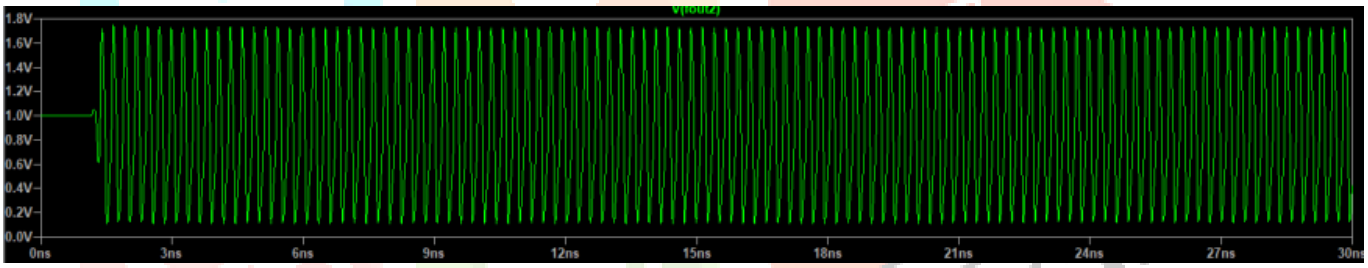

Figure 3.2.2: Output waveform of Negative Skewed CMOS Ring Oscillator

3.3 Current Starved CMOS Ring VCO

A major drawback in the earlier two CMOS designs was the lack of proper current regulation and control. To address this issue, the improved design increases the number of CMOS transistors and modifies their roles to function similarly to current sinks and drains, which are connected to standard inverters. In this setup, each inverter includes a built-in current source that also acts as a current limiter, helping to regulate the current flow. Additionally, matching drains are included to extract any excess current, ensuring that the current remains limited across all inverters. The amount of current drawn is primarily determined by the supply voltage (Vdd). This controlled current flow reduces both phase noise and power consumption. Moreover, directing the current through multiple branches of the circuit improves the quality of the output waveform. However, one trade-off is that this design requires more physical space due to the increased number of CMOS transistors. To test its performance, the circuit was implemented using a standard 50 nm technology node, without initially focusing on the oscillation frequency or waveform details. The implemented design is shown in Figure 8, and the output waveform in Figure 9 demonstrates an oscillation frequency of 2.3 GHz.

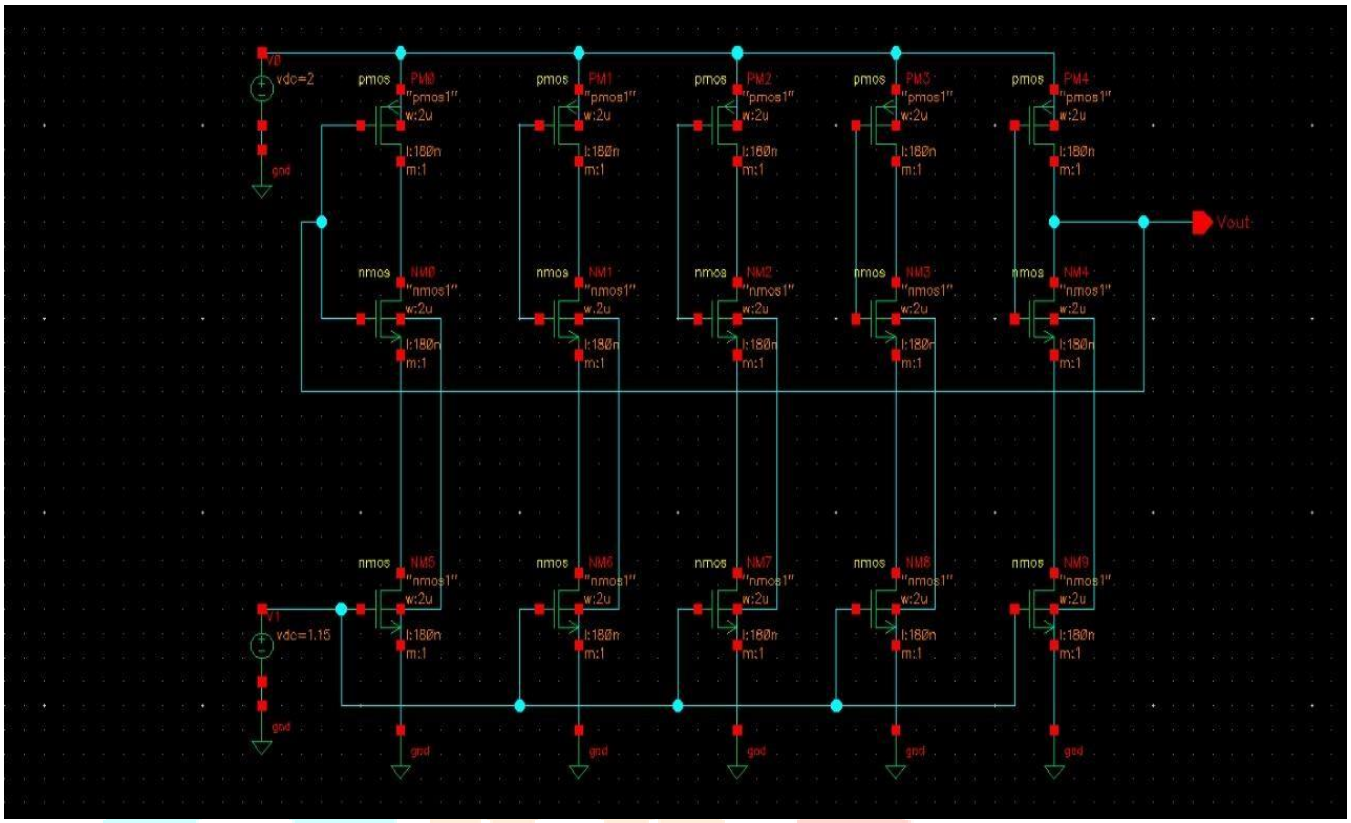

Fig.3.3.1 . Current Starved CMOS Ring Oscillator Simulated

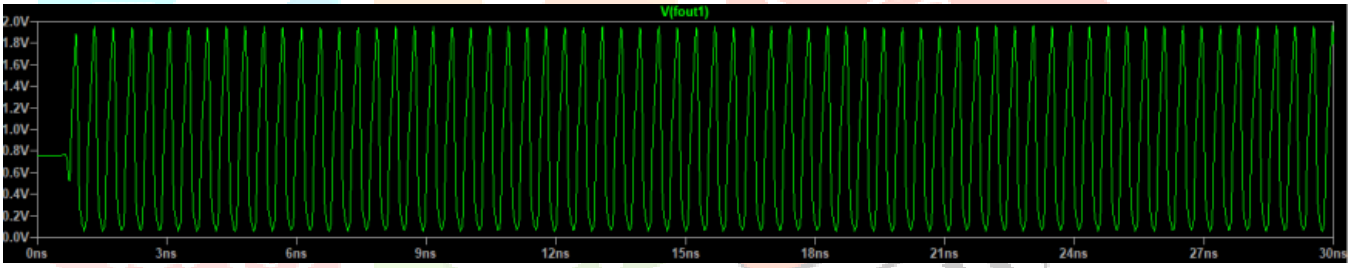

Fig 3.3.2: Output waveform of Current Starved CMOS Ring Oscillator

3.4 Proposed Architecture

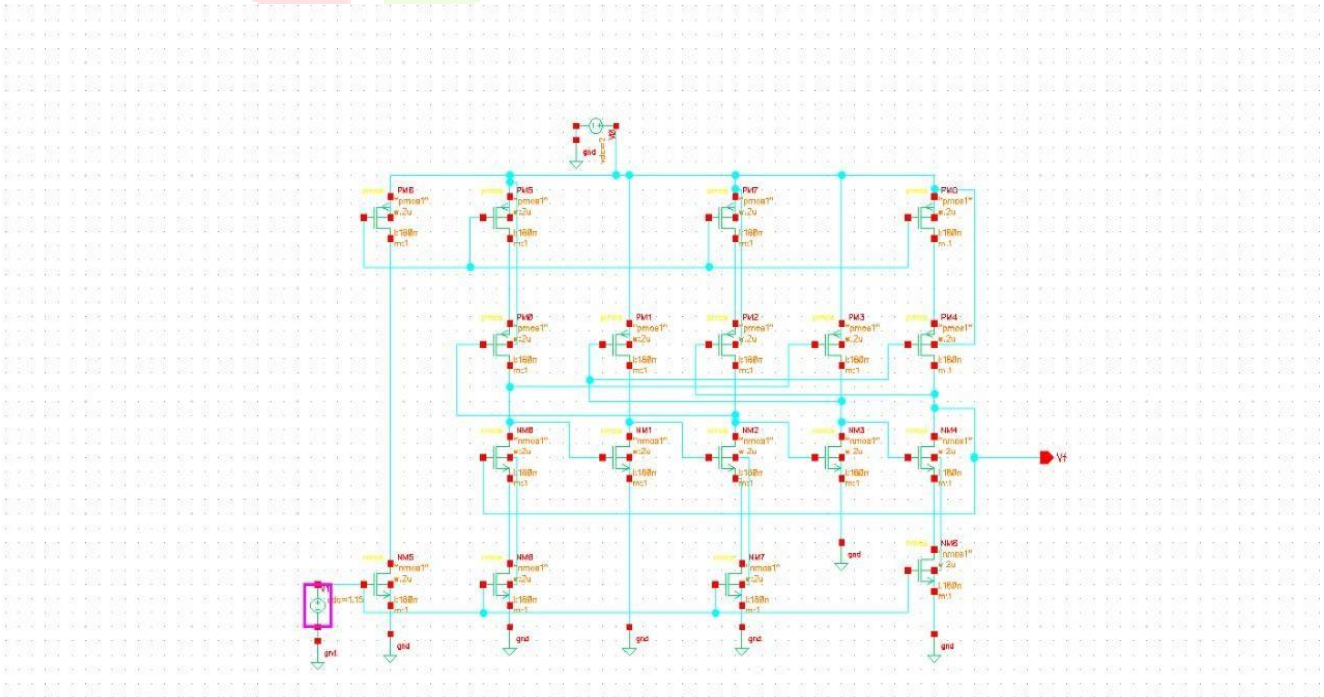

Fig. 3.4.1. Proposed Architecture Simulated

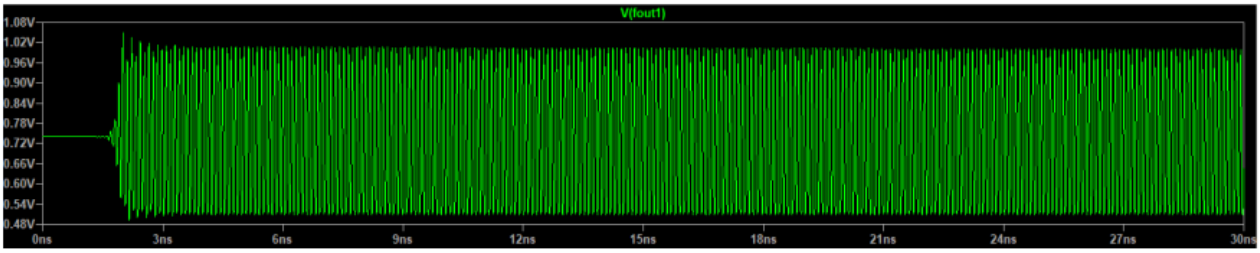

Fig 3.4.2 Output waveform of the proposed Architecture

The proposed CMOS ring oscillator architecture smartly combines both negative skewed and current-starved inverter topologies to achieve an optimal balance between high performance and low power consumption. In this hybrid design, the negative skewed inverter stages are implemented using transistors M1 to M10. These stages are modified such that the PMOS transistors introduce intentional delay during the rising edge of the signal. This skewing reduces the average propagation delay and allows for faster switching, thereby increasing the oscillator's overall frequency. On the other hand, the current-starved inverter stages are realized using transistors M11 to M16. These transistors limit the current available to each inverter stage by placing additional control elements in the supply paths (Vdd and GND). This technique effectively reduces power consumption and helps control phase noise by stabilizing the current flow, making it ideal for energy-efficient oscillator operation. The biasing and control of these current-starved stages are managed by transistors M17 to M21, which regulate the gate voltages of the current control devices based on the input control voltage (Vc). This enables fine-grained, voltage-controlled tuning of the oscillation frequency. The hybrid integration of these two techniques allows the architecture to capitalize on the advantages of both: high-speed performance from the negative skewed design and low power consumption from the current-starved design. The total delay in the ring is modeled as a weighted combination of the delays from each section, offering predictable and adjustable timing characteristics. As a result, the proposed design achieves a high operating frequency of 9.35 GHz and low harmonic distortion of 13.82%, outperforming conventional, skewed-only, or current-starved-only architectures. This makes it highly suitable for 5G communication systems, where both speed and efficiency are critical.

IV. Results and Discussion of Proposed Architecture

The waveform obtained as output is shown in Figure 5.1.4. The maximum voltage that can be served is one volt. This architecture has a higher frequency compared to other investigated architectures. Figure 6.1 illustrates the range of frequencies that the suggested design can produce through its FFT output. It turns out that 9.35 GHz is the most important frequency. Even more encouraging for 5Grelated uses is the existence of numerous frequencies over a broad range. The steps outlined below are an example of a design process for an application operating at a frequency of 27.7 GHz, which was picked at random. Using Equation 12, and assuming that the frequency of the application is already known, one can get the individual delays for the negatively skewed sections and the current-starved parts as follows:

$$\frac{1}{27.7\times10^{9}} = N_1\tau_{cs} + N_2\tau_{ns} \Rightarrow N_1\tau_{cs} + N_2\tau_{ns} = 0.0361\ ns$$

Equation.2

The particular application must be taken into consideration before deciding on the number of stages that will be used for each component, which is denoted by N1 and N2. If N1=3, N2=2, and the total number of stages is N=5, then Equation 13 will indicate the relation between the individual delays and the total delay for the stage.

$$\tau_{cs} = \frac{N_1}{N}\tau_d \Rightarrow \tau_{cs} = \frac{3}{5}(36.1\times10^{-12}) \Rightarrow \tau_{cs} = 0.0223\ ns$$
$$\tau_{ns} = \frac{N_2}{N}\tau_d \Rightarrow \tau_{ns} = \frac{2}{5}(36.1\times10^{-12}) \Rightarrow \tau_{ns} = 0.0145\ ns$$

Equation.3

After computing the individual delays, the operational parameters of the currently starved and negatively skewed parts are computed. From Equation 14, where Id is the saturation current, the total capacitance can be found as follows:

$$C_{tot} = \frac{\tau_{cs} I_d}{N_1 V_{dd}} \Rightarrow C = 0.0223ns \times \frac{360\mu A}{2V} \Rightarrow C = 0.3999fF$$

Equation.4

From Equation 5, the individual capacitance can be found as follows,

$$C_{tot} = \frac{5}{2} C'_{ox}\left(W_p L_p + W_n L_n\right) \Rightarrow C'_{ox} = 0.0159fF$$

Equation.5

The total delay of negative skewed portion allows the computation of the high to low and low to high delays, where for simplicity's sake they are taken as the same, as seen in Equation 16,

$$\tau_{ns} = \frac{\tau_{dlh} + \tau_{dhl}}{2N_2} \Rightarrow \tau_{dlh} = \tau_{dlh} = 0.0072ns$$

Equation.6

the operating capacitance of the negative skewed portion can be computed in Equation 17, with transistor parameters Vd=2V and Vtp=Vtn=0.3V,

$$\frac{c}{k_p} = \frac{\tau_{dlh}\left(V_{dd}+V_{tp}\right)}{\left(\frac{2V_{tp}}{V_{dd}+V_{tp}} + \ln\frac{3V_{dd}-4V_{tp}}{V_{dd}}\right)}; \frac{c}{k_n} = \frac{\tau_{dhl}\left(V_{dd}-V_{tn}\right)}{\left(\frac{2V_{tn}}{V_{dd}-V_{tn}} + \ln\frac{3V_{dd}-4V_{tn}}{V_{dd}}\right)} \Rightarrow \frac{c}{k_p} = \frac{c}{k_n} = \frac{0.0123\times10^{-9}}{0.3529\times\ln 2.4} = 0.0397 \times 10^{-9} sV$$

Thus, according to the application, the design can be modelled for specific requirements and adjusted to achieve results.

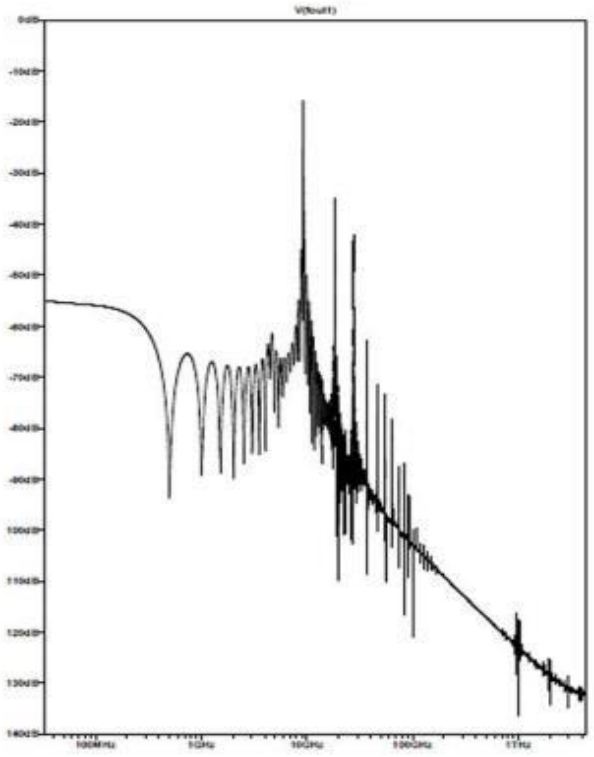

Figure 4.1: 4. FFT result of proposed architecture

V. Future Scope

- The proposed oscillator architecture can be seamlessly integrated with mixers, phase-locked loops (PLLs), and amplifiers to form complete transceiver modules compatible with 5G communication systems.
- Scaling the design to more advanced CMOS technology nodes offers the potential to further reduce power consumption while increasing the maximum achievable operating frequency.
- Future work will include layout generation, parasitic extraction, and post-layout simulations to validate the design's performance prior to fabrication.
- Comprehensive evaluation of phase noise and jitter using advanced RF simulation tools such as Spectre RF and P Noise will provide deeper insights into the oscillator's suitability for high-speed communication applications.
- Incorporating adaptive or digitally controlled biasing techniques can enhance frequency stability under varying temperature and supply voltage conditions.
- The robustness of the oscillator will be assessed across multiple process, voltage, and temperature (PVT) corners to ensure reliable operation in real-world environments.
- Expanding the oscillator's tuning range could enable its use across multiple 5G frequency bands and potentially in emerging 6G pre-standard frequency bands.
- Due to its low power characteristics, the oscillator can be adapted for integration in Internet of Things (IoT) sensor nodes and low-power edge computing platforms.
- The design may also serve as a key component in advanced clock generation or frequency synthesizer systems within digital and RF front-end architectures.
- Future enhancements may involve the application of machine learning and optimization algorithms to fine-tune transistor dimensions and biasing conditions for improved performance metrics.

VI. Conclusion

The VCO used in 5G transceivers must offer a wide tuning range, fast settling time, and low phase noise for optimal performance. While current-starved designs minimize harmonic distortion, they often compromise frequency range and occupy more area. Negative skew designs enhance frequency reach but require higher control voltage and increase distortion. The proposed architecture strikes a balance by combining current-starved and negatively skewed techniques, achieving high-frequency output (9.35, 18.71, and 28.07 GHz) with only 13.82% harmonic distortion.

Operating efficiently at a 2 V supply and 1.15 V control voltage, this design supports low-power, high-frequency applications like 5G.

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