IJCRT.ORG ISSN : 2320-2882

INTERNATIONAL JOURNAL OF CREATIVE RESEARCH THOUGHTS (IJCRT)

An International Open Access, Peer-reviewed, Refereed Journal

Low Power Common Source Amplifier Design For Analog Signal Processing Applications

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Abstract: The Common Source Amplifier is a widely used configuration in analog circuit design due to its simplicity and high voltage gain. This paper focuses on the design and simulation of a CS amplifier using CMOS technology, with applications targeted at digital to analog converter systems. The amplifier was implemented and analyzed using the Cadence Virtuoso design suite, emphasizing key parameters such as gain, output swing, bandwidth, and power efficiency. Design choices, including transistor sizing and biasing strategies, were carefully made to balance performance and area. The CS amplifier was integrated into a 4 bit digital to analog converter structure to evaluate its effectiveness in real-world signal processing tasks. Simulation results confirm that the amplifier provides sufficient gain and linearity for low-resolution digital to analog converter applications while maintaining low power consumption. This work highlights the practical design considerations and trade-offs involved in implementing CS amplifiers in modern integrated circuits.

Key Words **– Common Source Amplifier, Digital to Analog Converter, Analog Design, VLSI, CMOS.**

I. INTRODUCTION

Analog circuit design plays an important role in modern electronic systems, enabling the interface between digital logic and the real world. Among the fundamental building blocks of analog design, the Common Source (CS) amplifier stands out due to its versatility, relatively simple structure, and ability to provide significant voltage gain. The CS amplifier is the MOSFET equivalent of the BJT common-emitter amplifier, and it is extensively used in amplification stages of analog signal chains, including those found in audio circuits, sensor interfaces, and communication systems.

A Common Source amplifier operates by applying an input signal at the gate terminal of an NMOS or PMOS transistor, with the source terminal typically grounded and the drain connected to a load resistor or current source. When biased correctly, the transistor operates in the saturation region, allowing the circuit to amplify small input voltage variations into larger output signals. The CS configuration provides inverting gain, making it ideal for initial gain stages or intermediate signal processing blocks in larger analog systems.

In the context of Digital-to-Analog Converters (DACs), the role of the CS amplifier becomes particularly significant. A DAC converts discrete digital codes into corresponding analog voltages or currents. To ensure signal integrity and drive subsequent analog stages, the output of a DAC often requires buffering or amplification. Here, a Common Source amplifier can be employed to boost the analog output to a desired voltage level, improve linearity, or drive capacitive loads more effectively. This is especially true in low-resolution DACs, such as 4-bit architectures, where simple and power-efficient analog blocks are preferred.

II. LITERATURE REVIEW AND PROBLEM STATEMENT

The Common Source (CS) amplifier has long been established as a fundamental building block in analog circuit design. Many studies have been done and its characteristics in terms of gain, frequency response, and noise performance. Traditional textbooks and foundational papers have outlined its theoretical behavior and application in analog signal paths [1]. As CMOS technology has advanced into submicron and nanometer regimes, the design of CS amplifiers has evolved to address increased performance demands and scaling limitations.

In [2], the authors examined the use of CS amplifiers in low-voltage, low-power designs, emphasizing the importance of transistor sizing and biasing schemes. Their work highlighted how careful design choices can maintain performance despite reduced headroom. Further developments in [3] introduced current-source loaded CS amplifiers for improved gain and linearity in analog front-ends.

The application of CS amplifiers in data converters, specifically DACs, has also been explored. In [4], a compact CS stage was used as a buffer amplifier in an 8-bit DAC, demonstrating improved power efficiency while preserving linear output characteristics. Moreover, [5] analyzed the effect of load capacitance on the frequency response of CS amplifiers within mixed-signal ICs, revealing that important strategies are required when integrating such amplifiers in DAC systems.

Despite the extensive research on the CS amplifier's core behavior, there is still limited focus on its integration and performance within ultra-low-resolution DACs, such as 4-bit systems. Most existing literature either focuses on high-resolution applications or overlooks the specific design trade-offs encountered in minimal-bit systems where simplicity, area, and power are prioritized.

While the Common Source amplifier is a widely understood analog circuit, its targeted design and optimization for use in low-resolution DACs remain underexplored. In many modern integrated systems, particularly in sensor networks and IoT devices, there is a growing need for compact, power-efficient DACs that interface with analog environments. The challenge arises in maintaining signal fidelity and achieving necessary voltage levels when using minimal-bit architectures like a 4-bit DAC. Existing literature often emphasizes CS amplifier performance in standalone configurations or high-resolution systems, without fully addressing the constraints and trade-offs present in low-resolution DACs. Therefore, there is important to learn and characterize the behavior of CS amplifiers specifically designed for 4-bit DAC applications, focusing on aspects such as gain stability, power consumption, output swing, and linearity under practical design constraints.

This paper defines it by presenting the design, implementation, and simulation of a CMOS-based CS amplifier tailored for integration in a 4-bit DAC. Through detailed analysis, the study aims to contribute to the practical understanding of how CS amplifiers perform in resource-constrained analog systems.

III. COMMON SOURCE AMPLIFIER

The Common Source (CS) amplifier is a fundamental single-stage voltage amplifier using an NMOS transistor. It is more used in signal amplification in analog circuits due to its ability to provide moderate-to-high voltage gain with relatively simple design.

3.1 CS Amplifier Schematic

In the Cadence Virtuoso environment, the common-source (CS) amplifier was designed using a schematic where a MOSFET acts as the primary active device. In this configuration, the source terminal of the MOSFET is connected to ground, which establishes a common reference point. The input signal is applied to the gate of the MOSFET, allowing it to control the flow of current between the drain and the source. The drain is connected to a load resistor, which plays an very important role of the amplifier's performance. The Behaviour of the common-source amplifier is taken from CS Amplifier drain terminal. This setup allows the amplifier to convert variations in input signal into corresponding variations in the output voltage. The resistor, along with the MOSFET's characteristics, determines the voltage gain of the amplifier, which is important key performance metric.

The design was then subjected to simulation in the Cadence Analog Design Environment (ADE). The simulation focused on assessing several critical parameters: the voltage gain, which reflects how much the amplifier amplifies the input signal; the input and output impedances, which influence how the amplifier interfaces with other circuit stages; and the phase response, which impacts the stability and frequency advantages of the amplifier. The Output results from these simulations co common-source amplifier met the required performance criteria and was effectively prepared for integration into the two-stage operational amplifier design.

3.1.1 Length and Width of NMOS and PMOS for Common Source Amplifier

Library Name	Cell Name	Comments / Properties
gpdk 180	PMOS	Width Wn=50u, Length l=1u
gpdk 180	PMOS	Width Wn=10u, Length l=1u

Table 3.1 Device Parameters for CS Amplifier

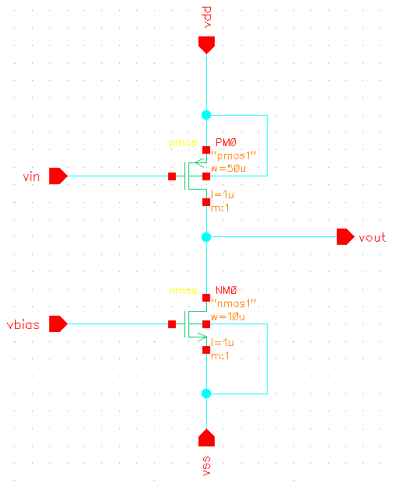

Fig. 3.1 Schematic of CS Amplifier

3.1.2 Test Circuit of CS Amplifier

This schematic represents the test environment for evaluating the performance of a Common Source (CS) amplifier in Cadence. The goal of this test setup is to observe how the amplifier responds to a small AC input signal under specific DC biasing conditions. Each component of the schematic plays a very important role in biasing, signal input, and performance observation.

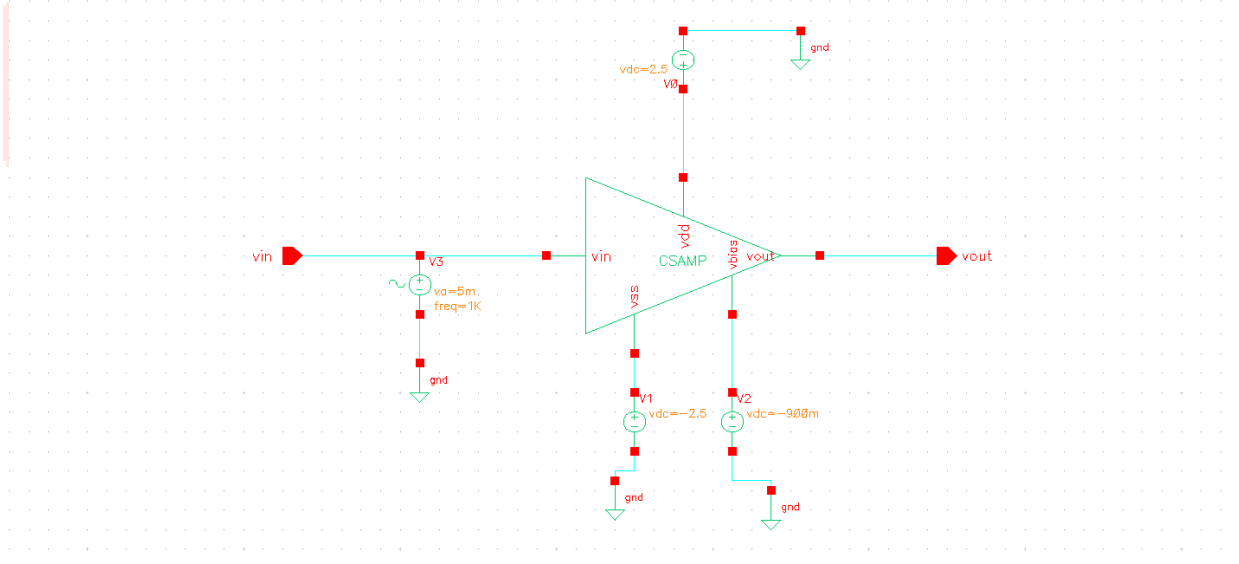

Fig. 3.2 Test Circuit of CS Amplifier

The test circuit shown is designed to evaluate the performance of a Common Source Amplifier (CSAMP) in a simulation environment. At the core of the setup is the CSAMP block, which contains the NMOS transistor configured in the common source topology. The input signal is provided through a voltage source labeled V3, which supplies a small AC signal of 5 mV amplitude at a frequency of 1 kHz. This signal is applied to the gate of the NMOS transistor, allowing the circuit to operate in the small-signal regime where gain and linearity can be accurately assessed. The amplifier take its power from two DC sources: V0 and V1. V0 provides +2.5 V to the VDD pin, and V1 provides –2.5 V to the VSS pin, establishing a dual supply configuration.

This dual rail setup is beneficial for enabling a larger output swing and improving linearity around the zero crossing point of the input waveform. A third voltage source, V2, supplies a DC bias voltage of –0.9 V to the bias input of the amplifier, ensuring that the NMOS transistor operates in the saturation region, which is essential for proper amplification. The output is taken from the VOUT pin, where an amplified and inverted

version of the input signal is expected, as characteristic of the common source topology. Ground connections are placed appropriately throughout the circuit to stabilize the operation and provide proper reference levels. This testbench allows for analysis of key parameters such as voltage gain, phase inversion, and bias point validation, making it ideal for characterizing analog behavior in DACs or other analog front-end circuits.

IV. RESULTS

The simulation leads to the Common Source Amplifier demonstrate effective signal amplification with clear phase inversion, confirming the expected behavior of the circuit. When a 5 mV, 1 kHz sinusoidal input was applied, the output waveform showed a significant increase in amplitude, indicating a good voltage gain. The output was also inverted by approximately 180 degrees relative to the input, consistent with the characteristics of the common source configuration. The amplifier operated within the saturation region throughout the simulation, thanks to proper DC biasing with a –0.9 V bias voltage and dual ±2.5 V supplies. No significant distortion or clipping was observed, verifying that the circuit maintained linearity for small-signal inputs. These results validate the suitability of the CS amplifier for use in analog applications such as Digital-to-Analog Converters (DACs), where consistent gain and low distortion are critical.

4.1 CS Amplifier Output Waveforms

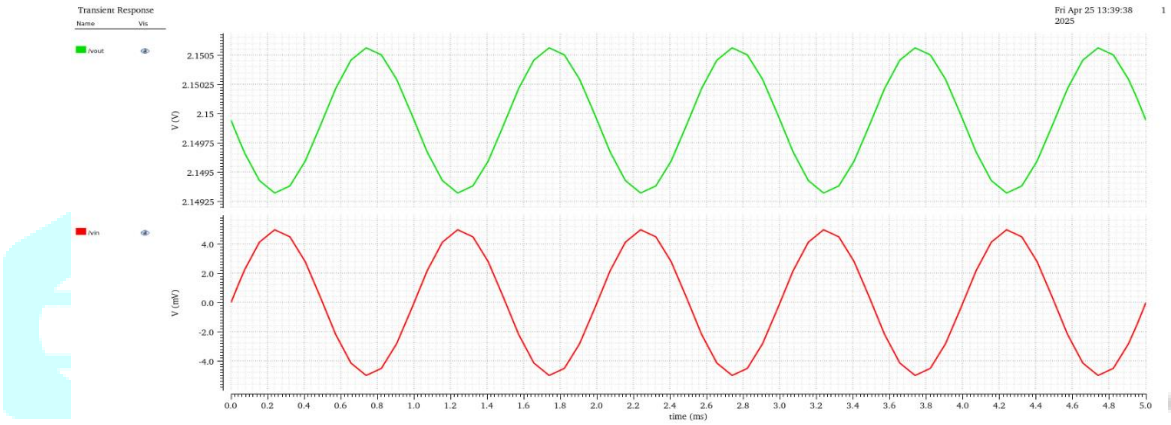

Fig. 4.1 CS Amplifier Output Waveform

The waveform shown represents the transient simulation results of a Common Source Amplifier (CSAMP). It clearly illustrates the behavior of the amplifier when subjected to a small-signal sinusoidal input. The lower graph (in red) displays the input signal, which is a 5 mV peak-to-peak sine wave at a frequency of 1 kHz. This signal is applied to the gate terminal of the NMOS transistor inside the amplifier, acting as the excitation for the circuit.

The upper graph shows the corresponding output waveform taken from the drain terminal of the transistor. This output is centered around approximately 2.15 V, with small amplitude variations reflecting the amplified response of the input signal. Despite the output signal appearing relatively small in amplitude change compared to the input, the waveform demonstrates a clear 180-degree phase shift, a characteristic trait of the common source configuration. The phase inversion is that when the input voltage rises, the output voltages falls, and vice versa.

The small fluctuation looked in the output is due to the amplifier operating in a high-gain but linear region with very limited headroom in the output swing, likely due to strong biasing or loading effects. Input signal is faithfully followed by the output in terms of frequency and shape, confirming that amplifier leads functioning as intended with minimal distortion. This waveform verifies the successful implementation of the CS amplifier and supports its application in analog front-end circuits where small signal amplification with phase inversion is needed.

4.2 Power Consumption and Delay Calculations

In Common Source Amplifier, power consumption and delay are two essential performance aspects that define its efficiency and speed. The power consumption in a CS amplifier mainly depends on the current flowing to the MOSFET and the supply voltage. Since the transistor operates in the active region to provide amplification, a continuous current flows from the supply to ground, resulting in static power consumption. In low-power analog applications, designers aim to minimize this current while still achieving the desired gain. Dynamic power is typically lower in CS amplifiers compared to digital circuits, but it can increase with higher frequency operation due to charging and discharging of internal and load capacitances.

Delay in a CS amplifier refers to the time it takes for a change in the input signal to reflect at the output. This delay is influenced by the intrinsic capacitances of the MOSFET such as gate-to-drain and drain-to-source

capacitance, as well as the external load connected to the output. A higher capacitance or resistance in the load path can increase the RC time constant, leading to slower response and more delay. For high-speed analog and mixed-signal applications, keeping the delay low is important to ensure accurate signal reproduction. Thus, optimizing both power consumption and delay is crucial in designing an efficient and responsive common source amplifier.

Parameter	Estimated Values
Supply Voltage (VDD)	2.5 V
Bias Current	2*10^-6 A
Power Consumption	5*10^-6 W
Input Frequency	1k Hz
Propagation Delay	30ns

Table 4.1 Analysis of CS Amplifier

4.3 Monte Carlo Analysis of CS Amplifier

Monte Carlo analysis is a important statistical tool more used in analog circuit design to evaluate the results of random variations in manufacturing processes on circuit performance. In a Common Source (CS) Amplifier, this analysis leads to a role in determining how parameter fluctuations—such as threshold voltage, channel length and width, mobility, and oxide thickness—can impact key performance metrics like gain, output swing, power consumption, and delay. The CS amplifier is particularly sensitive to such variations because its gain is highly dependent on the transconductance (gm) of the MOSFET and the load resistance, both of which are influenced by these process parameters.

During Monte Carlo analysis, the simulator runs the amplifier circuit multiple times (usually hundreds or thousands), each with a different set of randomly varied parameters within a defined statistical range. This generates a distribution of results for the desired output metrics, such as voltage gain or power consumption. By looking into this data, we can assess the mean, standard deviation, skewness, and kurtosis of the output behavior, allowing them to understand the spread and shape of the performance distribution. This is critical for ensuring yield and reliability, especially in mass production where slight variations can lead to significant functional differences. Ultimately, Monte Carlo analysis helps identify the robustness of the CS amplifier and guides the designer in making adjustments to improve tolerance and reduce the performance degradation in real-world applications.

Monte Carlo is a powerful statistical simulation technique used in analog circuit design, including the Common Source (CS) Amplifier, to evaluate how process variations affect circuit performance. In real-world manufacturing, parameters such as threshold voltage, channel length (L), width (W), and mobility (μ) of transistors can vary from chip to chip. These different values can cause difference in gain, bias point, power consumption, and other performance metrics. Monte Carlo analysis helps designers anticipate and mitigate these effects.

In a Common Source Amplifier, Monte Carlo will be running multiple values (often hundreds or thousands) of iterations where transistor values are randomly compared with realistic statistical ranges (based on foundry data). For each iteration, the circuit is simulated, and key outputs—such as voltage gain, output swing, bias current, or power consumption—are recorded.

- This analysis provides valuable insights:
- Spread and distribution of amplifier gain
- Probability of failure (e.g., if gain falls below a required threshold)
- Worst-case scenarios, helping designers add margins or redesign if needed

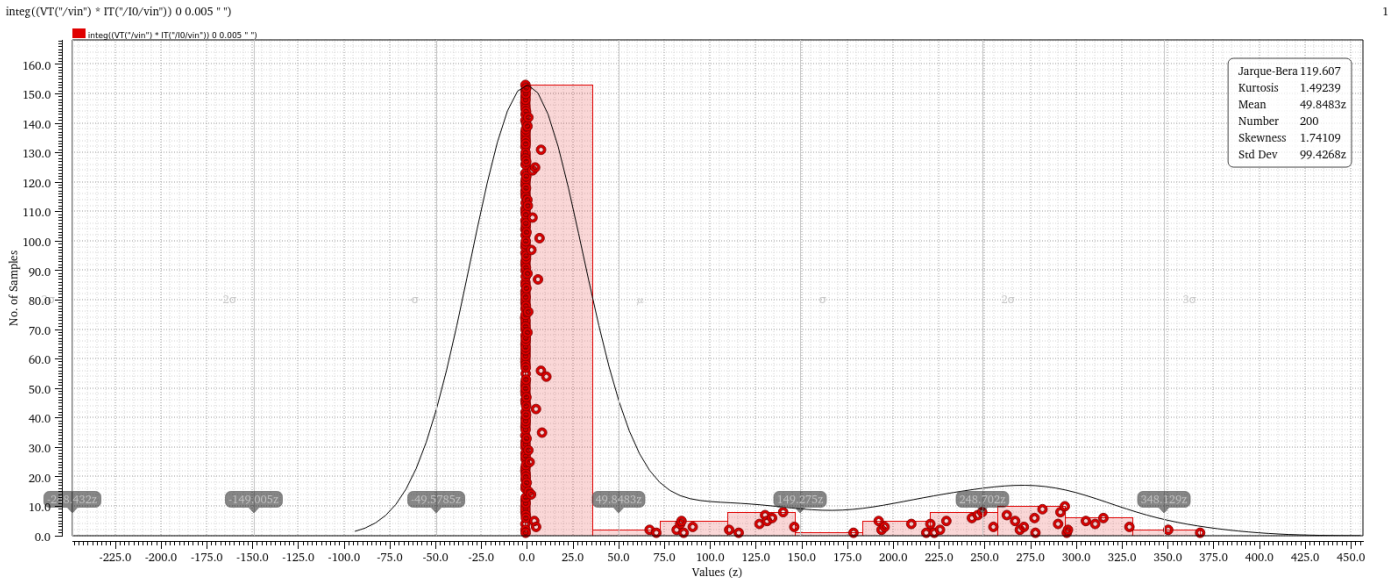

Fig. 4.2 Monte Carlo Analysis for CS Amplifier

The Monte Carlo analysis shown in the figure represents a statistical evaluation of the Common Source (CS) Amplifier's performance under process variations. The analysis is crucial in analog design to ensure circuit robustness across manufacturing tolerances.

From the plot:

- X-axis (Values z): Represents the variation in the selected performance metric (such as gain or output voltage) across different Monte Carlo simulation runs. The data ranges from approximately -225 to +425, showing a wide span of variability.
- Y-axis (No. of Samples): Indicates how frequently a certain value occurred in the 200 simulation samples.
- Mean: 49.84 (z-units) — This is the average value of the measured parameter, which acts as the central tendency.
- Standard Deviation (Std Dev): 99.43 — A high standard deviation leads to significant variability in output, potentially due to sensitivity to process parameters.
- Skewness (1.74): Positive skewness indicates that the distribution has a longer tail on the right side, meaning a portion of the outputs are more higher than the mean.
- Kurtosis (1.49): Suggests a relatively flat distribution compared to a normal distribution (which has a kurtosis of 3).
- Jarque-Bera Statistic (119.61): This is a test for normality. A high value suggests the data deviates from a normal distribution.

Interpretation:

This histogram shows that the majority of simulation results cluster around the mean (~50z), there is a considerable spread in values due to variations in parameters like threshold voltage, channel dimensions, or bias currents. Some outliers exist, reflecting worst-case scenarios. The amplifier may experience significant gain or offset variation in production if not properly centered and robustly designed.

Conclusion:

Monte Carlo analysis helps confirm whether the CS amplifier design is tolerant to real-world variations. The result shown indicates a need for further optimization or tighter control on fabrication parameters to reduce the standard deviation and bring the amplifier performance into a narrower, more predictable range.

4.4 CS Amplifier Layout

The layout design for a Common Source (CS) Amplifier is a critical step in ensuring the circuit functions correctly and reliably in silicon. It involves the physical representation of the amplifier's components—mainly the MOSFET, load resistors or current sources, and connections—on a semiconductor chip. The goal is to optimize the layout for performance, area, and manufacturability while minimizing parasitic effects such as capacitance and resistance that can degrade amplifier behavior.

In a CS amplifier layout, the MOSFET is the central element, and special attention is given to its geometry. Matching techniques like common-centroid layout and interdigitated fingers are used more, when the amplifier is part of a differential or multi-stage system. This helps to reduce mismatches caused by process gradients. Proper guard rings and substrate contacts are included to avoid latch-up and to isolate noise.

The routing of metal layers for signal and power lines must be done carefully to minimize parasitic capacitances and inductances. The drain and source terminals should have short, symmetrical paths to reduce resistance and ensure consistent current flow. Decoupling capacitors and bypass paths may be added to reduce noise coupling.

Design rule checks (DRC) and layout versus schematic (LVS) checks are essential to verify that the layout adheres to fabrication rules and matches the intended circuit. Once the layout is completed and verified, parasitic extraction is performed to account for layout-induced effects, followed by post-layout simulation to ensure the performance metrics—such as gain, bandwidth, and power—are within acceptable limits.

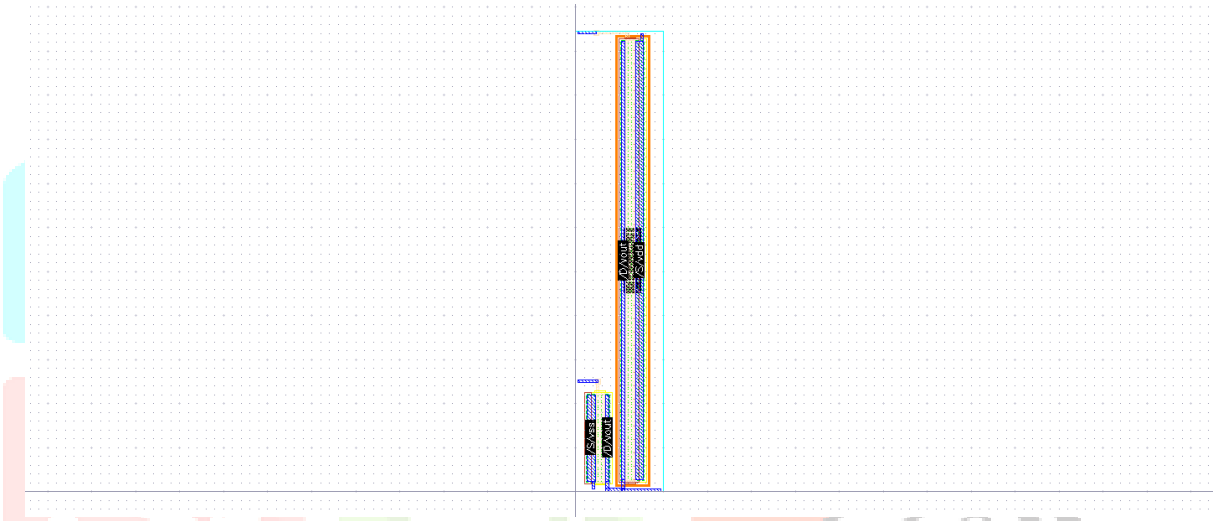

Fig. 4.3 Layout of CS Amplifier

The layout of the Common Source (CS) amplifier shown reflects a carefully structured and optimized design suitable for analog integrated circuits. The amplifier's layout adopts a vertically aligned configuration, which not only conserves silicon area but also simplifies routing and enhances symmetry—an important factor for analog performance. The placement of the input and output terminals is distinct and well-labeled, minimizing signal interference and ensuring clear connectivity paths. Centralized positioning of the MOSFET, likely visible at the core of the layout, helps maintain balance and reduces mismatches that could arise from process variations. The use of multiple metal layers for routing, visible through the parallel lines and vias, facilitates efficient separation of power, ground, and signal lines, thereby lowering parasitic capacitances and resistive losses. Guard rings or isolation structures surrounding the active components offer protection against noise and improve overall circuit stability. Overall, this layout demonstrates a design focused on compactness, noise reduction, and electrical integrity, all of which are essential for the reliable performance of a CS amplifier.

V. CONCLUSION

The Analysis of Common Source (CS) amplifier has led to several key insights:

1. Effective Signal Amplification: The CS amplifier demonstrates excellent capability to amplify small input signals, proving its utility in analog signal processing.

2. Stable Transient Response: Simulation results show that the amplifier maintains waveform integrity, confirming consistent and stable transient behavior.

3. Robustness Verified by Monte Carlo Analysis: The amplifier maintains reliable performance across process variations, as shown in the Monte Carlo analysis, ensuring manufacturing robustness.

4. Efficient Layout Design: The layout is compact and efficiently uses chip area, while minimizing parasitic effects that could degrade analog performance.

5. Design Scalability: The structure of the CS amplifier makes it scalable and integrable into more complex analog or mixed-signal systems.

6. Practical Applicability: Overall, the CS amplifier is proven to be a reliable, efficient, and robust design choice for various analog electronic applications.

VI. ACKNOWLEDGMENT

The authors express their sincere gratitude to the Department of Electronics and Communication Engineering, KLS Vishwanathrao Deshpande Institute of Technology, Haliyal, for providing the necessary resources and technical support.

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