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Design And Analysis Of Reversible Multiplier Circuit Using Reversible Gates

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Abstract: The advancement of low-power and quantum computing, traditional irreversible logic circuits face challenges due to energy loss from information erasure, as described by Landauer's principle. Reversible logic addresses this by ensuring bijective input-output mapping, enabling minimal energy dissipation. This paper proposes an optimized low-cost 4×4 reversible multiplier using Peres, Feynman, and TR gates. The design reduces quantum cost, garbage outputs, constant inputs, and gate count, improving computational and energy efficiency. Simulation results validate its performance over existing designs, making it suitable for energy-constrained and quantum applications.

***Keywords*:** Reversible Logic, Low Power Design, Quantum Computing, 4×4 Multiplier, Fredkin Gate, TSG Gate, Garbage Outputs, Quantum Cost, Constant Inputs, Energy-Efficient Circuits, Digital Signal Processing

I. INTRODUCTION

In recent years, the demand for energy-efficient and high-performance computing has intensified, particularly with the advancement of nanoscale technologies and quantum computing. Traditional irreversible logic circuits, which dominate current digital systems, suffer from inherent energy dissipation due to information loss, as described by Landauer's principle. According to this principle, the erasure of each bit of information results in a minimum energy loss of kTln2, making conventional designs less suitable for low-power applications.Reversible logic has emerged as a compelling alternative, offering lossless computation by establishing a one-to-one correspondence between input and output vectors. This not only reduces energy dissipation but also aligns with the operational requirements of quantum computing, where reversibility is fundamental. As a result, reversible logic circuits are being actively explored for applications in low-power VLSI, quantum systems, and portable embedded devices.Among arithmetic operations, multiplication is one of the most critical and power-intensive functions, widely used in digital signal processing (DSP), image processing, and cryptography. Optimizing multipliers using reversible logic can significantly enhance energy efficiency.

II. LITERATURE SURVEY

1. **Design and Analysis of Reversible Multiplier Circuit Using Reversible Gates (Khan et al.)**

   Aim: To develop a reversible multiplier circuit that reduces energy consumption and optimizes hardware resources.

   Approach: The authors used Toffoli and Fredkin gates to design a 4×4 reversible multiplier and evaluated its performance in terms of gate count and garbage outputs.

   Key Findings: The design improved energy efficiency but generated a relatively high number of garbage outputs, highlighting the need for further optimization in reversible circuit design.

2. **Efficient Design of a Reversible Multiplier Using HNG and Peres Gates (Singh et al.)**

   Aim: To propose a multiplier architecture with minimized quantum cost and fewer constant inputs.

   Approach: The multiplier was constructed using HNG and Peres gates, with a focus on optimizing partial product generation and addition stages.

   Key Findings: The design achieved reduced quantum cost and gate count compared to conventional reversible multipliers but still involved a moderate number of garbage outputs.

3. **Low Power Reversible Multiplier Using Novel Gate Combinations (Reddy et al.)**

   Aim: To design a low-power reversible multiplier suitable for quantum and nanoscale systems.

   Approach: The circuit used a combination of existing and custom-designed reversible gates to implement a 4×4 multiplier and was simulated to validate performance.

   Key Findings: The design showed improved power savings and area efficiency, but further improvements in constant input minimization were needed.

4. **A Novel Reversible Multiplier Using TR, Peres, and Feynman Gates (Sharma et al.)**

   Aim: To develop an optimized reversible multiplier with minimal garbage outputs and quantum cost.

   Approach: The authors implemented a hybrid reversible gate-based architecture using TR, Peres, and Feynman gates for partial product generation and addition.

   Key Findings: The proposed multiplier demonstrated significant improvements in gate count and garbage output reduction, making it well-suited for low-power and quantum applications.

III. PRELIMINARIES

Quantum Cost: Represents the number of basic quantum gates (NOT, CNOT, Controlled-V, Controlled-V^+) required to implement a reversible gate.

Constant Inputs: Inputs fixed to logic 0 or 1 to preserve reversibility. Fewer constants indicate a more optimized design.

Garbage Outputs: Unused outputs needed to maintain a one-to-one input-output mapping. Minimizing these improves circuit efficiency.

Hardware Complexity: Defined by the total number of logic operations, including XOR, AND, and NOT gates.

Delay: The time taken for an input change to affect the output. Lower delay ensures faster circuit operation.

IV. BASIC REVERSIBLE LOGIC GATE

4.1 NOT GATE

The NOT gate is a fundamental 1x1 reversible logic gate that inverts its single input. It takes a single input bit and produces one output bit, where the output is the logical complement of the input. Since there is a one-to-one mapping between input and output, the NOT gate is inherently reversible. It has a quantum cost of 1, as it is considered a basic building block in quantum and reversible circuit design. The NOT gate is widely used in the synthesis of complex reversible circuits due to its simplicity and essential role in logic inversion.

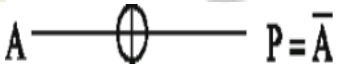

Fig.4.1 Not Gate

4.2 The Controlled -V And Controlled -V + Gates.

The Controlled-V gate is a 2x2 reversible gate that performs a square-root-of-NOT operation on the target bit only if the control bit is 1. It is one of the primitive quantum gates used in constructing more complex reversible circuits. Its quantum cost is taken as 1. This gate plays a crucial role in minimizing the overall quantum cost of logic designs. The Controlled-V^+ gate is also a 2x2 reversible gate and is the Hermitian (inverse) of the Controlled-V gate. It performs the inverse of the square root of NOT operation on the target bit when the control bit is 1. Like the Controlled-V gate, its quantum cost is 1. It is used to ensure reversibility and unitarity in quantum logic circuits.

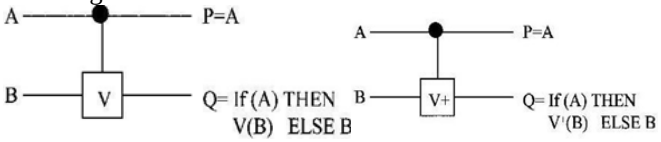

Fig.4.2 Controlled -V Gate & Controlled -V+ Gate

4.3 The Toffoli Gate

The Toffoli gate is a 3x3 reversible gate with two control inputs and one target input. It passes the first two inputs unchanged and flips the third input if both control inputs are 1. This gate is universal for classical reversible computation. Its quantum cost is 5 when implemented using a basic quantum gate.

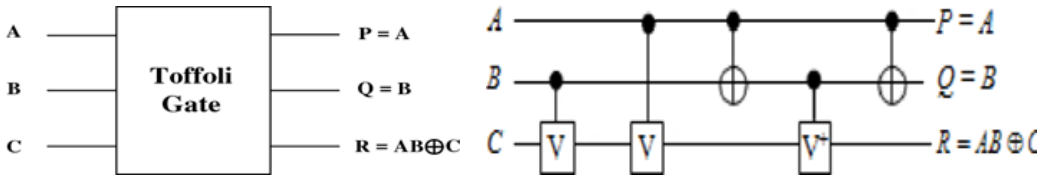

Fig.4.3 .Symbol of Toffoli gate & Quantum representation of Toffoli gate.

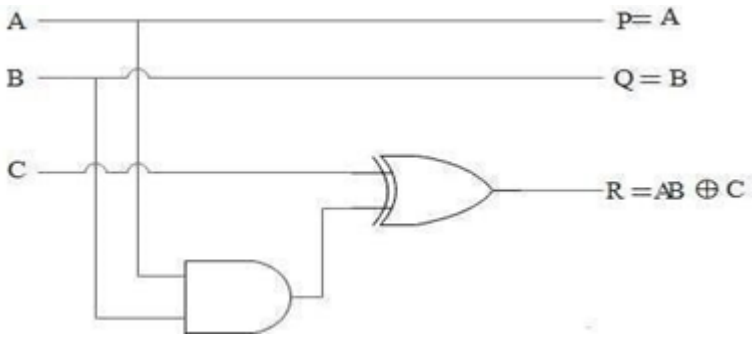

Fig 4.4 Circuit Diagram Of Toffoli Gate

4.4 Fredkin gate

The Fredkin gate is a 3×3 reversible logic gate commonly used in reversible and quantum circuit design. It takes three inputs: X, Y, and Z, and produces three outputs: P = X, Q = X′Y ⊕XZ, and R = X′Z ⊕XY. The gate performs a controlled swap operation—if X = 0, Y and Z remain unchanged; if X = 1, Y and Z are swapped. This characteristic makes it suitable for implementing conditional logic without losing information. The Fredkin gate has a quantum cost of 5 and is valued for its reversibility and conservative logic properties in low-power applications.

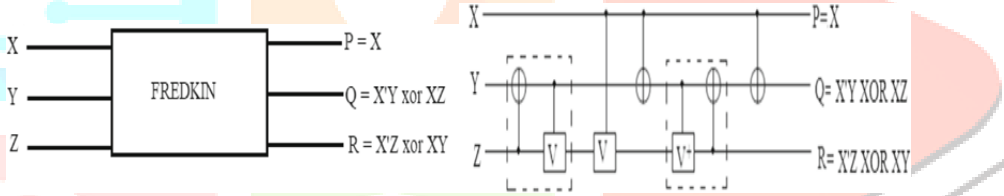

Fig. 4.5.Symbol of Fredkin gate & Quantum representation of Fredkin gate.

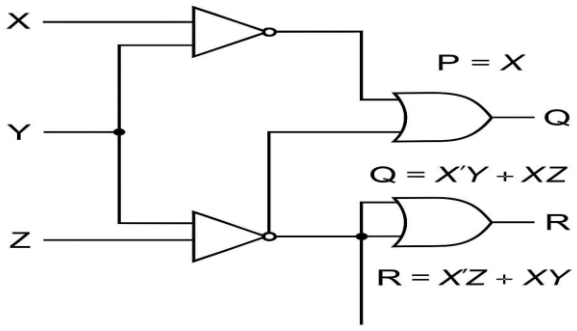

Fig 4.5 Circuit Diagram Of Fredkin Gate

4.5 TSG Gate

The TSG (Thapliyal–Srinivas Gate) is a 4x4 reversible gate designed to implement full adder logic within a single gate. It reduces garbage outputs and quantum cost when compared to using multiple gates for a full adder. The TSG gate is efficient for arithmetic circuit design. It is often used in reversible ALU and multiplier circuits.

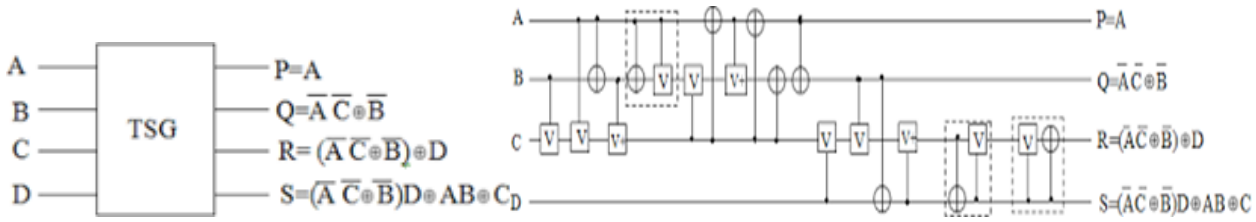

Fig. 4.6.Symbol of TSG gate & Quantum representation of TSG gate.

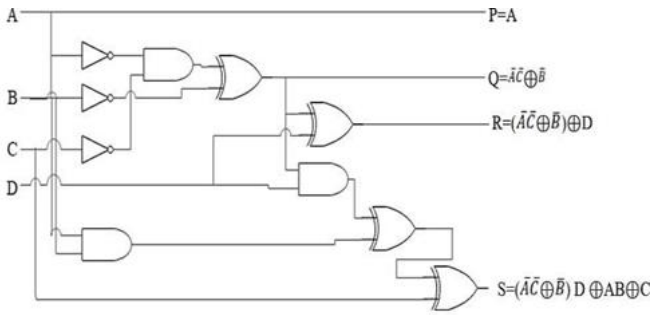

Fig 4.4 Circuit Diagram Of TSG Gate

V. Design Of Reversible Multiplier

The architecture of the proposed 4×4 reversible multiplier is developed with a strong emphasis on minimizing computational overhead while ensuring full reversibility. The design strategy is partitioned into two principal stages: Partial Product Generation (PPG) and Multi-Operand Addition (MOA). This modular approach not only simplifies the implementation but also helps in reducing overall hardware complexity, garbage outputs, and quantum cost.

Fig.5.1Symbol of PPG gate & Operation of 4X4 Multiplier

A. Partial Product Generation

In the first stage, partial products are computed by employing **Partial Product Generator (PPG) gates**, which are specifically designed to function efficiently under reversible logic constraints. Each PPG gate takes four inputs and produces four outputs, with two outputs directly replicating inputs and the other two representing logic product terms modulated by an auxiliary constant input. The PPG gate behaves correctly only when the constant input CCC is set to 0, ensuring the reversibility of the operation.

The input vector for the PPG is I=(A,B,C,D)I = (A, B, C, D)I=(A,B,C,D), while the output vector is O=(P,Q,R,S)O = (P, Q, R, S)O=(P,Q,R,S), where:

- P=AP = AP=A
- Q=BQ = BQ=B
- R=A· B⊕CR = A \cdot B \oplus CR=A· B⊕C
- S=A· D⊕CS = A \cdot D \oplus CS=A· D⊕C

This configuration ensures that logical operations are performed without any loss of information. To generate the full 4x4 partial product matrix, a total of **8 PPG gates** are used, requiring **8 constant inputs** and resulting in **4 garbage outputs**. The quantum cost for each PPG gate is **7**, yielding a total gate-level cost of **56**, not including overhead for wiring or synchronization.

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	0
0	1	1	0	0	1	1	1
0	1	1	1	0	1	1	1
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	1
1	0	1	0	1	0	1	1
1	0	1	1	1	0	1	0
1	1	0	0	1	1	1	0
1	1	0	1	1	1	1	1
1	1	1	0	1	1	0	1
1	1	1	1	1	1	0	0

Table 5.1 Truth Table of PPG Gate

B. PARTIAL PRODUCT GENERATOR CIRCUIT:

The optimized partial product generation is common in both designs. The product terms are generated using 8 PPG gates with 8 constant inputs as shown in fig.13. The product terms are then used as inputs to the multi operand addition circuit. For partial product generation a total of 8 reversible gates with 8 constant inputs are used which produces 4 garbage outputs. The total cost of each PPG block is 62.

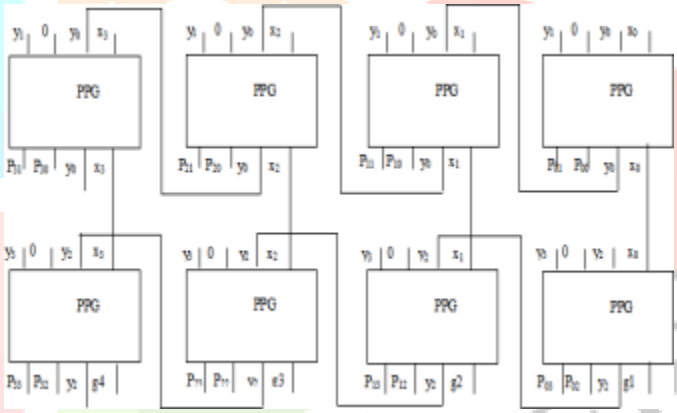

Fig.5.2 Optimized Partial Product Generation using PPG Gates

C. The 4x4 Reversable Multiplier Circuit:

A 4x4 reversible multiplier circuit performs the multiplication of two 4-bit binary numbers using reversible logic gates, ensuring no information loss. It is designed using combinations of reversible gates like TSG and Fredkin gates to optimize parameters such as quantum cost, garbage outputs, and constant inputs. The circuit generates an 8-bit product while maintaining reversibility throughout the computation. Such designs are crucial for low-power and quantum computing applications where energy efficiency and reversibility are essential.

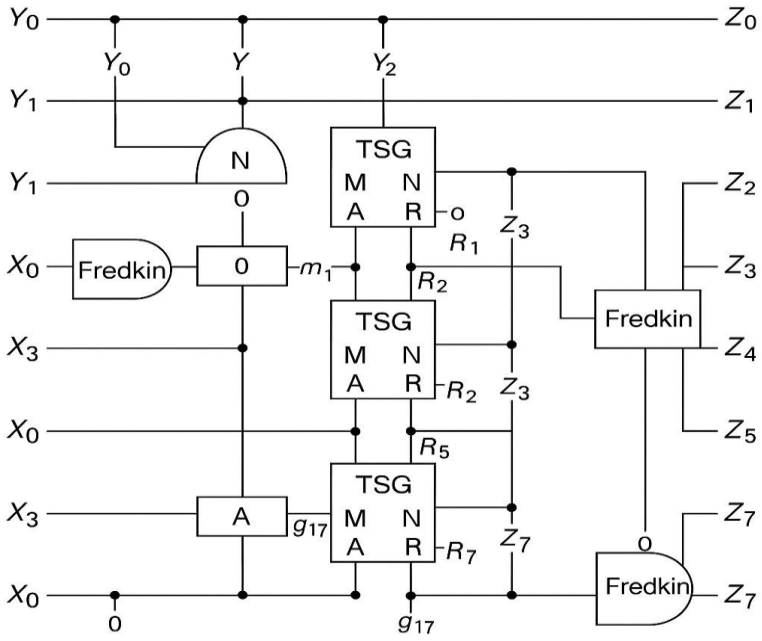

Fig 5.3 The 4x4 reversible multiplier circuit using TSG gate and Fredkin gate

VI. RESULT

The proposed 4x4 reversible multiplier circuit is designed in verilog coding by EDA Playground software.The proposed reversible multiplier circuit is more efficient than the existing multiplier using HNG and PG gates.For a meaningful comparison, TABLE II lists the characteristics of several reversible logic gates. In TABLE III, we compare the existing reversible multiplier circuit with our proposed design, focusing on key factors such as garbage outputs, constant inputs, quantum cost, and delay.

Phase	Inputs	Operation / Gate Used	Output
1	$X_0 \cdot Y_0$	Direct product	$Z_0 = X_0 \cdot Y_0$
2	$X_1 \cdot Y_0$, $X_0 \cdot Y_1$	Half Adder (Fredkin Gate)	$Z_1 = X_1 \cdot Y_0 + X_0 \cdot Y_1$
3	$X_2 \cdot Y_0$, $X_0 \cdot Y_2$, carry from HA	Full Adder 1 (TSG Gate)	
4	$X_2 \cdot Y_0 + X_0 \cdot Y_2$, $X_1 \cdot Y_1$, carry	Full Adder 2 (TSG Gate)	$Z_2 = X_2 \cdot Y_0 + X_0 \cdot Y_2 + X_1 \cdot Y_1$
5	$X_3 \cdot Y_0$, $X_0 \cdot Y_3$, carry	Full Adder 3 (TSG Gate)	
6	$X_3 \cdot Y_0 + X_0 \cdot Y_3$, carry	Full Adder 4 (TSG Gate)	
7	$X_1 \cdot Y_2$, $X_2 \cdot Y_1$, $X_3 \cdot Y_0 + X_0 \cdot Y_3$	Full Adder 5 (TSG Gate)	$Z_3 = X_1 \cdot Y_2 + X_2 \cdot Y_1 + X_3 \cdot Y_0$
8	$X_1 \cdot Y_3$, $X_3 \cdot Y_1$, carry	Full Adder 6 (TSG Gate)	
9	$X_1 \cdot Y_3 + X_3 \cdot Y_1$, $X_2 \cdot Y_2$, carry	Full Adder 7 (TSG Gate)	$Z_4 = X_1 \cdot Y_3 + X_3 \cdot Y_1 + X_2 \cdot Y_2$
10	$X_3 \cdot Y_2$, $X_2 \cdot Y_3$, carry	Full Adder 8 (TSG Gate)	$Z_5 = X_3 \cdot Y_2 + X_2 \cdot Y_3$
11	$X_3 \cdot Y_3$, carry	Half Adder (Fredkin Gate)	$Z_6 = X_3 \cdot Y_3$ + Carry, Z_7 = Carry

Table.6.1.Truth Table Final output generation of the proposed reversible 4 × 4 multiplier circuit.

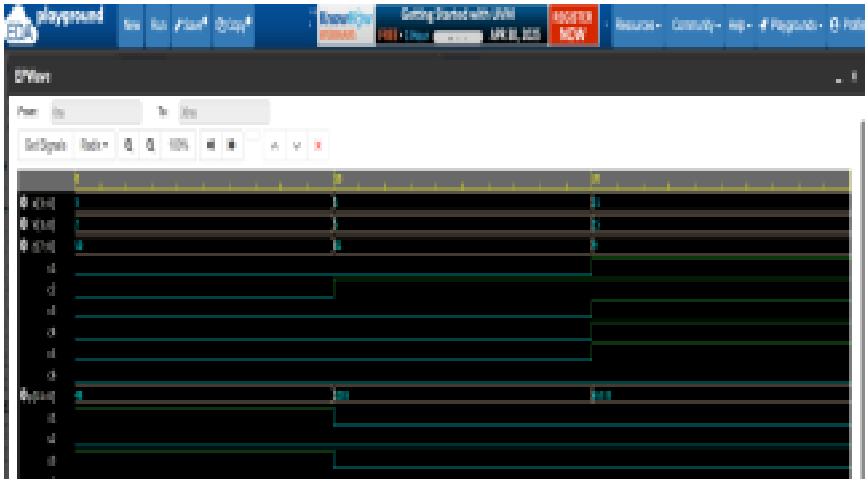

Fig 6.1:Simulation waveform generated for our proposed 4x4 reversible multiplier circuit

REVERSIBLE GATES	NO. OF INPUTS	NO. OF OUTPUTS	QUANTUM COST	DELAY (ns)
Peres gate(PG)	3	3	4	5.385
Fredkin gate(FRG)	3	3	5	5.456
TSG gate	4	4	17	5.473
Toffoli gate(TG)	3	3	5	5.776

TABLE I: Comparison of Reversible gates

Parameters	Reversible multiplier circuit using PG and HNG gate	Proposed reversible multiplier circuit using TSG and FRG gate
No. of constant Inputs	9	4
No. of Garbage Outputs	52	30
Total Quantum cost	120	83
Delay(ns)	8.051	3.953

TABLE II: Comparative experimental results of different reversible multiplier circuits

VII. FUTURE WORK

The current design effectively demonstrates the viability of using reversible logic for low-power and quantum-friendly multiplication circuits. Building on this foundation, future work can further explore and optimize the architecture by leveraging the unique properties of TSG and Fredkin gates. These gates offer promising trade-offs in terms of quantum cost, garbage output, and gate count, which can be harnessed for greater efficiency in scalable arithmetic designs.

One potential direction involves using **TSG gates more extensively as full adders** within the multi-operand addition stage. Given the TSG gate's ability to perform full addition with minimal garbage and a compact structure, its use can reduce the number of required gate levels and intermediate outputs. This can be particularly advantageous in larger multipliers such as 8×8 or 16×16, where cumulative complexity becomes more critical.

In parallel, **Fredkin gates**—known for their conservative logic properties and ability to perform conditional swaps—can be utilized in partial product alignment and carry propagation stages. Their reversible nature allows them to manage bit rearrangements without introducing extra garbage, thus supporting more structured and predictable multiplier designs.

Further optimization could involve the **hybrid integration of TSG and Fredkin gates** with existing reversible gate architectures (such as HNG or Peres) to form customized logic blocks tailored for specific functions within the multiplier. Design automation using evolutionary algorithms or AI-driven synthesis tools may also be employed to explore these hybrid designs for optimal results.

Additionally, the proposed gate-level optimizations should be validated using practical platforms such as **quantum-dot cellular automata (QCA)** or **CMOS-based reversible logic**. Finally, extending the multiplier's utility into complex reversible ALUs and integrating fault tolerance mechanisms will be crucial for advancing its real-world applicability in quantum computing, secure cryptographic systems, and energy-constrained embedded platforms.

VIII. Conclusion

This report presented an optimized low- cost 4x4 multiplier using reversible logic gates. By leveraging advanced reversible gates and optimizing the circuit design, the proposed multiplier achieves substantial improvements in power efficiency, gate count, and circuit complexity. Future work will explore extending the design to larger multipliers and applying these techniques to other arithmetic circuits. Additionally, the integration of reversible logic into emerging technologies such as quantum computing holds significant potential for further energy-efficient innovations.

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