IJCRT.ORG ISSN : 2320-2882

INTERNATIONAL JOURNAL OF CREATIVE RESEARCH THOUGHTS (IJCRT)
An International Open Access, Peer-reviewed, Refereed Journal

Design, Simulation & Comparative Analysis Of Current Mirrors Across Various Technologies In Cadence

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Abstract: Current mirrors are fundamental circuit components in analog and mixed-signal circuits, playing a crucial role in biasing, signal amplification, and active loads. The efficiency of a current mirror is determined by parameters such as output resistance, compliance voltage, power dissipation, and current accuracy. This paper presents a comprehensive study on the design, simulation, and comparative analysis of different current mirror configurations, including simple, Wilson, cascode, and regulated cascode current mirrors. The study evaluates the impact of various semiconductor technologies (180nm, 45nm, and beyond) on these topologies. Simulations are conducted using industry-standard tools like Cadence Virtuoso and HSPICE to compare each design's efficiency, reliability, and power performance. The findings provide in-depth insights into selecting the most suitable current mirror topology for VLSI, RF, and low-power analog design applications.

Key Words - Current Mirror, Wilson Current Mirror, Cascode, Analog Design, VLSI, Simulation, CMOS Technology.

I. INTRODUCTION

Current mirrors play a crucial role in providing stable and accurate current sources. These circuits are widely used in applications such as operational amplifiers, voltage references, differential amplifiers, and active loads. The primary function of a current mirror is to replicate a reference current while maintaining consistency across variations in voltage and process conditions. By ensuring accurate current replication, current mirrors help in achieving better gain, stability, and performance in analog circuits.

The working principle of a current mirror is based on matching transistor characteristics, ensuring that two or more transistors operate under the same conditions to mirror the reference current accurately. However, basic current mirrors suffer from limitations like channel-length modulation, low output resistance, and voltage-dependent current variations. To address these issues, advanced current mirror topologies such as the Wilson Current Mirror and Cascode Current Mirror have been introduced. These improved designs enhance accuracy, output resistance, and current stability, making them suitable for high-precision and high-frequency applications.

II. CURRENT MIRROR TOPOLOGIES

This section describes the three topologies of current mirrors studied in this work, including their main characteristics and their behavior.

2.1 Simple Current Mirror

The simplest form of a current mirror consists of two identical transistors, typically either MOSFETs or BJTs, arranged in such a way that one transistor sets a reference current while the other copies, or "mirrors," that current. The concept relies on the principle that if two transistors are perfectly matched and subjected to the same gate-to-source (for MOSFETs) or base-to-emitter (for BJTs) voltage, they will conduct equal currents, provided they operate in the same region of operation—saturation for MOSFETs or active region for BJTs. In a basic configuration, the gate and drain of the reference transistor are connected together to ensure it operates in saturation and sets up a stable current. This voltage is then applied to the gate of the second transistor, causing it to conduct a current ideally equal to the reference.

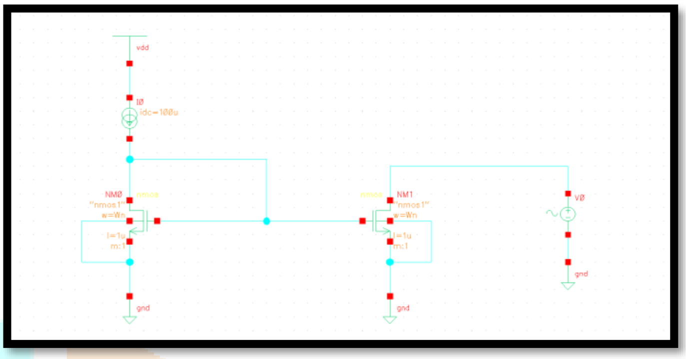


Figure 2.1- Basic Current Mirror

2.2 Wilson Current Mirror

The Wilson Current Mirror, introduced by George Wilson, improves upon the basic current mirror by incorporating negative feedback to enhance accuracy and output resistance. This design consists of three transistors, where the additional feedback mechanism helps in reducing the effect of early voltage (for BJTs) or channel-length modulation (for MOSFETs). This configuration significantly enhances current matching and stability, making it ideal for high-precision analog circuits, but comes at the cost of increased circuit complexity. Thus, the Wilson configuration offers comparable accuracy with slightly reduced headroom requirements, making it advantageous in moderate-voltage applications. Nevertheless, the circuit's feedback action introduces dynamic effects that may need to be considered in high-speed or high-frequency environments.

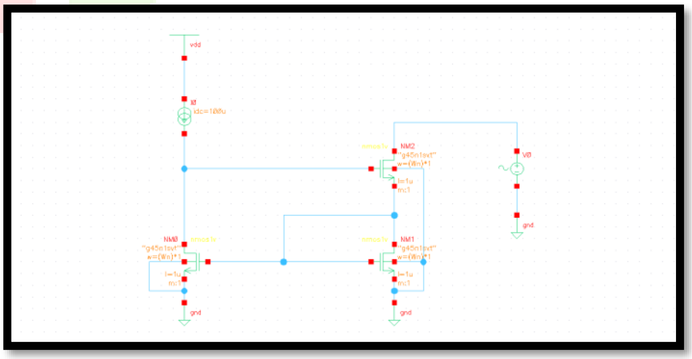


Figure 2.2 – Wilson Current Mirror

2.3 Cascode Current Mirror

To overcome the basic current mirror's limited output resistance and voltage dependency, the cascode current mirror adds a transistor (M3) to the output branch. This cascode device maintains a stable drain-source voltage across the mirroring transistor (M2), significantly increasing output resistance and improving current accuracy. The configuration offers superior output impedance, making it ideal for high-gain analog blocks and precision biasing. While it enhances current regulation and reduces channel length modulation effects, it requires higher voltage headroom, which can be a drawback in low-voltage designs.

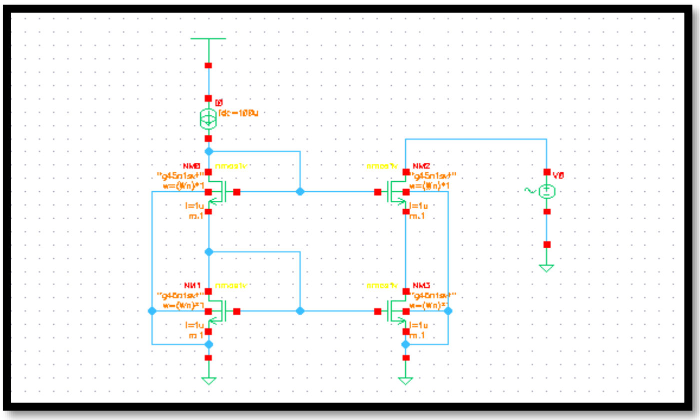


Figure 2.3 Cascode Current Mirror

III. COMPREHENSIVE CIRCUIT EVALUATION

To rigorously evaluate the performance of different current mirror architectures, we conducted an extensive simulation-based analysis encompassing DC, AC, and PVT (Process, Voltage, Temperature) evaluations for three distinct current mirror topologies: Basic, Wilson, and Cascode. Each topology was implemented and simulated within the Cadence Virtuoso environment, and tested under varying conditions:

- **Technology Nodes**: 180nm and 45nm
- **Temperature Ranges**: -30°C to 125°C, with room temperature at 27°C

The following analysis types were employed to assess the performance:

- **DC Analysis**: This analysis focuses on the output current characteristics, output resistance, and current mirroring accuracy, providing insight into each topology's fundamental performance metrics.
- **AC Analysis**: To evaluate the frequency response, gain, and bandwidth behaviour, ensuring the topologies meet the necessary dynamic performance standards.
- **PVT Analysis**: To simulate real-world operational conditions, including variations in process, supply voltage, and temperature, and assess the impact of these factors on circuit stability and performance.

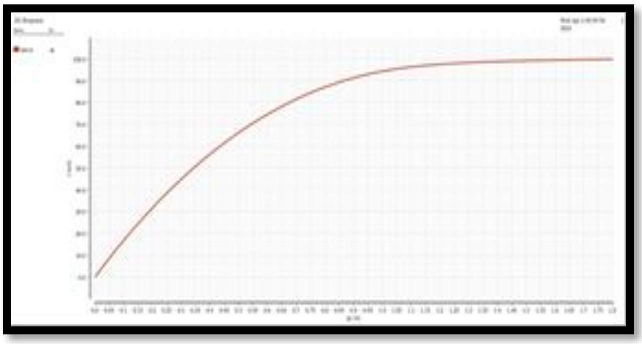
The objective of this evaluation is to comprehensively compare the behaviour of each current mirror topology under realistic and varied conditions. By understanding how each architecture responds to process scaling, temperature variations, and different technological nodes, we aim to identify the strengths and weaknesses of the topologies and gain deeper insights into their suitability for analog circuit design across a range of applications.

3.1 DC Analysis of Current Mirrors

DC analysis is an essential step in assessing the performance of current mirror topologies, as it provides valuable insights into the circuit's behavior under steady-state conditions. The key parameters analyzed include output current characteristics, output resistance, and current mirroring accuracy, all of which are critical for evaluating the efficiency and stability of current mirrors.

This refers to the accuracy of the output current relative to the reference current. The ideal scenario is for the output current to match the reference current without significant errors, which is important for precision applications.

DC analysis was performed on three current mirror topologies—Basic, Wilson, and Cascode—using a 180nm & 45nm technology node. The analysis compares how each topology performs under DC conditions, focusing on output current accuracy and output resistance.



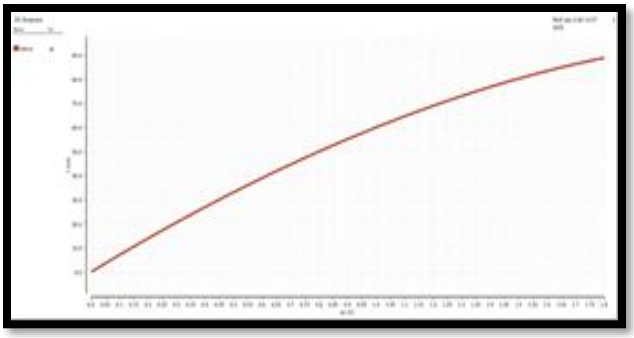


Figure 3.1.1 DC Characteristics of Basic Current Mirror

Figure 3.1.2 DC Characteristics of Wilson Current Mirror

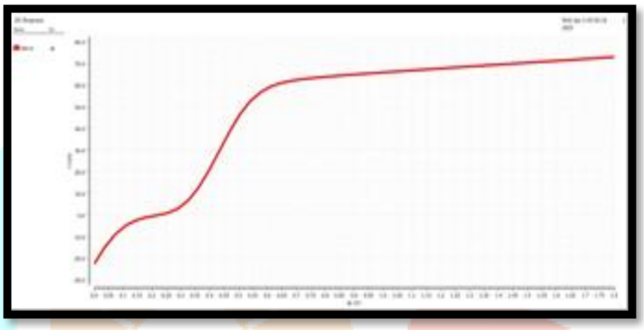


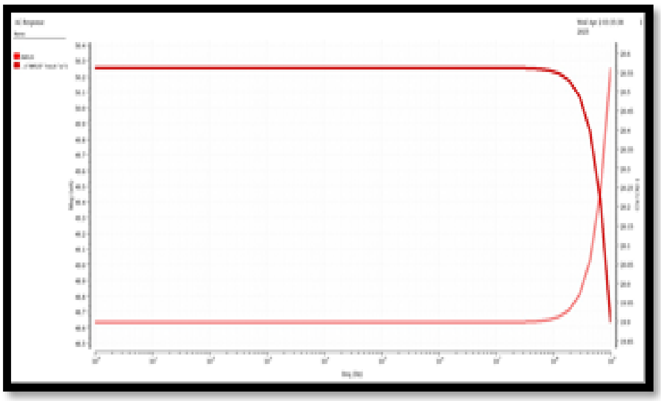
Figure 3.1.3 DC Characteristics of Cascode Current Mirror

3.2 AC Analysis of Current Mirrors

AC analysis provides critical insights into the small-signal behavior of current mirrors, particularly their frequency response, gain, and bandwidth. While DC analysis helps assess steady-state performance, AC analysis reveals how each current mirror topology behaves under dynamic signal conditions, which is essential for analog and mixed-signal circuit design.

AC analysis evaluates the small-signal performance of current mirrors across different frequencies. It focuses on frequency response, showing how the output current reacts to input variations, AC gain, which reflects how well the mirror transfers small signals, and bandwidth, indicating the frequency range over which the mirror operates effectively.

For this study, AC analysis was conducted on the Basic, Wilson, and Cascode current mirror topologies using the 180nm technology node. The input was subjected to small-signal variations, and the corresponding output response was observed over a wide frequency range.



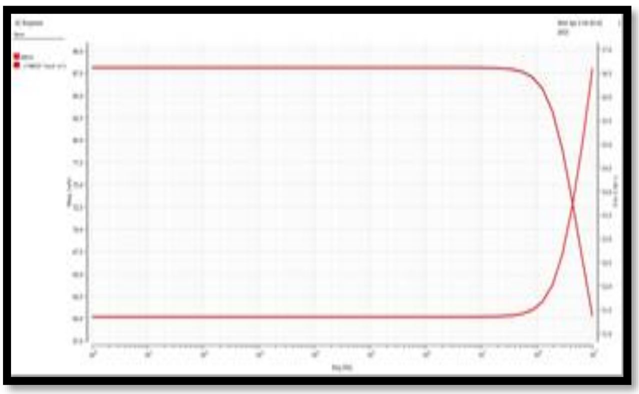


Figure 3.2.1 AC Characteristics of Basic Current Mirror

Figure 3.2.2 AC Characteristics of Wilson Current Mirror

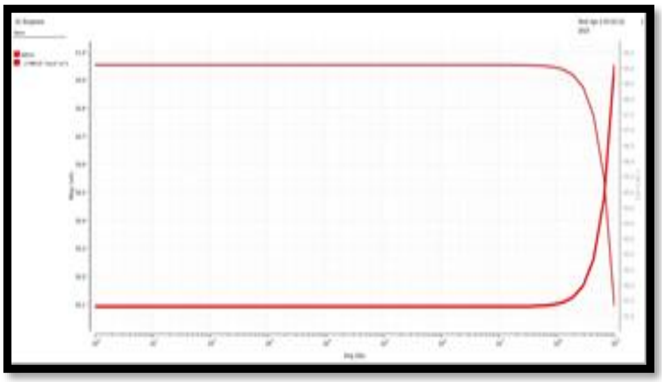


Figure 3.2.3 AC Characteristics of Cascode Current Mirror

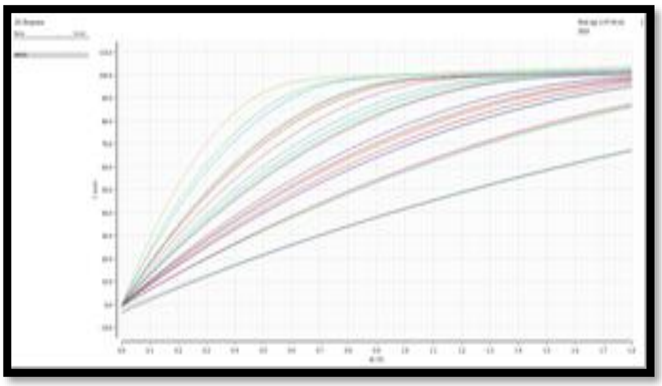
3.3 PVT (Process, Voltage & Temperature) Analysis of Current Mirrors

PVT (Process, Voltage, Temperature) analysis is a critical step in evaluating the stability, robustness, and reliability of analog circuit designs under varying real-world conditions. It provides insight into how circuit performance is influenced by unavoidable variations in semiconductor fabrication processes, fluctuations in power supply voltages, and changes in ambient temperature. For current mirrors, such analysis is essential to ensure consistent current replication across all operating scenarios.

In this study, comprehensive PVT analysis was conducted on three widely used current mirror topologies: Basic, Wilson, and Cascode, using the 180nm CMOS technology node. The process variation analysis considered four standard process corners—SS (Slow-Slow), FF (Fast-Fast), SF (Slow-Fast), and FS (Fast-Slow)—to capture the effects of manufacturing inconsistencies in NMOS and PMOS transistor characteristics. Voltage variation involved sweeping the supply voltage slightly above and below the nominal value to test the circuit's response to power fluctuations. Additionally, temperature was varied from -30°C to 125°C, including a typical room temperature of 27°C, to reflect a broad range of realistic environmental conditions.

Each simulation scenario was carefully configured using SPICE-level modeling to ensure accuracy and repeatability. The performance metrics focused on output current deviation, current matching accuracy, and temperature drift sensitivity. These parameters were selected for their relevance to analog reliability and practical deployment. The study aimed to identify which topology offers the best compromise between precision and robustness in PVT-sensitive applications.

The following figures present the output current deviations for each topology across all tested PVT conditions, offering a detailed view of their relative performance and resilience. This analysis serves as a valuable reference for analog designers aiming to optimize circuits for extreme and variable operating environments. The insights gained can guide topology selection in low-power, high-reliability integrated systems.



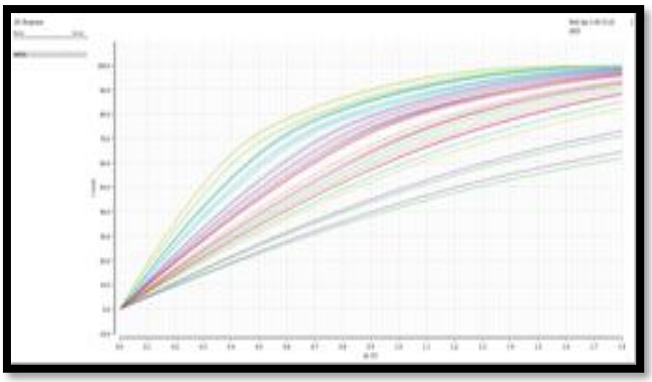


Figure 3.3.1 PVT Analysis of Basic Current Mirror **Figure 3.3.2 PVT Analysis of Wilson Current Mirror**

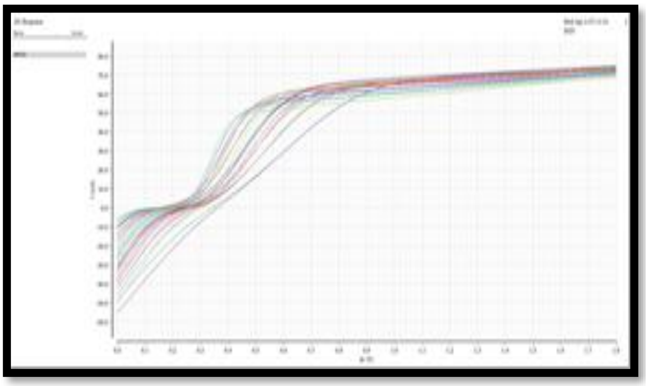


Figure 3.3.3 PVT Analysis of Cascode Current Mirror

IV. SIMULATION RESULTS

This section presents the results of electrical simulations for three types of current mirror topologies: **Simple**, **Cascode**, and **Wilson**. The objective is to compare their performance across different **transistor widths (W)** and **temperatures (T)**. All simulations were performed using **Cadence Virtuoso** with a constant **MOSFET channel length L = 130 nm**, and **VDD= 1.5 V**. The reference current (I) was fixed at **10 µA**, unless stated otherwise.

4.1 Output Voltage Sweep at Constant Temperature (T = 27 ºC)

A DC sweep was applied to the output voltage ranging from **0 V to 1.5 V**, with the ambient temperature held constant at **27 ºC**. The **output current (I)** was measured for different **transistor widths (400 nm to 800nm)**. The **output voltage** at which the mirror current reached **10 µA (Simple, Cascode)** and **5 µA (Wilson)** was recorded to evaluate compliance range and output resistance.

Observations:

- **Simple Mirror**: Required the lowest output voltage but exhibited limited compliance range.
- **Cascode Mirror**: Required a higher output voltage but offered a wider compliance range and higher output resistance.
- **Wilson Mirror**: Showed non-monotonic behaviour, where increasing W required higher V_{out} to maintain the desired current.

4.2 Load Sensitivity

Load sensitivity was assessed by observing current deviations with changes in transistor width. The voltage range where current variation remained within ±10% of the nominal value (10 µA or 5 µA) was used to evaluate robustness.

Observations:

- **Cascode Mirror** was the most stable against load variations due to higher output resistance.
- **Simple Mirror** exhibited the highest degradation in performance with width variations, indicating weaker load tolerance.
- **Wilson Mirror** performance was in-between, with moderate sensitivity to load variations.

4.3 Temperature Sensitivity

Simulations were conducted at three temperatures: **–30 °C, 27 °C, and 125 °C**, using widths **W = 400 nm, 600 nm, 800 nm**. The output resistance (Rout) was extracted at VDD= 1.5 V.

Table 4.1: Simulated results for 180nm CMOS technology at VDD = 1.5 V at Temperature = - 30°C.

Configuration	**Width**	**Rout**
Simple Current Mirror	W=400 n	27.50 kΩ
	W=600 n	58.53 kΩ
	W=800 n	120.76 kΩ
Cascode Current Mirror	W=400 n	18.08 kΩ
	W=600 n	18.85 kΩ
	W=800 n	24.89 kΩ
Wilson Current Mirror	W=400 n	24.48 kΩ
	W=600 n	19.47 kΩ
	W=800 n	14.38 kΩ

Table 4.2: Simulated results for 180nm CMOS technology at VDD = 1.5 V at Temperature = 27 °C.

Configuration	**Width**	**Rout**
Simple Current Mirror	W=400 n	20.84 kΩ
	W=600 n	29.59 kΩ
	W=800 n	52.85 kΩ
Cascode Current Mirror	W=400 n	19.99 kΩ
	W=600 n	17.96 kΩ
	W=800 n	18.57 kΩ
Wilson Current Mirror	W=400 n	33.93 kΩ
	W=600 n	25.28 kΩ
	W=800 n	18.87 kΩ

Table 4.3: Simulated results for 180nm CMOS technology at VDD = 1.5 V at Temperature = 125 °C

Configuration	**Width**	**Rout**
Simple Current Mirror	W=400 n	19.26 kΩ
	W=600 n	20.02 kΩ
	W=800 n	23.40 kΩ
Cascode Current Mirror	W=400 n	24.83 kΩ
	W=600 n	20.28 kΩ
	W=800 n	18.49 kΩ
Wilson Current Mirror	W=400 n	45.55kΩ
	W=600 n	35.79 kΩ
	W=800 n	26.54 kΩ

Table 4.4: Simulated results for 45nm CMOS technology at VDD = 1.5 V at Temperature = - 30°C.

Configuration	Width	Rout
Simple Current Mirror	W=400 n	20.34 kΩ
	W=600 n	44.64 kΩ
	W=800 n	89.29 kΩ
Cascode Current Mirror	W=400 n	21.32 kΩ
	W=600 n	16.58 kΩ
	W=800 n	18.17 kΩ
Wilson Current Mirror	W=400 n	24.46 kΩ
	W=600 n	16.32 kΩ
	W=800 n	12.27 kΩ

Table 4.5: Simulated results for 45nm CMOS technology at VDD = 1.5 V at Temperature = 27 °C.

Configuration	Width	Rout
Simple Current Mirror	W=400 n	18.29 kΩ
	W=600 n	22.74 kΩ
	W=800 n	41.76 kΩ
Cascode Current Mirror	W=400 n	26.81 kΩ
	W=600 n	18.51 kΩ
	W=800 n	16.66 kΩ
Wilson Current Mirror	W=400 n	31.00 kΩ
	W=600 n	31.00 kΩ
	W=800 n	15.59 kΩ

Table 4.6: Simulated results for 45nm CMOS technology at VDD = 1.5 V at Temperature = 125 °C

Configuration	Width	Rout
Simple Current Mirror	W=400 n	19.64 kΩ
	W=600 n	18.22 kΩ
	W=800 n	20.18 kΩ
Cascode Current Mirror	W=400 n	37.04 kΩ
	W=600 n	25.03 kΩ
	W=800 n	19.46 kΩ
Wilson Current Mirror	W=400 n	42.70 kΩ
	W=600 n	28.51 kΩ
	W=800 n	21.54 kΩ

V. CONCLUSION

The comparative analysis of current mirror topologies has led to several key insights:

1. Effect of Width (W): Increasing transistor width enhances current replication accuracy due to a reduction in (VGS). The Simple and Cascode mirrors benefit significantly from width scaling, reducing the required (V1) to reach the desired. However, the Wilson topology does not follow this trend; instead, it requires higher (V1) with increased (W), possibly due to the configuration's internal node voltage redistribution.

2. Effect of Temperature: As temperature rises, all topologies exhibit increased output current due to a decrease in threshold voltage and improved subthreshold conduction. This highlights a temperature sensitivity that must be accounted for in precision analog designs.

3. Topology Comparison:

- The Simple mirror is compact and low-power but suffers from limited output resistance and poor load/temperature stability.
- The Cascode mirror exhibits superior performance in terms of output impedance and compliance range, making it suitable for high-gain and precision applications.

The Wilson mirror provides a trade-off with moderate area and complexity while achieving reasonable accuracy.

VI. ACKNOWLEDGEMENT

The authors express their sincere gratitude to the Department of Electronics and Communication Engineering, KLS Vishwanathrao Deshpande Institute of Technology, Haliyal, for providing the necessary resources and technical support throughout this project.

The authors also thank the faculty mentors for their valuable guidance and the VTU Belagavi for offering an academic framework conducive to research. Special appreciation is extended to the Cadence design suite support team for enabling the simulations used in this study.

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