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DESIGN OF TUNABLE ALUs WITH INTEGRATED POWER MINIMIZATION TECHNIQUES

[1] M. KRISHNA SAI NAIK, [2]Dr. D. SRIHARI
[1]M. Tech Student, [2]Professor (Guide) & HOD
[1]Electronics and Communication Engineering (VLSI Design)
[2]Electronics and Communication Engineering (VLSI Design)
[1]SRI VENKATESWARA COLLEGE OF ENGINEERING AND TECHNOLOGY(AUTONOMOUS)
[2]SRI VENKATESWARA COLLEGE OF ENGINEERING AND TECHNOLOGY(AUTONOMOUS)

Abstract:

Minimizing power consumption is a crucial concern in VLSI design. The Arithmetic Logic Unit (ALU), a fundamental processor component, performs arithmetic and logical operations, often leading to increased power usage with higher complexity. A major contributor to dynamic power is the clock network, which can be optimized using clock gating to disable inactive blocks. Existing literature offers multiple power reduction techniques within ALUs, but further optimization is achievable by integrating diverse approaches. This project presents a tunable ALU design employing clock gating along with Parallel-In Parallel-Out (PIPO) shift registers and Booth's algorithm. Specific operations are activated based on the input opcode, while others remain idle to minimize power. The ALU supports 8-bit inputs, carry-in, borrow-in, enable signals, and a 2-bit shift input, with a 4:16 decoder enabling 16 operations through a 4-bit opcode. The design evaluates four clock gating techniques: latch-free, latch-based, flip-flop-based, and synthesis-based gating, all integrated with PIPO registers. Each design iteration demonstrates reduced power consumption through selective operation activation and efficient data handling.

Keywords: —Tunable ALU, Dynamic Power, Clock Gating, RTL Design, PIPO, Booth's Algorithm, Power Optimization

I. INTRODUCTION:

Minimizing power dissipation has become a crucial concern in VLSI design. In the past, design optimization primarily emphasized area, delay, and testability. With the advancement of technology and downscaling, issues such as increased leakage and power dissipation have emerged in chips. To tackle these challenges, optimization methods like clock gating and voltage scaling must be adopted. Today, VLSI designers consider four primary aspects for any design: area, delay, testability, and power. Consumers now demand electronics that are lightweight, fast, and thermally efficient. For instance, modern smartphones are expected to perform multiple functions swiftly without overheating. To achieve this, various ICs are integrated into a single chip, which escalates both area usage and power consumption, often leading to heat buildup.

Technology scaling helps in reducing the chip area but tends to increase power dissipation, resulting in overheating. To ensure fast response, compactness, and lower temperature operation, adopting low-power techniques is essential. Fig. 1 highlights the four key dimensions for VLSI chip optimization. Power

consumption in a chip comprises both static and dynamic components. Static power dissipation occurs even when the circuit is off, and as transistor sizes shrink, leakage power becomes more significant. This leakage arises from drain-induced barrier lowering (DIBL), hot carrier effects, channel punch-through, and reverse-biased source/drain junction leakage. On the other hand, dynamic power is consumed during switching—when output capacitance charges and discharges based on node activity and clock frequency.

Dynamic power dissipation manifests primarily during signal transitions at specific nodes; otherwise, it remains negligible. The primary contributor to dynamic power is switching activity, which is largely governed by the clock signal. In this project, our focus is on reducing dynamic power by minimizing unnecessary signal transitions. Since the clock network is a significant dynamic power, gating the clock when not in use results in meaningful savings. Through operation selection logic, only the required operations are activated while others remain idle, avoiding transitions and reducing dynamic power. The selection-based activation ensures less energy wastage in the inactive units. Historically, the major concerns in VLSI design included area, performance, cost, and power consumption. However, power has become a focal point, on par with speed and area.

Power optimization strategies vary with application types and circuit design. In compact battery-powered devices like smartphones, the objective is to maximize battery life while keeping the size and packaging cost minimal. Scaling CMOS devices has allowed the semiconductor industry to meet the demand for higher speed and integration. However, as transistor dimensions shrink, sub-threshold leakage currents increase, especially when transistors are off but not fully turned off. This inability to completely shut off transistors contributes to higher leakage power. Hence, leakage has become a major component of total power in modern silicon technologies. The three main design parameters in VLSI are power, speed, and area. In CMOS circuits, overall power dissipation stems from three key factors: dynamic, static, and short-circuit components.

II. EXISTING METHOD:

Reducing power usage is essential in VLSI design, especially within Arithmetic Logic Units (ALUs), which are critical blocks in processors. ALUs perform key arithmetic and logical operations that heavily influence power behavior. The clock network contributes significantly to energy use, and deactivating it during idle cycles can lead to considerable savings.
One conventional approach for minimizing power integrates clock gating with Parallel Input Parallel Output (PIPO) shift registers and the Booth multiplier algorithm to design a low-power ALU. Specific operational codes (opcodes) are employed to control ALU functions, selectively enabling necessary tasks using inputs like carry-in (cin), borrow-in (bin), enable flags, and 2-bit control signals. A 4:16 line decoder interprets a 4-bit opcode to activate one of sixteen available operations.

Clock gating disables the clock in inactive modules, cutting down dynamic power caused by unnecessary transistor switching. This method proves efficient for flip-flops that retain control or intermediate values by stopping excess transitions. PIPO registers are responsible for both incoming data and intermediate values, enhancing speed by enabling concurrent processing.
The Booth encoding method minimizes redundant arithmetic operations. It is particularly effective for binary multiplication and division of signed numbers, allowing the system to perform fewer additions by encoding multiplier values. The integration of PIPO registers, clock gating, and the Booth algorithm helps minimize switching activity, leading to lower energy use, improved processing, and longer battery life for portable electronics.

The design combines different forms of clock gating with PIPO shift registers, implemented and verified on a Virtex-6 FPGA using 40nm fabrication technology. The evaluation spans clock frequencies from 100MHz to 1GHz, measuring dynamic power consumed in ALUs configured with and without clock gating alongside PIPO and Booth logic.
Various techniques are employed in existing tunable ALUs for efficient power management. These include gate-level methods (implementing energy-efficient logic structures), circuit-level strategies (such as voltage/current scaling and threshold voltage tuning), and power gating (shutting off unused components). Additional methods include clock gating, transition-aware data encoding, and high-level architectural improvements using low-power logic and optimal data path handling.

The Effectiveness of these approaches is application-dependent and often improves when multiple

methods are used together. Circuit-level practices like voltage scaling (reducing supply voltage), current tuning (modifying bias), and threshold voltage management help curb leakage. Dynamic voltage scaling adjusts voltage dynamically with the workload while leakage-saving designs aim to minimize standby power.

At the architectural level, systems are crafted to balance power savings with functional needs. Dynamic Voltage and Frequency Scaling (DVFS) changes operating levels in real time to conserve power under light loads and improve throughput during peak demands. Enhanced interconnect design and low-power data encoding limit unnecessary transfers and reduce energy waste.

The currently used ALU structure combines clock gating, Booth encoding, and PIPO logic to isolate active modules while disabling unused paths. This helps reduce dynamic switching and thus lowers overall power. Experimental setups test these combinations under various frequency conditions to evaluate power-saving potential. The joint use of power gating and clock gating further minimizes both static and dynamic consumption in CMOS-based ALU circuits.

III. PROPOSED METHOD:

Performance and Operation of ALU

This proposed method focuses on a reconfigurable 8-bit Arithmetic Logic Unit (ALU) with tunable modules and integrated low-power design techniques. The ALU supports basic and complex operations such as addition, subtraction, multiplication, division, bitwise logic, shifts, and complement functions. The key feature of this design is its **operation-specific tunability**, where each functional block is activated only when required by the opcode. This selective activation minimizes unnecessary power usage and ensures optimal functionality. Low-power D flip-flops are used for internal registers, operating under a tunable clock management system that adapts based on real-time instruction analysis.

The architecture is described and tested using Xilinx ISE 14.4 and implemented on a Virtex-6 FPGA with 40nm CMOS technology. The Xpower Analyzer evaluates the energy profile of the tunable ALU. Custom opcodes control block-level enable signals, improving the efficiency of switching logic and reducing dynamic power. The outcomes of various configurations and operation-based tuning are analyzed in the results section.

Tunable Clock Gating Techniques

The proposed ALU integrates smart clock gating techniques that dynamically adjust based on selected operations. Clock gating is controlled by an opcode decoder, which activates only the relevant parts of the ALU. Four advanced techniques are implemented and tuned for performance and power metrics across the arithmetic and logic operations.

1. **Signal-Aware Latch-Free Clock Gating:**
   Basic logic gates manage gating signals based on real-time inputs.
   Tuned to prevent false activation using a filtered enable logic but remains prone to occasional glitches.

2. **Operation-Controlled Latch-Based Gating:**
   Introduces operand-aware latches that enable gating only during actual data operations.
   This method blocks transitions when inputs are idle, reducing redundant toggling significantly.

3. **Opcode-Driven Flip-Flop Gating:**
   Uses opcode-driven flip-flops to delay and synchronize enable signals with clock transitions.
   Offers better stability and clock control in operation-heavy ALU pipelines.

4. **Compiler-Assisted Synthesis Gating:**
   Clock gating logic is automatically inserted by synthesis tools using HDL pragmas and constraints.
   This technique improves timing closure and power efficiency without manual intervention.

5. Detailed Implementation Results

The tunable ALU with these clock gating methods is implemented and tested at different operating frequencies ranging from 100MHz to 1GHz. Results show that combining opcode-based tuning with compiler-assisted gating leads to major reductions in dynamic switching. Operation-controlled latching exhibits the highest savings, especially during idle or repetitive instruction cycles. This approach maintains performance while minimizing power waste.

6. Power Optimization Techniques

Dynamic power reduction is achieved by isolating unused blocks and using selective clock control through opcode-aware gating logic. For static power minimization, a modified LECTOR-based leakage reduction technique is embedded within the critical logic paths. The system also supports real-time reconfiguration of operation modes, which enables better thermal stability and energy management. Together, these methods create a scalable and tunable ALU architecture suitable for portable and low-power embedded systems.

IV. ADVANTAGES:

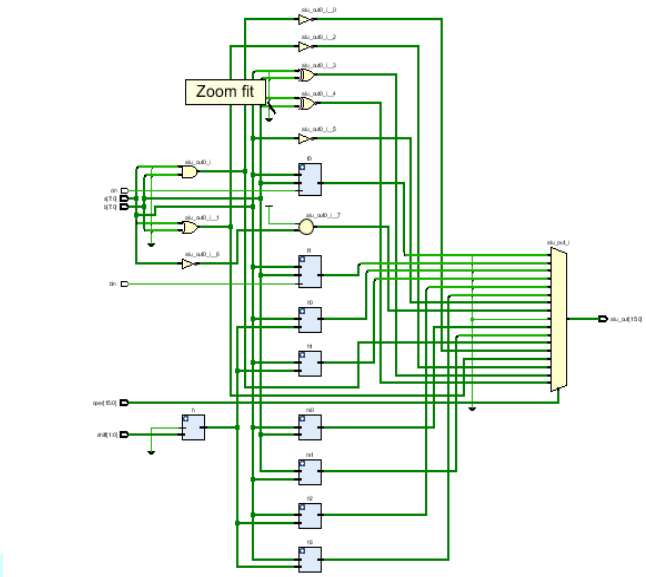
- Lower Energy Consumption: Efficient tuning and power-saving techniques reduce energy usage across ALU operations.
- Extended Battery Operation: It is beneficial for portable electronics like smartphones, tablets, and IoT gadgets for longer battery durations.
- Improved Computational Speed: Achieves better execution speed and responsiveness through optimized and targeted operation modes.
- Dynamic Reconfigurability: Allows real-time reconfiguration of functional units, adapting to workload changes while conserving energy.
- Design Scalability: Supports expansion to higher-bit ALUs or more complex systems without drastically changing or increasing power demands.
- Stable Thermal Performance: Maintains acceptable operating temperatures with stability, improving device reliability and preventing overheating.
- Reduction in System Costs: Lower power demand reduces the need for high-capacity cooling or power regulation hardware, cutting system costs.

V. APPLICATIONS:

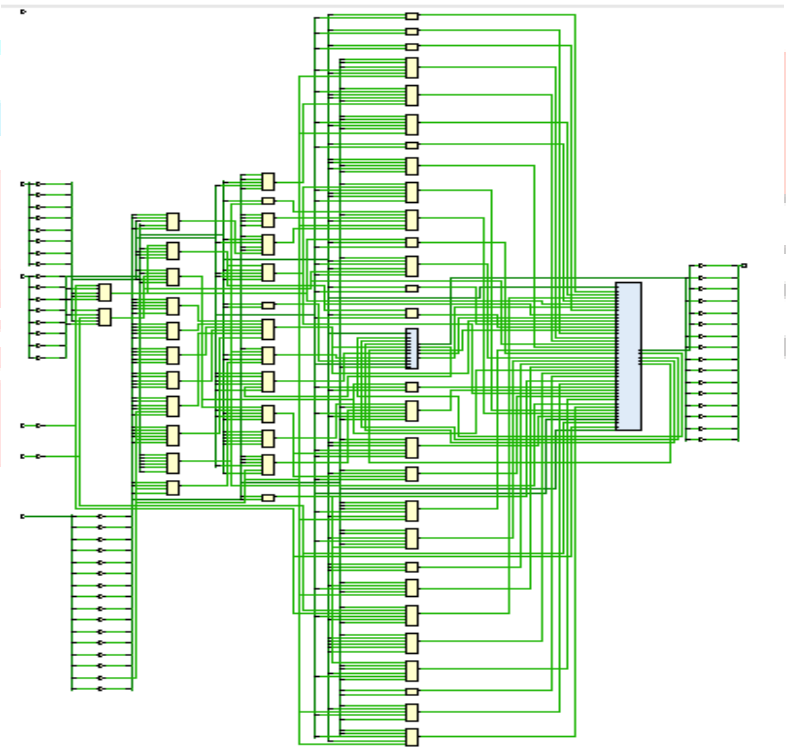
- **Smart Devices:** Vital for smartphones, tablets, and wearable tech to enhance battery efficiency and deliver prolonged, user-friendly operation.
- **IoT Networks:** Support low-power functionality and longer device duration in IoT environments by minimizing energy usage and maintenance cycles.
- **Embedded Platforms:** Used in sectors like automotive, healthcare, aerospace, and industry for meeting strict power and performance requirements.
- **Cloud and Data Infrastructure:** Assists in optimizing energy usage in server farms and data centers, leading to reduced operational costs and greener computing.
- **Advanced Computing Systems:** Ideal for energy-conscious HPC setups that demand a balance between peak performance and low power draw.
- **In-Vehicle Systems:** Powers efficient and dependable operation in electronics such as infotainment systems and ADAS features within automobiles.
- **Portable Electronics:** Enhances performance and battery runtime in laptops, handhelds, and wearables through fine-grained power control mechanisms.

VI. RESULTS:

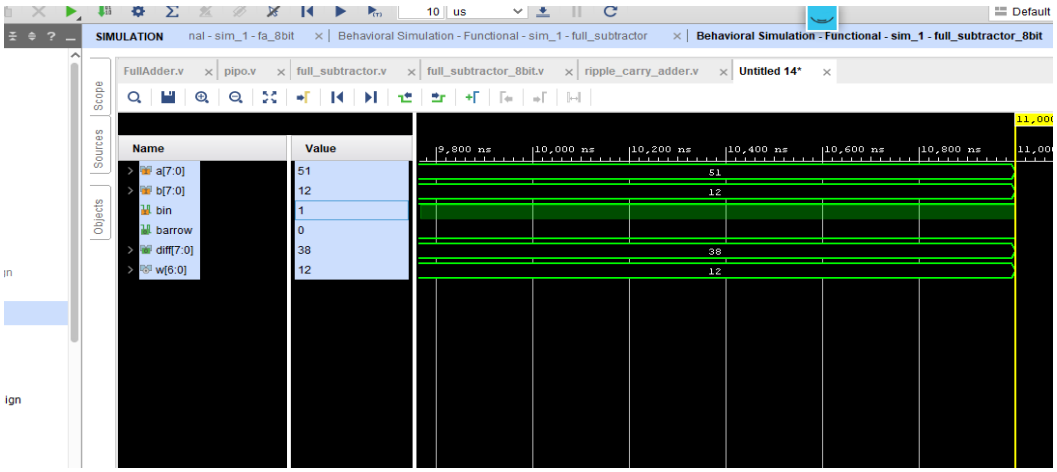
RTL Schematic:



Technology schematic:



Simulation:



Area:

Name	Slice LUTs (134600)	Slice (33650)	LUT as Logic (134600)	Bonded IOB (400)
ALU	353	101	353	50
m0 (booth_mul)	169	50	169	0
m1 (booth_div)	144	49	144	0

Delay:

```
Max Delay Paths
--------------------------------------------------------------------------------------
Slack:                  inf
  Source:               b[1]
                          (input port)
  Destination:          alu_out[0]
                          (output port)
  Path Group:           (none)
  Path Type:            Max at Slow Process Corner
  Data Path Delay:      32.568ns  (logic 14.980ns (45.996%)  route 17.588ns (54.004%))
  Logic Levels:         43  (CARRY4=21 IBUF=1 LUT2=7 LUT3=7 LUT4=1 LUT6=5 OBUF=1)
```

Power:

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power:	**5.928 W**
Design Power Budget:	**Not Specified**
Power Budget Margin:	**N/A**
Junction Temperature:	**36.1°C**
Thermal Margin:	48.9°C (25.8 W
Effective ϑJA:	1.9°C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Launch Power Constraint Advisor to find and fix invalid switching activity

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**10.437 W**
Design Power Budget:	**Not Specified**

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power:	**444.893 W (Junction temp exceeded!)**

Evaluation table for Area, Delay:

Name	Slice LUTs (134600)	Slice (33650)	LUT as Logic (134600)	Bonded IOB (400)
ALU	353	101	353	50
m0 (booth_mul)	169	50	169	0
m1 (booth_div)	144	49	144	0

VII. CONCLUSION

The design of tunable ALUs with integrated power minimization techniques offers a detailed examination of methods aimed at lowering power usage in tunable Arithmetic Logic Units. This research addresses the growing need for energy-efficient architectures in contemporary computing systems. The study investigates a variety of power-saving strategies, such as gate-level, circuit-level, and algorithm-level optimizations. These techniques are cohesively integrated to enable substantial power reduction while preserving the ALU's tunability and core functionality.

The results of the study demonstrate the effectiveness of the proposed Integrated Power minimization Techniques, by carefully analyzing the Design of Tunable ALUs at different levels the researchers can achieve effective power minimizations without compromising the performance of the ALU.

The findings confirm the efficiency of the integrated power minimization methods. Through multi-level design analysis and optimization, the study achieves notable power savings without sacrificing the performance or adaptability of the tunable ALU.

VIII. REFERENCES

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