IJCRT.ORG ISSN : 2320-2882

INTERNATIONAL JOURNAL OF CREATIVE RESEARCH THOUGHTS (IJCRT)

An International Open Access, Peer-reviewed, Refereed Journal

# Low Noise Amplifier Design With Noise And Distortion Cancellation: A Survey of CMOS Implementations

[1]Karthik Bhat M, [2]Dr. Vasundhara Patel K S

[1]MTech student, [2]Professor

[1]VLSI Design and Embedded Systems, Department of ECE,

[1]BMS College of Engineering, Bengaluru, Karnataka

***Abstract:*** Low Noise Amplifiers (LNAs) serve as the critical front-end block in the receiver chain of any transceiver system, where minimizing noise, power consumption, and area is essential for overall performance. This review presents a comprehensive analysis of various LNA topologies, evaluating their power efficiency and noise characteristics. The study reveals that conventional single-stage LNAs often fall short of stringent noise performance requirements, necessitating the adoption of noise cancellation techniques. However, traditional noise cancellation approaches typically incur higher power consumption. To address this, sub-threshold operation of transistors is explored as a low-power alternative, albeit with the trade-off of increased noise. To mitigate this, the review examines the integration of noise cancellation methods tailored for sub-threshold LNAs, effectively suppressing the excess noise while retaining power efficiency. The paper offers comparative insights into different LNA architectures and highlights promising strategies for achieving optimal trade-offs between noise figure, power consumption, and design complexity.

***Index Terms*** - Low Noise Amplifier (LNA), Noise cancellation, Low-power design, CMOS LNA, Noise figure, RF circuit design, Transceiver systems, gain, linearity, S parametrs

## Introduction

Consumer transceivers require compact, low-power, and cost-effective designs, driving full integration onto a single chip. The receiver's first block, the Low Noise Amplifier (LNA), must offer low noise and power consumption to recover weak RF signals. Transmitters, though less complex, dominate power usage but can be shut down to save energy.

A Low Noise Amplifier (LNA) is an essential component in any receiver system, used to amplify weak signals captured by the antenna without introducing significant additional noise. Since the received signals are typically very low in strength, maintaining signal integrity through low noise amplification is critical. The LNA serves as the first gain stage in the receiver chain and plays a key role in determining the overall noise performance of the system. Designing an LNA is challenging due to the trade-off between gain and noise figure, higher noise figures typically result in lower gain. Key design considerations include noise figure, power gain ($S_{21}$), input/output impedance matching ($S_{11}/S_{22}$), power consumption, bandwidth, stability, and linearity, all of which influence the efficiency and performance of the receiver.

Modern transceivers require LNAs with very low noise figures, but single-stage designs have high NF due to noise from biasing circuits. To meet stringent noise requirements, two-stage LNAs with noise cancellation techniques are preferred, where an auxiliary path cancels noise from the main path. The auxiliary path's noise is minimized by increasing its current.

Single-stage LNAs have high noise figures, leading to the use of noise cancellation techniques, which increase power consumption. To meet low-power demands in mobile transceivers, combining dual noise cancellation technique and sub-threshold operation offers a promising solution for achieving low-noise, low-power LNA designs.

A key challenge in RF system design is ensuring proper input and output matching to minimize signal loss and maximize power transfer. Proper matching improves noise figure, making it a critical aspect of LNA design.

## I. METHODOLODY

This review paper explores recent advancements in low noise amplifier (LNA) design, emphasizing noise-cancellation methods, low-power techniques, and wideband applications across CMOS technologies. The review draws primarily from peer-reviewed journal and conference papers published between 2015 and 2024, sourced through academic databases. Papers were prioritized based on their innovation in architecture, clarity of experimental results or simulations, and contributions to low-power or noise-sensitive communication systems, such as IoT, 5G, and UWB technologies. Foundational studies introducing or significantly enhancing techniques like feedforward and feedback noise cancellation, gm boosting, and subthreshold operation were particularly emphasized. Approximately 20 papers were selected that demonstrate a wide range of design methodologies, frequency bands (from MHz to mmWave), and performance trade-offs. These works provide a representative cross-section of the state of the art and form the basis for the comparative analysis, discussion, and identification of future trends included in this review.

## II. LITERATURE SURVEY

Recent advancements in Low Noise Amplifier (LNA) designs have demonstrated significant improvements in noise performance, gain, linearity, and power efficiency across various frequency ranges and CMOS technologies.

Rahman and Harjani [1] introduced a dual-path noise and nonlinearity cancelling LNA operating at 2.4 GHz, leveraging both feedforward noise cancellation and feedback noise reduction techniques. This approach effectively mitigates noise from the main and auxiliary signal paths, achieving a noise figure (NF) of 2.8 dB, a gain of 17.4 dB, an input third-order intercept point (IIP3) of 10.7 dBm, and ultra-low power consumption of 475 µW. Similarly, Aravinth Kumar et al. [3] proposed a wideband (2–5 GHz) noise-cancelling LNA operating in the subthreshold region, utilizing gate inductor-assisted impedance matching and current reuse feedforward noise cancellation. Fabricated in a 180 nm CMOS process, this design achieves a noise figure of 6 dB, gain of 13 dB, 3 GHz bandwidth, and a power consumption of 1 mW, demonstrating the effectiveness of low-power techniques for broadband applications.

In the ultra-wideband domain, Lee and Kwon [4] presented a 3–10 GHz noise-cancelling CMOS LNA employing a gm-boosting technique to reduce current in the matching stage. Fabricated in 110 nm CMOS technology, the LNA achieves a noise figure ranging from 2.4 to 2.9 dB, a gain between 17.5 and 18.7 dB, and consumes 8.3 mW. Its common gate input stage coupled with a gm-boosted common-source stage effectively improves noise cancellation and linearity, evidenced by an IIP3 of 0.6 dBm.

Guo et al. [5] developed a complementary noise cancelling LNA using multiple complementary nMOS and pMOS transistors to suppress third-order distortions arising from noise cancellation stages. This 180 nm CMOS design operates at low power with a current reuse topology, delivering a gain of 17 dB, noise figure of 3.5 dB, and consuming 9.7 mW. Kim and Kwon [6] introduced a low-frequency (50 MHz to 1 GHz) noise-cancelling balun-LNA employing a modified current-bleeding technique and balanced loads. Their design integrates common-gate and common-source stages with a balun circuit to optimize low-power operation. The LNA achieves a voltage gain of 30 dB, a minimum noise figure of 2.3 dB, and consumes 9.3 mW.

Pan et al. [7] proposed an inductorless LNA combining common-gate and common-source stages with shunt feedback and cross-coupled push-pull structures to achieve gm enhancement and partial noise cancellation. Implemented in CMOS technology, the design effectively mitigates the Miller effect with cascode transistors and uses current steering to improve bandwidth and gain, achieving a 4 dB noise figure at 2 mW power consumption.Tang et al. [8] designed a wideband complementary noise and distortion cancelling

LNA targeting high-frequency ultrasound imaging applications. This 180 nm CMOS LNA employs feedforward noise cancellation and leverages complementary NMOS and PMOS devices to cancel second-order harmonics, enhancing linearity. It achieves a noise figure of 2.1 dB with power consumption of 18 mW.

Regulagadda et al. [9] presented a packaged, single-ended wideband LNA that combines gate-source inductor-assisted impedance matching and current reuse feedforward noise cancellation techniques. Fabricated in CMOS, the design delivers a noise figure of 2.5 dB while consuming 29 mW, optimizing bandwidth and gain for high-sensitivity receivers.

Guo et al. [10] also reported an inductorless noise-cancelling CMOS LNA utilizing a complementary stacked NMOS/PMOS configuration to compensate second-order nonlinearity and mitigate third-order distortion using weak inversion transistors. The design achieves a noise figure of 2.8 dB at 19 mW power consumption.

Yu et al. [11] introduced a resistor-plus-source-follower feedback noise-cancelling LNA featuring resistor feedback combined with source follower feedback (SFF) to enhance gain and noise figure. This approach reduces noise contributions from both the feedback resistor and noise-cancelling transistors. The LNA achieves a noise figure of 3.77 dB and consumes 11.3 mW.

In the context of broadband LNAs, a two-stage design exploiting lossy input matching components for noise figure and stability optimization was presented [12]. Implemented in 0.25 µm GaN technology, the LNAs achieve noise figures of 1.3 and 1.5 dB with gains of 15 and 16 dB at 6 GHz, respectively.

A broad frequency range LNA covering 2–40.5 GHz was developed [13] using multiple bandwidth expansion techniques such as cascode, resistance feedback, and cascode Darlington amplifiers in a 0.15 µm GaAs pHEMT process. The three-stage design achieves an average gain of 21.6 dB, noise figure below 3.6 dB, and output 1 dB compression points between 4.5 and 12.8 dBm.

To address out-of-band blocker rejection in cellular applications, a CMOS LNA employing parallel all-pass and band-stop filters was proposed [14]. Fabricated in 65 nm CMOS, it operates over 0.7–2.7 GHz, providing blocker rejections of 22.8 dB and 16 dB for low and high bands, respectively, with noise figures between 3.7 and 4.9 dB, gains of approximately 10.5–11 dB, and 23.9 mA current consumption.

For IoT and RFID applications, a compact 90 nm CMOS design integrated an SPDT switch and LNA [16]. The LNA uses a gyrator-based active inductor and buffer to achieve a peak gain of 33 dB, 30 MHz bandwidth, and 6.6 dB noise figure at 2.45 GHz. The SPDT switch exhibits low insertion loss (0.83 dB) and high isolation (45.3 dB).

At millimeter-wave frequencies, a two-stage LNA for 5G applications operating at 26–28 GHz was implemented in 0.25 µm SiGe BiCMOS technology [17]. The design combines common base and emitter stages to minimize Miller effects, achieving 26 dB gain and an average noise figure of 3.84 dB under a 3.3 V supply.

In advanced CMOS, a compact 33 GHz LNA in 28 nm LP CMOS technology [18] was developed with two cascode stages, leveraging electromagnetic simulations to optimize passive components. It achieves a noise figure of 4.9 dB, gain of 18.6 dB, occupies 0.68×0.34 mm², and consumes 9.7 mW.

A 60 GHz LNA designed in 28 nm low-power CMOS [19] demonstrates high-frequency device modeling and layout techniques, achieving 13.8 dB gain, 18 GHz bandwidth, 4 dB noise figure, and 12.5 dBm 1 dB compression point at 24 mW power consumption, setting benchmarks for mm-wave LNAs.

Finally, a 2.2–13.2 GHz CMOS differential common-gate LNA targeting ultra-wideband receivers was presented [20]. Fabricated in 65 nm CMOS, it employs capacitor cross-coupled gm boosting and positive current feedback, achieving 16.3 dB peak gain, 3.3 dB noise figure, 3.2 mW power consumption, and operation under a 1 V supply.

## III. DISCUSSION

The reviewed literature reveals that significant progress has been made in the design of noise-cancelling low-noise amplifiers (LNAs), targeting wideband operation, power efficiency, and linearity. Most modern LNAs employ dual-path topologies that balance gain and noise performance while attempting to minimize power. For instance, paper [1] showcases exceptional performance with both noise and nonlinearity cancellation, achieving sub-3 dB NF with ultra-low power. Subthreshold operation ([3]) is viable for energy-constrained applications but comes with compromised NF, indicating a need for more effective noise mitigation in this regime. High-frequency and ultra-wideband LNAs ([4], [11]) often leverage gm-boosting and feedback structures to maintain a flat gain and low NF over large bandwidths, but typically consume more power. Complementary transistor topologies ([5], [8]) show promise in reducing harmonic distortion and enhancing linearity, though their complexity and higher power draw remain trade-offs. Inductorless designs ([7], [10]) offer area savings and simplified integration but face challenges in achieving comparable NF and gain.

Table 1 provides a comparative summary of recent LNA designs, highlighting key parameters such as frequency range, noise figure, gain, power consumption, CMOS node, and design techniques. It illustrates trade-offs between noise performance, power efficiency, and gain across various technologies. The table aids in identifying suitable LNA topologies for applications like IoT, 5G, and broadband systems.

Table 1: Comparison of LNA Performance Metrics and Design Techniques

| Paper | Frequency Range | NF (dB) | Gain (dB) | Power (mW) | Technique | CMOS Node |
|---|---|---|---|---|---|---|
| [1] | 2.4 GHz | 2.8 | 17.4 | 0.475 | Dual-path noise & nonlinearity cancelling | 65 nm |
| [3] | 2 - 5 GHz | 6.0 | 13.0 | 1.0 | Subthreshold + feedforward cancellation | 180 nm |
| [4] | 3 - 10 GHz | 2.4 - 2.9 | 17.5 -18.7 | 8.3 | gm-boosting, CG-CS topology | 110 nm |
| [5] | ~3 - 5 GHz | 3.5 | 17.0 | 9.7 | Complementary NMOS/PMOS, current reuse | 180 nm |
| [6] | 50 MHz - 1 GHz | 2.3 | 30.0 | 9.3 | Current bleeding + balanced loads | 65 nm |
| [7] | ~3 - 5 GHz | 4.0 | 21.2 | 2.0 | Inductorless, gm-boosting, push-pull | 65 nm |
| [8] | 30 - 120 MHz | 2.1 | 19 | 18.0 | Complementary NMOS/PMOS, harmonic cancellation | 180 nm |
| [9] | 0.4 - 2.2 GHz | 2.5 | 20.5 | 29.0 | Packaged, current reuse feedforward cancellation | 65 nm |
| [10] | ~3 - 5 GHz | 2.8 | 16.1 | 19.0 | Inductorless, NMOS/PMOS distortion cancellation | 180 nm |
| [11] | 0.5 - 7 GHz | 3.3 ± 0.45 | 16.8 | 11.3 | Resistor + source-follower feedback | 65 nm |

## IV. CONCLUSION

The state-of-the-art in LNA design reflects a careful balance of power, gain, noise, and bandwidth, driven by application-specific constraints. Dual-path and complementary structures emerge as effective strategies for noise cancellation, while gm-boosting and inductorless techniques support integration and bandwidth scalability. However, each solution comes with inherent trade-offs in complexity, power, or area. Moving forward, innovations will focus on hybridizing these methods, optimizing for extreme low-power use cases, and adapting LNAs for the wide frequency demands of next-gen wireless systems and IoT platforms.

## REFERENCES


[1] M. Rahman and R. Harjani, "A 2.4-GHz, Sub-1-V, 2.8-dB NF, 475-µW Dual-Path Noise and Nonlinearity Cancelling LNA for Ultra-Low-Power Radios," IEEE J. Solid-State Circuits, vol. 53, no. 5, pp. 1423-1430, May 2018, doi: 10.1109/JSSC.2017.2786736.

[2] Das and N. Nallam, "Noise Cancelation? Explained!: The Role of Feedback in Noise-Canceling LNAs and Receivers," IEEE Microw. Mag., vol. 18, no. 6, pp. 100-109, Sept.-Oct. 2017, doi: 10.1109/MMM.2017.2712039.

[3] R. A. Kumar, B. D. Sahoo and A. Dutta, "A Wideband 2–5 GHz Noise Canceling Subthreshold Low Noise Amplifier," IEEE Trans. Circuits Syst. II: Express Briefs, vol. 65, no. 7, pp. 834-838, July 2018, doi: 10.1109/TCSII.2017.2719678.

[4] M. Lee and I. Kwon, "3–10 GHz noise-cancelling CMOS LNA using gm-boosting technique," IET Circuits, Devices & Syst., vol. 12, no. 1, pp. 12-16, Jan. 2018, doi: 10.1049/iet-cds.2017.0094.

[5] B. Guo, J. Chen, L. Li, H. Jin and G. Yang, "A Wideband Noise-Canceling CMOS LNA With Enhanced Linearity by Using Complementary nMOS and pMOS Configurations," IEEE J. Solid-State Circuits, vol. 52, no. 5, pp. 1331-1344, May 2017, doi: 10.1109/JSSC.2017.265759.

[6] S. Kim and K. Kwon, "A 50-MHz–1-GHz 2.3-dB NF Noise-Cancelling Balun-LNA Employing a Modified Current-Bleeding Technique and Balanced Loads," IEEE Trans. Circuits Syst. I: Regular Papers, vol. 66, no. 2, pp. 546-554, Feb. 2019, doi: 10.1109/TCSI.2018.2866184.

[7] Z. Pan, C. Qin, Z. Ye, Y. Wang and Z. Yu, "Wideband Inductorless Low-Power LNAs with Gm-Enhancement and Noise-Cancellation," IEEE Trans. Circuits Syst. I: Regular Papers, vol. 65, no. 1, pp. 26-38, Jan. 2018, doi: 10.1109/TCSI.2017.2710057.

[8] Y. Tang, Y. Feng, Q. Fan, C. Fang, J. Zou and J. Chen, "A wideband complementary noise and distortion canceling LNA for high-frequency ultrasound imaging applications," 2018 Texas Symposium on Wireless and Microwave Circuits and Systems (WMCS), Waco, TX, 2018, pp. 1-4, doi: 10.1109/WMCaS.2018.8400635.

[9] S. S. Regulagadda, B. D. Sahoo, A. Dutta, K. Y. Varma and V. S. Rao, "A Packaged Noise-Canceling High-Gain Wideband Low Noise Amplifier," IEEE Trans. Circuits Syst. II: Express Briefs, doi: 10.1109/TCSII.2018.2828781.

[10] B. Guo, J. Chen, H. Chen, X. Wang and C. Liu, "An inductorless noise-cancelling CMOS LNA using wideband linearization technique," 2017 IEEE 12th International Conference on ASIC (ASICON), Guiyang, 2017, pp. 690-693, doi: 10.1109/ASICON.2017.8252569.

[11] H. Yu, Y. Chen, C. C. Boon, C. Li, P. Mak and R. P. Martins, "A 0.044-mm² 0.5-to-7-GHz Resistor-Plus-Source-Follower-Feedback Noise-Cancelling LNA Achieving a Flat NF of 3.3±0.45 dB," IEEE Trans. Circuits Syst. II: Express Briefs, doi: 10.1109/TCSII.2018.2833553.

[12] M. Zaid, P. Kumari, A. Pampori, M. S. Nazir, U. Goyal, M. Mishra, and Y. S. Chauhan, "Optimizing Low Noise Amplifiers: A Two-Stage Approach for Improved Noise Figure and Stability," IEEE Access, vol. 12, pp. 1-10, Apr. 10, 2024, doi: 10.1109/ACCESS.2024.3387108.

[13] J. Li, J. Zeng, Y. Yuan, D. He, J. Fan, C. Tan, and Z. Yu, "Analysis and design of a 2-40.5 GHz low noise amplifier with multiple bandwidth expansion techniques," IEEE Access, vol. 11, pp. 13501-13509, 2023, doi: 10.1109/ACCESS.2023.3243090.

[14] J. Jeong, S. Kim, S. Lee, and J. Han, "Calibration-free blocker rejection broadband CMOS low noise amplifier for advanced cellular applications," IEEE Access, vol. 11, pp. 7739-7750, 2023, doi: 10.1109/ACCESS.2023.3238365.

[15] M. A. S. Bhuiyan, M. R. Hossain, M. S. K. Hemel, M. B. I. Reaz, K. Nisa'Minhad, T. J. Ding, and M. H. Miraz, "CMOS low noise amplifier design trends towards millimeter-wave IoT sensors," Ain Shams Eng. J., vol. 15, no. 2, p. 102368, 2024, doi: 10.1016/j.asej.2023.102368.

[16] M. A. S. Bhuiyan, "CMOS series-shunt single-pole double-throw transmit/receive switch and low noise amplifier design for internet of things based radio frequency identification devices," Informacije MIDEM, vol. 50, no. 2, pp. 105-114, 2020, doi: 10.33180/InfMIDEM2020.203.

[17] Ben Hammadi, M. A. Doukkali, P. Descamps, and C. Niamien, "A 26–28 GHz, Two-Stage, Low-Noise Amplifier for Fifth-Generation Radio Frequency and Millimeter-Wave Applications," Sensors, vol. 24, no. 7, p. 2237, 2024, doi: 10.3390/s24072237.

[18] M. K. Hedayati, A. Abdipour, R. S. Shirazi, C. Cetintepe, and R. B. Staszewski, "A 33-GHz LNA for 5G wireless systems in 28-nm bulk CMOS," IEEE Trans. Circuits Syst. II: Express Briefs, vol. 65, no. 10, pp. 1460-1464, 2018, doi: 10.1109/TCSII.2018.2859187.

[19] D. Fritsche, G. Tretter, C. Carta, and F. Ellinger, "Millimeter-wave low-noise amplifier design in 28-nm low-power digital CMOS," IEEE Trans. Microwave Theory Techn., vol. 63, no. 6, pp. 1910-1922, May 2015, doi: 10.1109/TMTT.2015.2427794.

[20] L. Zhang, N. L. Nguyen, J. Chen, O. Momeni, and X. Liu, "A 3.2 mW 2.2-13.2 GHz CMOS differential common-gate LNA for ultra-wideband receivers," in 2022 IEEE/MTT-S International Microwave Symposium-IMS 2022, pp. 715-718, Jun. 2022, doi: 10.1109/IMS37962.2022.9865626.