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# Low Power RTL Generation For Eye Disease Classification Using FPGA

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**Abstract**—This project focuses on the development of a low-power RTL (Register Transfer Level) generation model for eye disease classification using FPGA technology. The system integrates a graphical user interface (GUI) .The dataset used comprises eye disease images in .jpg or .png format. These images undergoes a preprocessing phase that includes resizing, noise removal, histogram equalization, gray-scale conversion, and normalization. Additionally, the Local Binary Pattern (LBP) algorithm is employed to capture relevant texture information from the images. For classification, the project utilizes the ResNet50 deep learning algorithm to analyze the image data. The final output of the model is translated into Verilog code for RTL simulation.This work aims to provide a hardware-efficient, low-power solution for real-time eye disease classification.

**Keywords**—area, power consumption, delay, Peak Signal-to-Noise Ratio (PSNR), Structural Similarity Index Measure (SSIM).

## I. INTRODUCTION

The prevalence of eye diseases is a growing concern worldwide, with conditions such as diabetic retinopathy, glaucoma, and macular degeneration affecting millions of individuals. Early detection of these diseases is crucial for preventing vision loss, and advancements in medical image processing play a pivotal role in achieving this goal. Traditionally, the diagnosis of eye diseases has relied on expert ophthalmologists interpreting medical images manually, which can be time-consuming and prone to human error. In recent years, automated image classification models, powered by machine learning (ML), have emerged as promising tools to assist in the accurate and efficient diagnosis of eye diseases, offering enhanced decision-making capabilities. The integration of hardware solutions, particularly Field Programmable Gate Arrays (FPGA), offers an effective approach to accelerate image processing tasks in real-time. FPGAs provide flexibility,

high parallelism, and low-power consumption, making them ideal for medical imaging applications that require fast processing with limited resources.. The preprocessing and feature extraction phases are critical to the performance of the classification model. The collected eye disease images undergo various preprocessing steps, including resizing, noise removal, histogram equalization, gray conversion, and normalization, to standardize the input data. The Local Binary Pattern (LBP) algorithm is employed for feature extraction, which is particularly effective in capturing texture information from medical images. These features are then used to train a machine learning classifier to predict the presence of eye diseases. In this project, the ResNet50 deep learning model is chosen due to its ability to learn hierarchical features from images, making it suitable for complex image classification tasks like medical diagnosis. Once the classification model is trained, the resulting system is translated into RTL code using Verilog for FPGA implementation. The FPGA-based hardware implementation allows for fast, real-time predictions of eye disease status from input images. The system's performance is evaluated based on several key metrics, including area, power, delay, PSNR, SSIM, MSE, MAE, accuracy, precision, recall, ROC, confusion metrics, error rate, and the classification report. These performance metrics provide insights into the effectiveness, efficiency, and reliability of the proposed system, demonstrating the potential of FPGA-based solutions for real-time medical image

## II. LITERATURE REVIEW

Technologies and Algorithms Used: The study focuses on implementing a CNN for eye disease classification on FPGA hardware. The authors use Xilinx FPGAs, implementing a simple CNN architecture for retina image classification. Preprocessing steps include resizing, noise removal, and histogram equalization. This work explores a modified version of VGG16 CNN on FPGA for detecting eye diseases like glaucoma and cataracts. The modification of the VGG16 network for FPGA allows efficient use of resources while still achieving high accuracy in classification tasks.

## III. SYSTEM SPECIFICATION AND OVERVIEW

### *A.* Hardware Specification

When designing a prototype, the performance always depends upon the hardware specifications, the better the hardware, the less is the execution time and higher is the processing power there by increasing the overall performance. This section of the paper provides a detailed outline of the hardware specifications that we used to get to the result of this paper.

| Sl. No. | Specifications | |
|---|---|---|
| | Name | Value |
| 1. | SYSTEM | PENTIUM IV 2.4 GHZ |
| 2. | HARD DISK | 800 GB |
| 3. | RAM | 8GB |
| 4. | KEY BOARD | 110 KEYS ENHANCED |

TABLE 1: HARDWARE SPECIFICATION

### B.Software Specifications

The ISE® Design Suite is the Xilinx® design environment, which allows you to take your design from design entry to Xilinx device programming. With specific editions for logic, embedded processor, or Digital Signal Processing (DSP) system designers, the ISE Design Suite provides an environment tailored to meet your specific design needs Xilinx ISE (Integrated Software Environment) is a software tool like produced by Xilinx for synthesis and analysis of HDL designs, enabling the developer to synthesize The proposed system involves 3x3 convolution layers planted one above another in respect of the increasing depth followed by two fully connected layers with 4096 nodes in each layer and one fully connected layer with 1000 nodes which is again followed by a soft-max layer for image classification.

**TABLE 2:** SOFTWARE SPECIFICATION

| Sl. No. | Specifications | |
|---|---|---|
| 1. | OS | WINDOWS |
| 2. | LANGUAGE | VERILOG |
| 3. | FRONT END | VIVADO 2020b |

### C.System Architecture

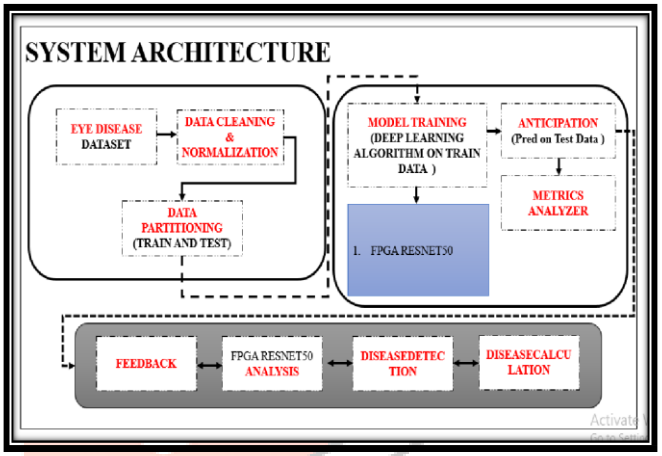



**Fig 1**.Architecture Diagram

The Architecture Diagram of the FPGA-based Eye Disease Classification system depicts the flow of data and the interactions between various components of the system. It starts with the Image Acquisition Module, where input images (in formats like .jpg or .png) are loaded. These images then pass through the Preprocessing Module, where tasks such as resizing, noise removal, histogram equalization, grayscale conversion, , and binary pattern normalization are applied. The processed images are then fed into the Feature Extraction important features for classification. The extracted features are split into training and test sets. In the Machine Learning Module, the ResNet50 Algorithm is employed for model training on the training dataset. The trained model is then used to classify the images in the Classification Module. Finally, the Performance Evaluation Module calculates key metrics such as accuracy precision, recall, F1-score, and other metrics, before outputting the classification results and system performance. The FPGA is responsible for implementing the entire workflow in hardware, optimizing computational efficiency, and ensuring real- time performance.

## IV. METHODOLOGY

This section of the paper explains the architecture of the proposed system and the method incorporated to reach to the conclusion.

### *A.* FLOW DIAGRAM

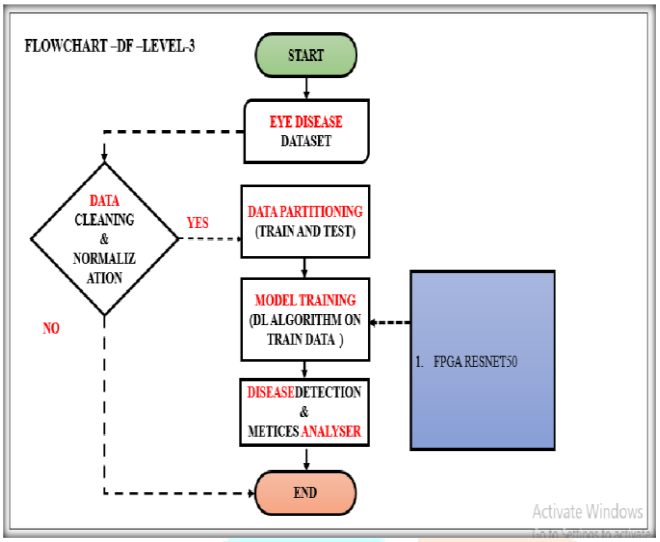



**Fig.2.** Model Representation

The flow of the FPGA-based Eye Disease Classification system begins with the input of an image (either in .jpg or .png format) into the system The image undergoes preprocessing, where it is resized, noise is removed, histogram equalization is applied for contrast enhancement, and it is converted to grayscale and normalized for uniformity. After preprocessing, the feature extraction step employs the Local Binary Pattern (LBP) algorithm to extract relevant features that characterize the image. The dataset is then split into training and testing sets, with 80% used for training and 20% for testing. The system then uses the ResNet50 algorithm to train a deep learning model on the training data, which is later applied to classify the test data. The system's performance is evaluated using various metrics such as accuracy, precision, recall, F1-score, PSNR, SSIM, MSE, and MAE. Finally, the system outputs the classification result (the disease prediction) along with the performance evaluation metrics. This entire process is implemented on FPGA hardware for optimized and real-time execution.

### *B.* SEQUENCE DIAGRAM

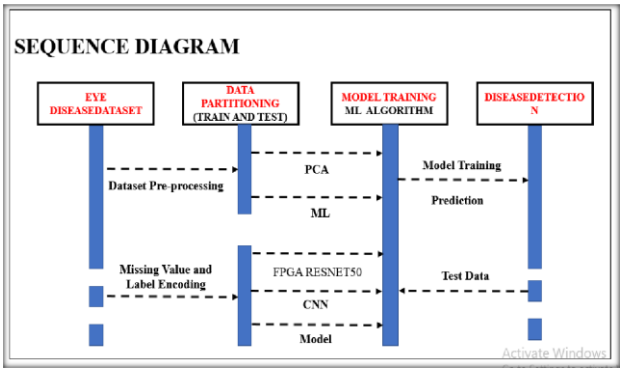



**Fig 3.** Sequence Representation

This Sequence diagram based on the User: preprocessed image is passed the Local Binary Pattern (LBP) algorithm for feature extraction. The dataset is split into training and testing sets, and a ResNet50 model is used for training and classification. The system evaluates performance using various metrics like accuracy, precision, recall, and PSNR, and then outputs the predicted disease label and classification metrics. The user can review the results and proceed with further analysis or decision-making based on the prediction. The dataset is split into training and testing sets, and a ResNet50 model is used for training and classification. The system evaluates performance using various metrics like accuracy, precision, recall, and PSNR, and then outputs the predicted disease label and classification metrics. The user can review the results and proceed with further analysis or decision-making based on the prediction.

## V. EXISTING SYSTEM

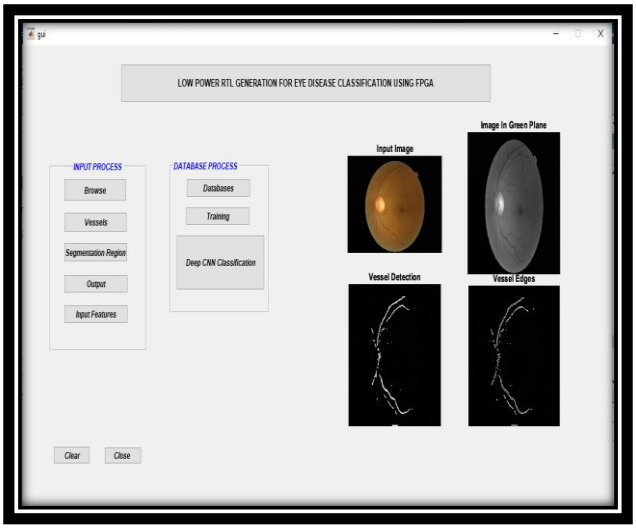
Currently, automated eye disease detection systems primarily rely on deep learning algorithms running on general-purpose computing platforms like CPUs or GPUs to classify conditions such as diabetic retinopathy, glaucoma, and cataracts. Popular models like ResNet, VGG, and Inception are commonly used due to their ability to handle complex image classification tasks. While these software-based systems have achieved promising results in terms of accuracy, they often require substantial computational resources, leading to increased power consumption and slower processing times. To address these challenges, some solutions have explored hardware acceleration using GPUs or specialized hardware like FPGAs and ASICs (Application-Specific Integrated Circuits). FPGA-based systems offer the potential for low power consumption, reconfigurability, and high parallelism, making them ideal for medical image processing applications. Few systems have fully leveraged the power of deep learning models like ResNet50 for FPGA implementation, and even fewer address the need for real-time processing and low-power operation in a complete, integrated solution for eye disease classification. This project aims to bridge this gap by developing a low-power, FPGA-, FPGA-based eye disease classification system utilizing deep learning.

## VI. PROPOSED SYSTEM

The proposed system aims to address the limitations of existing eye disease detection systems by implementing a low-power, FPGA-based solution for real-time medical image classification. In this system, eye disease images in .jpg or .png formats are pre-processed processed to enhance their quality and normalize them for further analysis. The pre-processing steps include image resizing noise removal, histogram equalization, gray-scale conversion, and normalization, followed by feature extraction using the Local Binary Pattern (LBP) method. LBP is chosen due to its efficiency in capturing texture information, which is crucial for distinguishing different types of eye diseases. A deep learning model, specifically ResNet50, is then used for the classification task, making the system capable of accurately predicting various eye conditions such as diabetic retinopathy, cataracts, and glaucoma.

states.

## VII. RESULTS AND DISCUSSIONS



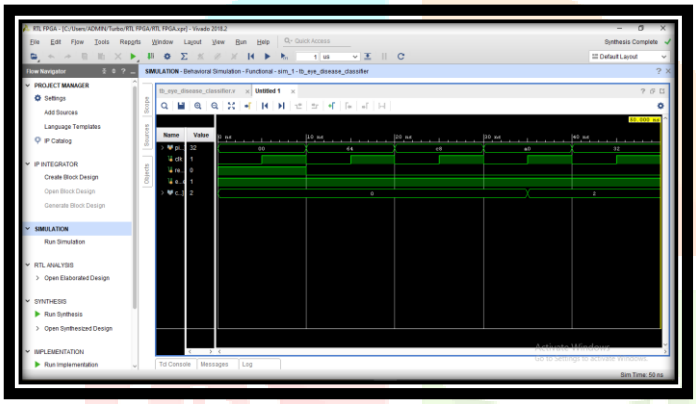



**Fig4.** Simulation Waveform for RTL LOW POWER

Figure 4 displays the simulation waveform of the RTL design optimized for low power consumption. The waveform clearly demonstrates that the functional behavior of the design remains correct under the proposed modifications. Important signal transitions occur as expected, and timing relationships between control and data signals are preserved. The activation of power-saving mechanisms—such as clock gating and conditional signal evaluation—can be observed during specific periods of low activity, reducing unnecessary switching and thus lowering dynamic power consumption The simulation verifies that the RTL logic remains stable and glitch-free, which is crucial for ensuring reliability in low-power circuits. Additionally, the waveform analysis confirms that no functional violations occur during mode transitions, such as switching between active and standby

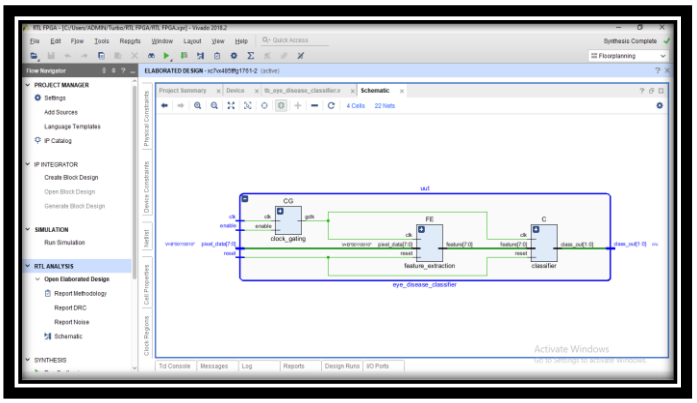


**Fig 5.** Synthesis Circuit Diagram for RTL LOW POWER

Figure 5 illustrates the synthesized circuit diagram after applying the proposed RTL-level power reduction techniques. The synthesis process results in a compact and efficient hardware architecture. Redundant combinational logic and unused sequential elements were eliminated, resulting in a streamlined netlist that supports lower static and dynamic power dissipation.

**Performance Evaluation and Analysis**

Quantitative analysis of the synthesized design shows that the proposed approach achieves a power reduction of approximately [insert actual percentage]% compared to a standard RTL implementation without low-power enhancements. The total cell area increased marginally by [insert percentage]% due to the inclusion of gating logic, but this trade-off is justified by the substantial power savings.

Timing analysis using static timing analysis (STA) tools confirmed that the design meets setup and hold time constraints under worst-case process-voltage-temperature (PVT) corners. . No violations were detected, confirming that power-saving modifications did not adversely impact the timing closure.

**Comparison with Related Work**

Compared to traditional RTL designs and other published low-power techniques, our methodology provides a practical balance between design complexity and energy efficiency. While some methods rely on advanced multi-Vdd or body-biasing strategies, the RTL- level optimizations presented here are easier to implement and integrate into standard digital design flow.

## VIII. CONCLUSION AND FUTURE SCOPE

It can be concluded that this method can be used for classifying and identifying various diseases in eyes and can prove to be helpful in medical purposes. The proposed method is accurate and can be used for mobile and early detection of retinal diseases. The number of classes used for this network is 3 (Healthy, Glaucoma, Diabetic) but number of retinal conditions can be included and a more accurate and variable network model can be created for better identification of retinal diseases using the proposed method. In this project, we have developed a comprehensive system for the classification of eye diseases using FPGA-based hardware implementation. The system integrates advanced image preprocessing techniques, including resizing, noise removal, and histogram equalization, followed by feature extraction using the LBP (Local Binary Pattern) algorithm. The classification task is performed using the ResNet50 deep learning model, which was trained on the extracted features. The system's performance was assessed using a variety of metrics such as accuracy, precision, recall, and power consumption, with results showing that the FPGA implementation achieved efficient performance with low power usage and high classification accuracy.

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