



Approximate Pruned and Truncated Haar Discrete Wavelet Transform VLSI Hardware for Energy-Efficient ECG Signal Processing

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Abstract: Approximation computing emerged as a key option for balancing the need for accuracy with the need to use as little energy as possible. Some programmes, like multimedia and signal processing, can handle errors and still process information correctly. This means that the accuracy level is lower than what is required at the circuit level, but the service quality is still good enough at the application level. Automatic recognition of R-peaks is the first and most important step that an electrocardiogram (ECG) signal must go through before it can be processed and analyzed. As its name suggests, the Haar discrete wavelet transform (HDWT) is a simple pre-processing filter that works great for finding electrocardiogram (ECG) R-peaks in embedded systems with very little power, like wrist tech. A study is used to show an approximate HDWT hardware architecture for ECG processing that is very good at using energy efficiently. Our best choice, which includes pruning in the roughly HDWT hardware design, only needs seven extra things to be added. In addition, this article looks at how to use a truncation method to make things use less energy. This is done by looking at how the signal-to-noise ratio changes over time and how that affects the ECG peak-detection programme in the end. According to the findings of this study, our HDWT approximation hardware architecture proposal is capable of bearing larger truncation levels than the HDWT that was first developed. Finally, our results show that using our HDWT matrix approximation idea along with pruning and the highest level of truncation still achieves an average R-peak recognition performance accuracy of 99.68%. This results in a decrease of approximately nine times the amount of energy that was previously consumed.

Index Terms - Haar DWT, Energy-Efficient, ECG.

I. INTRODUCTION

Edge computing, which is powered by artificial intelligence, has placed complicated processing units closer to the source of the data, which has negatively impacted their autonomy [1]. Making processing more energy-efficient is something that needs to be done because processing data on edge devices is getting more involved and needs a lot of power.

Object detection in computer vision is a difficult job that involves figuring out where things are and what kind of things they are [2,3]. This helps you fully understand a picture, which is why it's important. Some of the things that standard object detection models do are pick out useful areas, pull out features, and classify objects. On the other hand, over the course of the past ten years, deep neural network-based detection models have emerged as the most advanced methods for object detection [4]. These models combine the process described above and are trained on enormous databases of photos that have been labelled.

It is still a difficult challenge to detect small, fast-moving things like honeybees, where processing speed plays a key role, notwithstanding the recent advancements that have been made in this area. In [5], several different methods were suggested as ways to find honeybees and pollen loads and keep an eye on the beehive's health. A video that was acquired by unmanned aerial vehicles was used by the authors of [6] to propose a system for the autonomous monitoring of honeybee activity that occurred outside of the hive. To track the severity of a Varroa destructor mite infestation, the authors of a recent study [7] suggested a mobile computer vision system that could record a video stream of honeybees. As a last point, the discovery of Varroa destructor mites on honeybees was made possible by the first use of deep neural network object detectors implemented on graphics processing units in a recent study [8]. None of these systems, however, involved constant monitoring in close proximity to beehives; rather, they all depended on offline analysis of the recorded images or videos. This monitoring was typically carried out without a power source, and it was only performed by a device that ensured long-term autonomy.

Electrical dipoles are produced by the heart. As each beat passes, the dipole's intensity and direction undergo a shift. The different ECG leads that are used to gather the information are a reflection of these variations. By analyzing the performance of the heart and identifying any potential irregularities, the signal waveform on these leads is utilized. ECG waveforms that are aberrant are distinguished from those that are usual by these distinctive characteristics. One symptom of ventricular fibrillation is a big QRS complex and the lack of P waves. In contrast, an appreciable PR interval and a normal QRS complex are hallmarks of atrial fibrillation. First-degree AV blocks are characterized by a normal QRS frequency that is more than 0.20 seconds.

II. PROBLEM DESCRIPTION AND FORMULATION

Various techniques for detecting cardiac abnormalities are included in survey publications by [9]. Methods might be either based on hardware improvements or on enhanced software processing. Established a hierarchical probabilistic system with multichannel capabilities for foetal ECG R-peak detection via predictive modelling. Efficient processing of electrocardiogram (ECG) signals with R-peak detection maintained is suggested utilising the Haar-DWT hardware architecture. Used the SPH database to evaluate a number of machine learning models for classifying data.

There has been a lot of research on using wavelets for signal processing. When processing signals in the time-frequency domain, wavelets are employed to preserve the signal's important characteristics.

To find the R-peak, the authors of [10] employed a wavelet transform in conjunction with a tweaked Shannon energy envelope. Talk about how to use wavelet denoising and support vector machine classification to find late ventricular potentials. Following the suggested methodology, this study use wavelets to correct baseline wander in ECG data while maintaining frequency information.

Those models aren't going to work on Internet of Things devices because they typically require a powerful computer. Several offloading strategies have been suggested for Internet of Things devices to address the problem of computing efficiency. Partial offloading and distributed Mobile Edge Computing are two of the many architectures that have been investigated. Distributed intelligence models and an Internet of Things (IoT) fog cloud architecture were also proposed to optimise offloading efficiency. When transmitting relatively large amounts of data, however, these designs are generally inefficient [11].

One open-source deep learning framework that can be used for inference on the go is TensorFlowLite [12]. As wireless technology continues to expand, more and more applications are being explored for Internet of Things (IoT) devices. This calls for sophisticated deep learning models to be implemented on embedded and edge devices. The TensorFlow/Keras stored model is transformed into a FlatBuffer using TensorFlowLite. Flatbuffer is a library for serialisation that works on Python, C++, C, Java, and C++. A lot less power is required to run the Flatbuffer. The size of the model is reduced via quantization optimisations throughout the conversion process. Flatbuffers have the advantages of being tiny, adaptable with different platforms, and efficient with memory. Perfect for low-power Internet of Things devices, they don't require parsing or unpacking

III. METHODOLOGY

An electrocardiogram (ECG) is a typical test that records the electrical activity of the heart over a certain amount of time. It is feasible to gauge the cardiac muscles' electrical activity with this test. Using this, patterns can be identified and a variety of cardiac ailments, including congenital heart disease, conduction issues, pericarditis, arrhythmia, and coronary obstruction, can be diagnosed. The V0 function space is home to the signal X_n seen in Figure 1. Coefficients of detail (d_1) and approximation (a_1), which belong to spaces W_1 and V_1 , respectively, are obtained by downsampling the input signal by a factor of 2 in the low-pass (HL) and high-pass (HH) stages. The WT is also applied to the approximation coefficients of V_1 , resulting in the signals of d_2 and a_2 , which are members of the subspaces W_2 and V_2 , respectively. When the required wavelet scale is reached, the process is repeated.

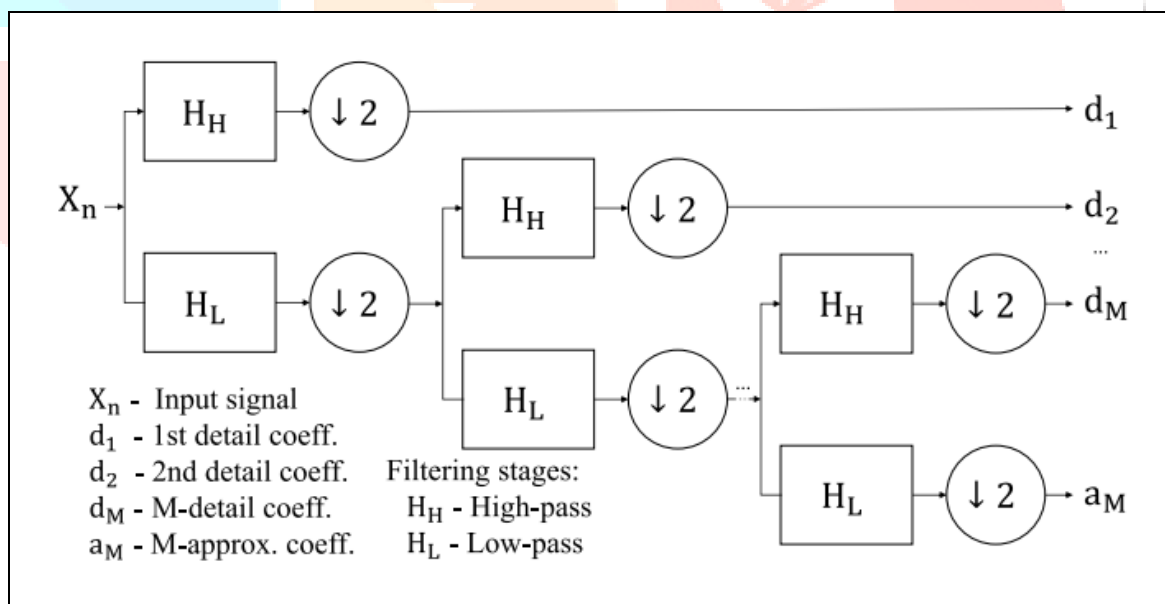


Fig. 1. DWT filter bank with M levels.

In Figure 2, we can observe that the parameter k , which represents the degree of truncation, influences the bit-width reduction of HDWT designs. Additionally, we explore in this study the upper limits of k that are consistent with HDWT's high-quality R-peak detection.

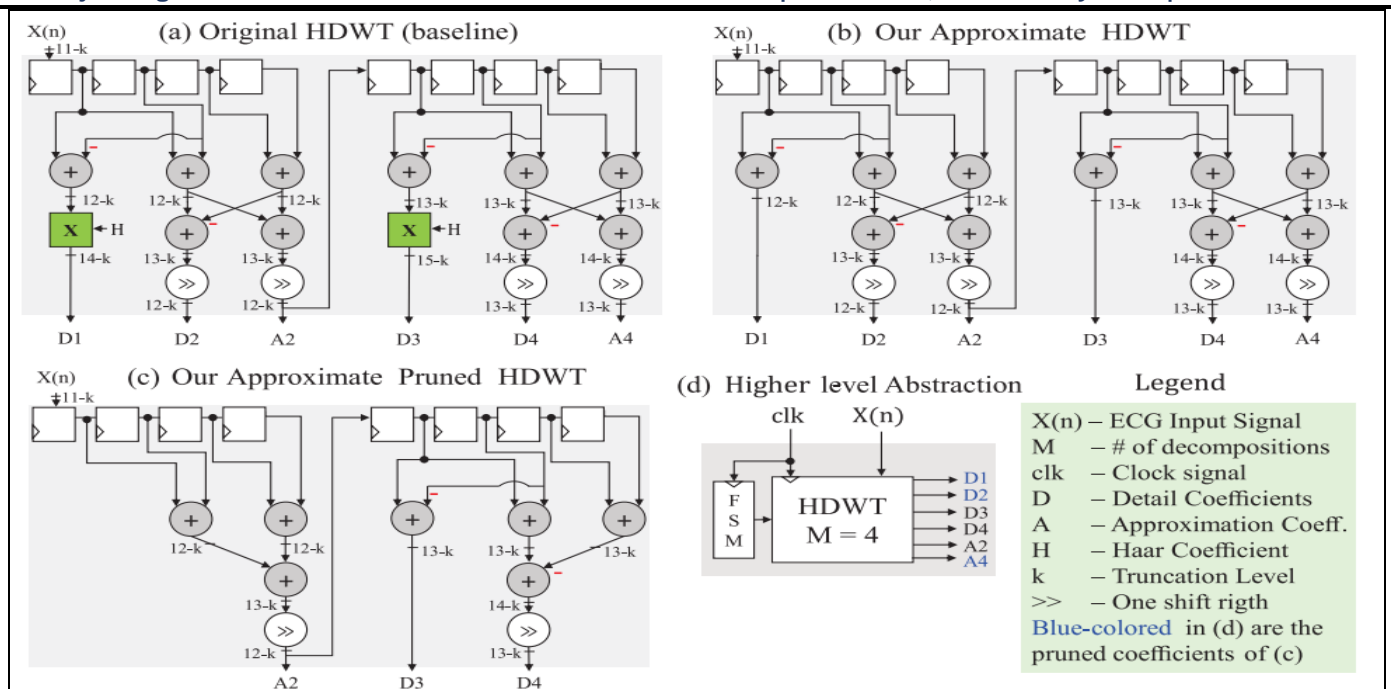


Fig. 2. a) The default HDWT, b) Our approximation of the original, c) Our approximation of the pruned version, and d) A bird's-eye perspective. K is the depth-propagated truncation level used in the datapath of the architecture and represents the input signal.

IV. RESULTS AND DISCUSSIONS

The A-HDWT hardware architecture's SNR surpasses that of the O-HDWT at the 5-bit truncation, as seen in Figure 3.

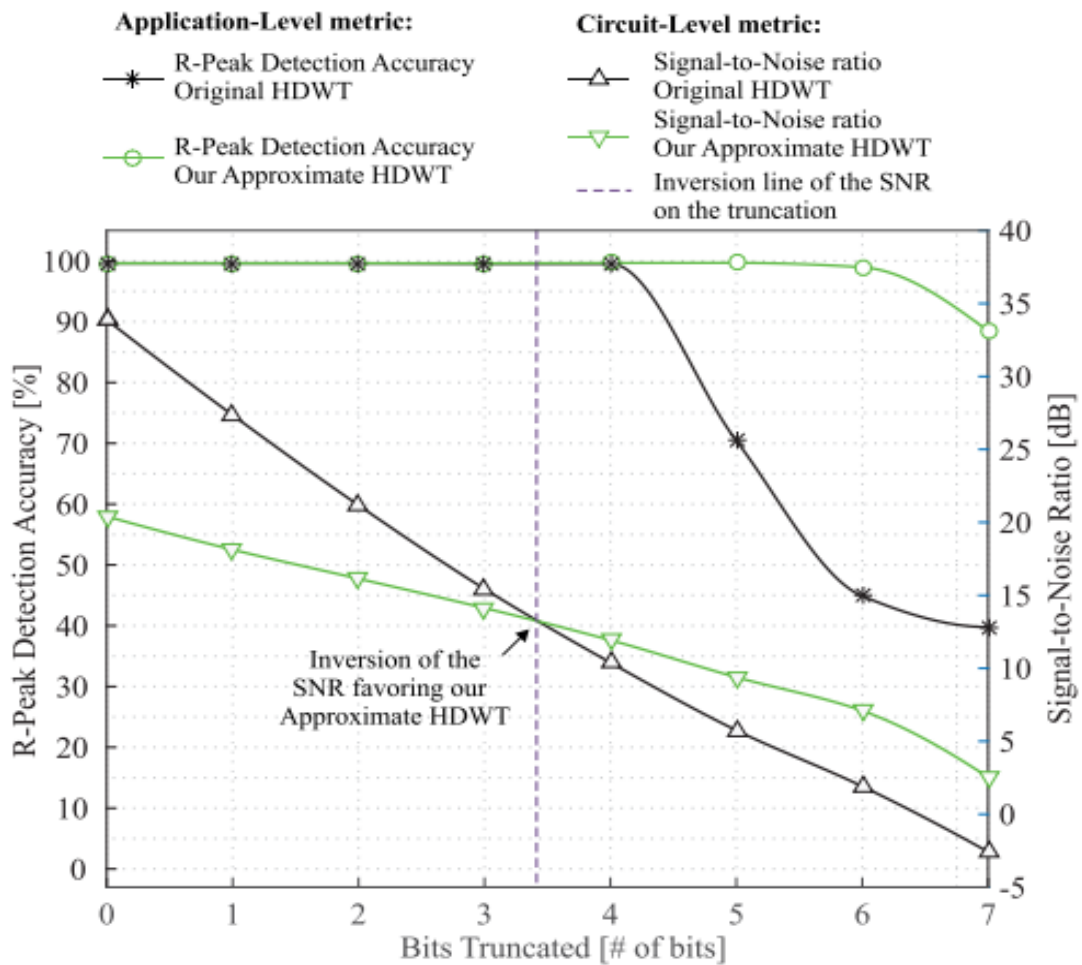


Fig. 3. Comparison of the original HDWT (O-HDWT) with the approximation HDWT (A-HDWT) strategy for truncation



Fig .4. RTL Schematic of Approximate BrentKung Adder



Fig.5. RTL Schematic of Approximate KoggeStone Adder

Brentkung and koggestone adder RTL is shown in figure 4 and figure 5.

V. CONCLUSION

An estimated pruned and truncated HDWT was presented in this study as hardware architecture for energy-efficient processing of electrocardiogram (ECG) signals. We achieved a considerable reduction in bit-width and arithmetic operations, an acceptable SNR loss at the circuit level, and achieving the application level's ultimate quality requirements by employing four levels of decomposition and approximation in the original HDWT matrix. We proposed an approximation pruning HDWT matrix that enabled a multiplierless design to be implemented with only seven additions. The consequences of datapath truncation in approximation designs were also explored in this work. The proposed HDWT hardware design with a maximum of 5-bit truncation level reduced power dissipation by 9.05 times and circuit area by 5.83 times, while preserving the same level of quality, according to the results of the quality analysis and synthesis. This was done without compromising the R-Peak detection performance.

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