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RTL HDL DESIGN OF TERA HERTZ CLOCK SPEED PRBS GENERATOR OF DIFFERENT SEQUENCE PATTERNS FOR ULTRA HIGH SPEED WIRELESS COMMUNICATION

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Abstract: The paper proposes RTL and HDL design for Tera hertz speed PRBS carrier generator ASIC for Ultra high speed long distance communication Hi-tech Smart computing applications wireless, telecom, satellite, internet and cloud computing, CDMA/GPS, LTE ASIC etc. The design consists PRBS generator generate carrier frequency of different tapped sequences $2e^7$-1, $2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1 and multiplexer. The PRBS generator designed by using LFSR block with above tapped sequences with tapping elements (7,6),(10,3),(14,15),(18,23),(28,31) generates carrier waves in repeated random number frequency sequence format. These carrier sequences are efficiently and effectively modulate and demodulate low frequency base band signal digital binary message information for long distance wireless and communication, satellite applications. The different pattern sequences are designated as per CCITT ITU O.150, O.151, O.152 standards. The soft IP Core Designed by Verilog HDL Languages and design simulation Synopsys 2023 and design flow Implemented by Xilinx ISE 9.2i IDE Software. This PRBS generator mainly suit for latest coming generation New Innovative Low Power Portable Smart Computing Products like I phones, Tablets, Note Book, Pocket Multimedia SOC Computing, GPS Mobile phone Cards, GPRS, and Handheld Instruments etc.

Index Terms **-** LTE ASIC – Long Terminal equipment Application Specific Integrated Circuit, CDMA- Code Division Multiple Access ,GPS – Global Position System, PRBS – Pseudo Random Binary Sequence , Verilog HDL – Verification logic Hardware Description Language.

I. INTRODUCTION

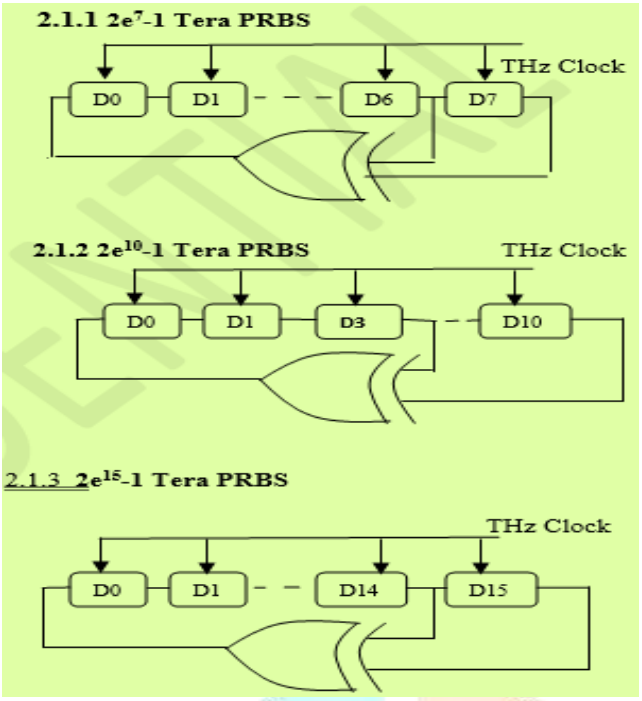
In the latest Modern Hi-tech Information Technology & Communication Engineering world, High speed is a major constraint factor for VLSI chip designs. Now Giga Hertz speed (Gbps) based wireless & communication products came to the market. Now we proposed new Tera hertz clock speed (Tera bits per second baud rate) PRBS carrier generator for all latest new Innovative & future generative Hi-tech Wireless high speed and High performance smart computing products. In Modern Hi-tech Communication Engineering and software world, High Speed based Portable communication system hardware & software products came to the market, speed is an important factor and it is in terms of Giga bits per second for all Hi-tech real time

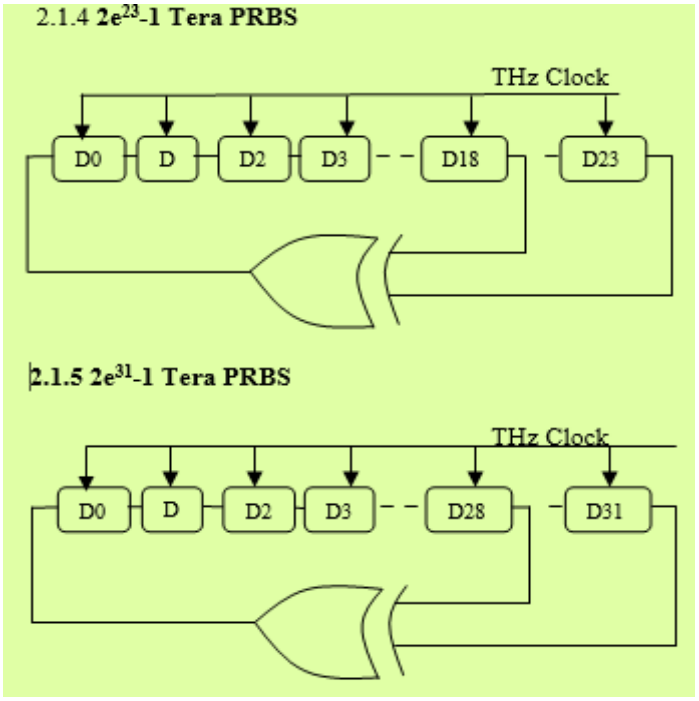
smart computing Portable wireless communication system software Applications. For that purpose, we designed and developed tera bits per second high speed PRBS is Pseudo Random Binary sequence frequency generators, generate & received random frequency data in the form of random frequency numbers of different speed w.r.t specific data tapping sequence points for both signal & carrier wave generation. PRBS Generators, Receivers, Transceivers Designed for HiFi Wireless Internet Data Packets Computing communication etc. Transmission, Reception of Data is in the RANDOM Sense, This PRBS Generator, Receiver is Designed for Identification property of Different Tapped PRBS Sequences like 7, 10,15,23,31 at a clock carrier frequency speed of Tera bits per second. The length of PRBS sequence is 2^L-1. 2^L-1 times repeated the sequences. this is mainly suit for multiple users to transmit and received data in accurate time for very long distance communications like GPS Data Acquisition, GSM Communication Systems, WIFI, GIFI, LTE, Wireless OFDMA , CDMA,QCDMA Computing, wireless internet computing, cloud computing etc. because of Ultra High speed communication transfer packet message speed rate in terms of tera bits per second. All these PRBS LFSR sequences are designed by tapping different points according to ITU O.150, O.151, and O.152 Standards. This PRBS design consists of Multiplexer, PRBS registers of different tapped sequence points, Clock frequency generators of tera bits per second speed. The Advantages of these PRBS Generators having in built Checkers, Bit error rate detection & correction by using PRBS Checkers. these are simply Linear Polynomial Checkers & CRC.

PRBS TYPE	STANDARD	SUGGESTED DATA RATE(Kilo Bits Per Second)	FEED BACK TAP
2^7-1	ITU-T O.150	14.4	7,6
2^{10}-1	ITU-T O.150	64	10,3
2^{15}-1	ITU-T O.150	1544, 2048, 6312, 8448, 32064, 44736	14,15
2^{23}-1	ITU-T O.150	34368, 44736, 139264	18,23
2^{31}-1	ITU-T O.150		28,31
2^{48}-1	ITU-T O.150/151/152		48,42
2^{52}-1	ITU-T O.150/151/152		52,47
2^{63}-1	ITU-T O.150/151/152/153		48,63

Table(1): PRBS bit-pattern are generated in a linear feed-back shift-register. This is a shift-register with a XORed feedback of the output-values of specific flip-flops to the input of the first flip-flop.

II TERA PRBS DESIGN ARCHITECTURES





NOTE:
SIMILARLY FOR 2^{48}-1,2^{52}-1,2^{63}-1 PRBS DESIGN SEQUENCES

2.1 Real Time Tera Hertz Clock Frequency Oscillator

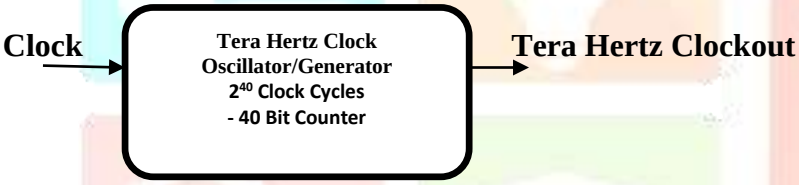
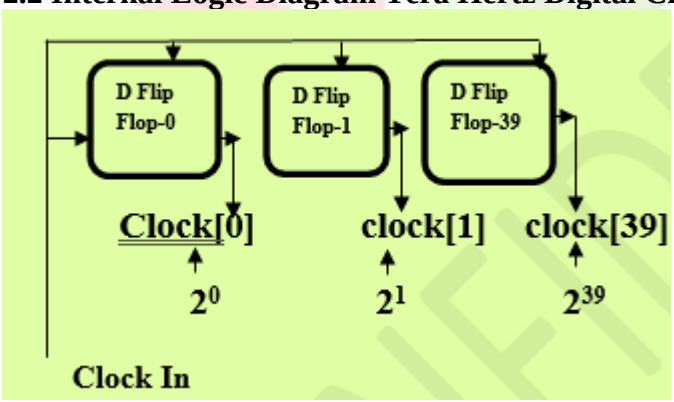
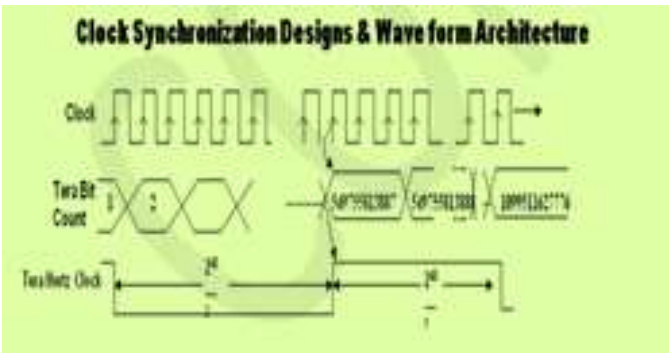


Fig. Tera Hertz Clock Generator/Oscillator ASIC

2.2 Internal Logic Diagram Tera Hertz Digital Clock Oscillator

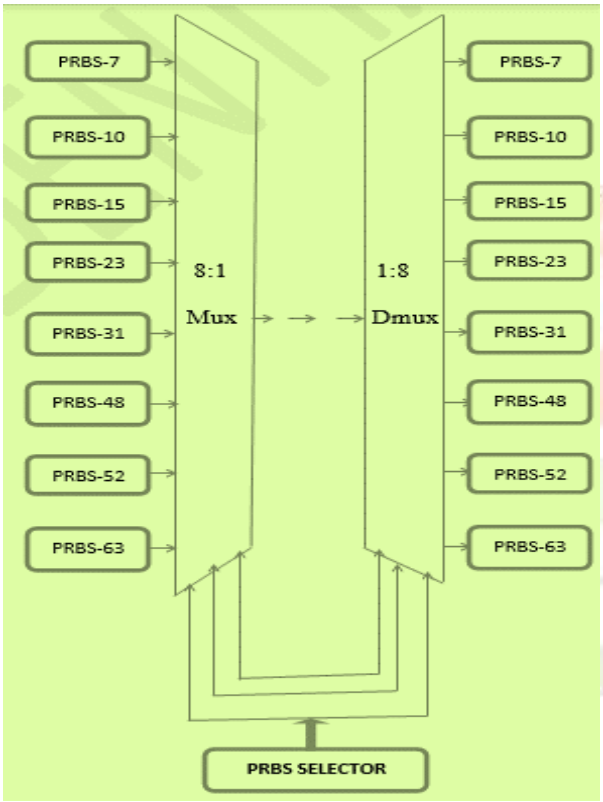


2.3 Tera Hertz Clock Frequency Oscillator Wave Forms



```
`timescale 1ns / 1ps
module teraclockgen(clock,teraclock);
input clock;
output teraclock;
reg teraclock;
reg [39:0]teracount =
40'b0000000000000000000000000000000000
0000000000;
reg clok;
always @(posedge clock)
begin
teracount = teracount+1;
clok = teracount[39];
teraclock = clok;
end
endmodule
```

2.4 HIGH SPEED MULTI CHANNEL MULTI SPEED PRBS DATA SERDES/TRANSCEIVER



FIG(2): PRBS DATA SERIALIZER De-SERIALIZER TRANSCEIVER

2.5 EDA SOFTWARE – VLSI IC DESIGN FLOW

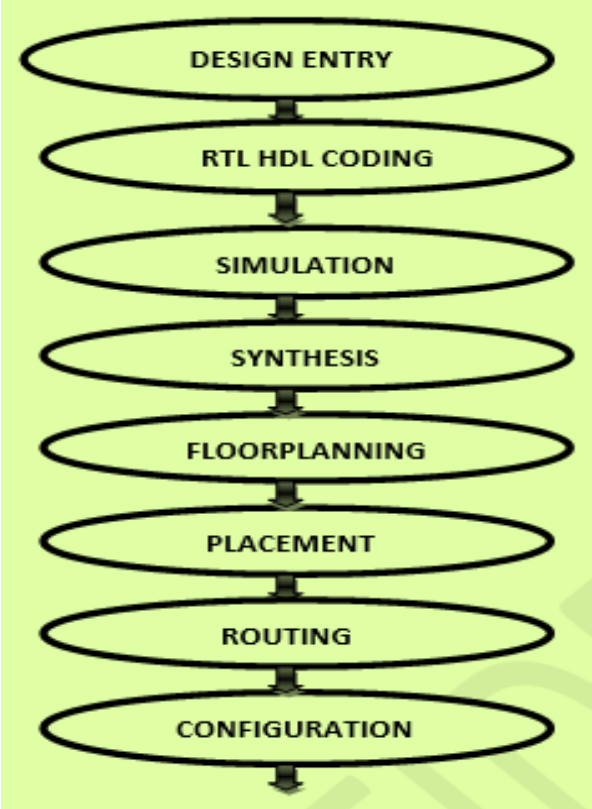
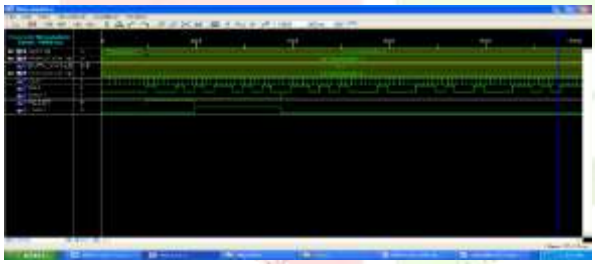


FIG (3): VLSI IC DESIGN FLOW

III RTL DESIGN SIMUALTION

3.1 SIMULATION RESULTS

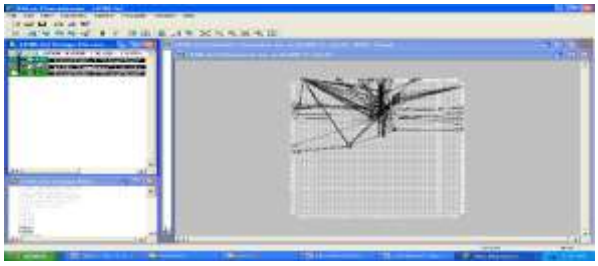


IV RTL DESIGN FPGA SYNTHESIS

4.1 RTL DESIGN ARCHITECTURE

4.2RTL-DESIGN-SCHEMATIC

4.3 FPGA PLACED DESIGN LAYOUT



4.4 FPGA ROUTED DESIGN REPORT

V CONCLUSION

The proposed Tera bits per second ultra High speed PRBS generator generates carrier waves of different deterministic repeated random number frequency patterns of $2e^{7}$-1, $2e^{10}$-1, $2e^{15}$-1, $2e^{23}$-1, $2e^{31}$-1 and the purpose is for long distance wireless signal communication and satellite applications. Why we proposed this because to efficient modulate and demodulate low frequency signal by above PRBS carrier patterns.

REFERENCES

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[2] “ITU-T Recommendations O151, O152 and O153,” Tech. Rep.
[3] SY Hwang, GY Park, DH Kim, KS Jhang, “Efficient Implementation of a Pseudorandom Sequence Generator for High-Speed Data Communications”, ETRI Journal, Volume 32, Number 2, April 2010.