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DESIGN AND DEVELOPMENT OF DYNAMIC COMPARATOR FOR BIOMEDICAL APPLICATIONS USING LTSPICE

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Abstract: In the quickly changing digital world, data acquisition and digitalization becomes imperative. The ADC is the second most widely used type in data acquisition systems. Inside an ADC a dynamic comparator plays a crucial role in digitalization of the input signal. In this work we propose a low power area efficient single tail rail-to-rail dynamic comparator for biological signal acquisition systems. The proposed design consumes 9.032pW of average power under 1 v supply voltage. The area efficiency is achieved by using 11 transistors to implement the full comparator functionality. The schematic was designed and simulated in LT spice XVII tool.

Index Terms - Low Power Dynamic Comparator, ADC, Biomedical Applications

I. INTRODUCTION

A comparator is an electronic device used for decision-making that employs a high-gain operational amplifier. An input voltage level is compared to another using a comparator, voltage level or the VREF, a fixed voltage [1]. Depending on which analog input voltage is greater, it generates a binary output. As the demand for higher resolution, increased sampling rates, and enhanced power efficiency continues to escalate, the design of ADCs has become an area of intense research and innovation. Among the various building blocks that comprise an ADC, the dynamic comparator stands out as a critical component influencing the overall performance and functionality of the converter.

First, dynamic circuit refers to the addition of clocks to the circuit design's input, and this is the case with dynamic regenerative comparators. The clock's current state determines the phases of comparator circuit. Regenerative comparators are those that compare signals by means of positive feedback, such as a latch. Higher speed in the circuit is made possible by the feedback.

A comparator's output is pulled up to +V, as seen in Fig. 1, when the non-inverting terminal is at a greater voltage potential than the inverting terminal. Likewise, the output is pushed down to –V when the inverting terminal is at a greater voltage potential than the non-inverting terminal.

The most common applications for comparators are in analog to digital converters, such as SAR ADC, flash ADCs etc. The main factor affecting the overall performance of ADCs is the comparator design.

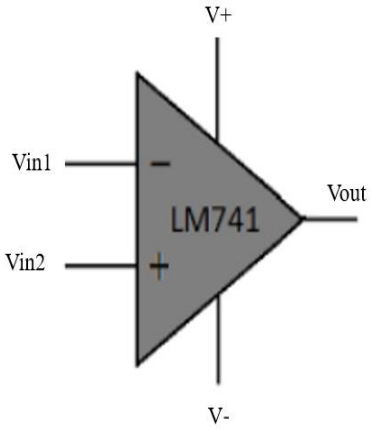

Fig.1 Op-amp in Open Loop Configuration

A compact chip size, high speed, and low supply voltage are essential for any comparator. It becomes necessary to make compensations in the design area in order to achieve the required speed and low power. As a result, the comparator's area and speed are trade-offs that are to be considered while designing.

A comparator consists of three primary stages: the pre-amplifier stage is the first. This step amplifies the input signal that is supplied to the comparator. The subsequent phase is a

stage of efficient positive feedbacking. The primary purpose of this is to determine if the input signal is high or low. The decision-making and output buffer stages are the last ones of comparator stages. In this case, the buffer's primary function is to amplify the information received and generate a digital signal as its output. Input common mode range, power consumption, propagation latency, and chip area are all taken into account while designing a comparator. CMOS dynamic latching comparators are highly desirable for a variety of applications, including memory sense amplifiers (SAs), data receivers, and high-performance analog-to-digital converters (ADCs), because of their fast speed, low power consumption, high input impedance, and full-swing output. Offset voltage is the most crucial design parameter while creating a dynamic latched comparator since it has a significant impact on the comparator's performance.

The high-speed comparator's block diagram, which includes a pre-amplifier and latch stage that regenerates. In addition to amplifying a tiny input voltage difference to a big output voltage, the pre amplifier stage is utilized to lower the latch offset voltage. In order to lessen the kickback noise, the huge output voltages are used to overcome the latch offset voltage. Large bandwidths will result in high static power consumption due to the pre-amplifier stage, and intrinsic gain will also decrease as a result of the drain-to-source resistance (rds). Therefore, a dynamic comparator without a pre-amplifier stage is extremely desirable for high-performance CMOS applications. Numerous accuracy problems, including random offset errors and mismatched internal parasitic or external load capacitances. To resolve these accuracy problems and enhance performance.[2] It is preferable to use dynamic latch-based comparators without a preamplifier stage. Since the pre-amplifier has a large static power consumption, a comparator without one is desirable for a high-performance analog to digital converter.

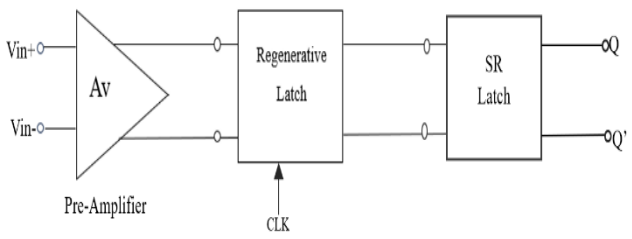

Fig 2. High-speed voltage comparator block diagram

The following sections are taken into consideration in this paper: Part II explains the suggested dynamic latch comparator and how it works, while Part III provides an overview of the proposed comparator and in Section IV various comparators power and the number of transistors was estimated and tabulated, and the work is concluded in Section V.

II. DYNAMIC COMPARATORS

A. EXISTING DYNAMIC COMPARATOR

In the case of dynamic comparators, inputs are compared at different times [5]. A clock or triggered signal is necessary for these comparators. Using positive feedback, dynamic comparators increase the reward and are forced to make choices within a constrained time frame. The dynamic comparator, which has a high input impedance, rail-to-rail output swing, and no static power consumption, is a straightforward comparator used in ADCs. The schematic design is displayed in Fig. 1 for the traditional dynamic comparator.

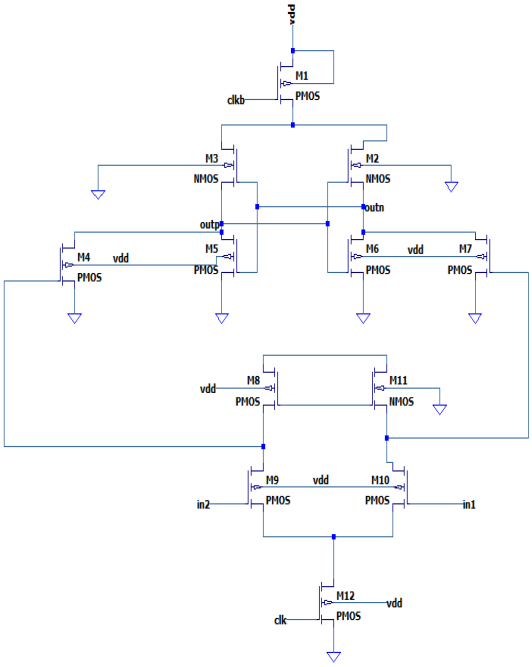

Fig 3. Existing dynamic comparator

When clk=0, the M1 transistor is ON and M12 transistor is OFF. The Outp and Outn nodes are precharged to Vdd through M3 and M2 transistor. When clk=1 the M12 transistor is ON and the inputs that are to be compared are applied to M9 and M10 transistor. If IN2>IN1, transistor M9 conducts more and the Outp node is discharged to 0 at a faster rate compared to Outn node.

This drives Outp node to be high. When IN1>IN2, M10 conducts in a faster manner and Outn node is discharged to 0 and it turns ON the Outp node. In this circuit a complementary clock signal is required, which increases the total clock load of the circuit.

III. PROPOSED DESIGN

An 11- transistor single tail dynamic comparator circuit is shown in fig.4[3]. The entire operation of the circuit is controlled by a global clock signal.

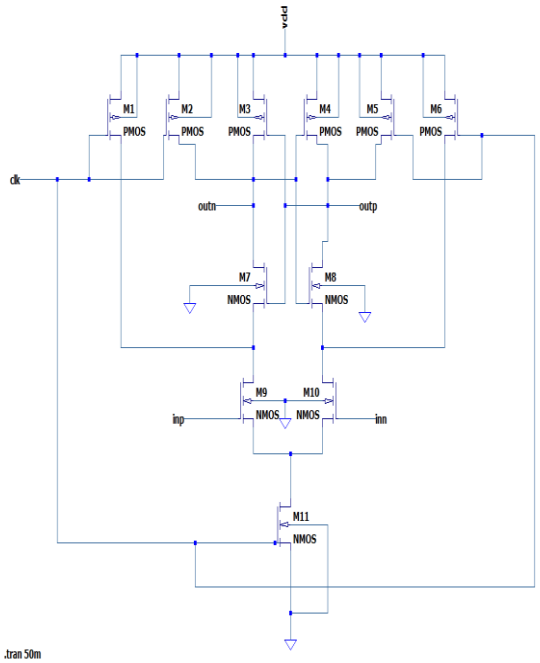

Fig 4. Proposed Circuitry

The operation of the comparator is divided into two phases: initial phase (recharge or pre-set phase) and evaluation phase or decision phase. When the clock signal is 0(clk=0) the PMOS transistors M1, M2, M6 and M5 will become ON. The tail transistor M11 will be OFF. The output nodes Outn and Outp are charged to Vdd(high) through transistors M2 and M5. This condition is known as initial or pre-set phase. To evaluate the input the clock signal is made high (clk=1). These makes the PMOS transistors OFF and it eventually turns ON.

The tail transistor M11 the input signal that are to be compared are applied at the gate terminal of NMOS transistor M9 and M10 respectively.

First consider inp> inn, the transistor M9 conducts heavily than M10, because of more voltage that is being applied at the gate terminal of M9. Similarly, transistor M7 and M8 conducts accordingly and the M7 transistor conduct more than that of M8 and the output node (Outn) discharges to 0. These zero voltages at Outn are coupled to the inverter circuit (combination of M4 and M8 terminal) and the output nodes is charged to

Vdd [4].

On the other hand, if the input inn>inp transistor M8 conduct heavily and eventually the output node is discharged to 0. This low voltage is coupled to the input side of inverter formed by transistors M3 and M7 and the Outn node is charged to Vdd.

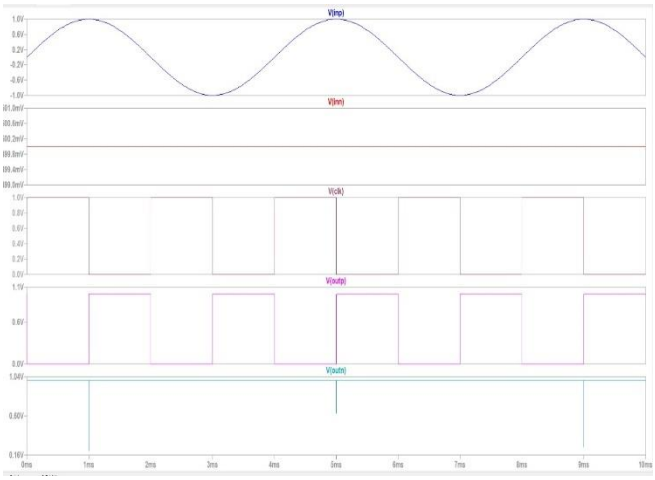

Fig 5. Simulation of the Proposed Design

IV. COMPARISON TABLE

Literature	NO.OF TRANSISTORS	POWER CONSUMED
[5]	12	12.97pW
[6]	12	10.06pW
[7]	19	4.156mW
Proposed	11	9.032pW

V. CONCLUSION

In this paper the average dynamic power of the proposed system is found as 9.032 pW. The proposed design was compared with the existing dynamic comparator designs and was found that the former dissipates the least average power. Moreover, in the proposed design only 11 transistors are used, which imparts area efficiency and thus the proposed design is suitable for low power, area efficient dynamic comparator design for biomedical applications.

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