IJCRT.ORG ISSN : 2320-2882

INTERNATIONAL JOURNAL OF CREATIVE RESEARCH THOUGHTS (IJCRT)

An International Open Access, Peer-reviewed, Refereed Journal

DESIGN AND ANALYSIS OF SQUARE ARCHITECTURE BASED ON VEDIC MULTIPLIER

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ABSTRACT: The squarer architecture is designed to provide low power, speed, and area for all the fields of image processing, animation and signal processing. This paper explains a squarer architecture using a Vedic multiplier and adders. The proposed architecture uses a different adders(CSA, KSA) to increasing the speed and to reduce the power and delay of squarer architecture.The main advantage of this proposed technique is that it focuses on reduced circuit complexity. The proposed method is coded in Verilog language. The square architecture will be performed in Xilinx Vivado 2016.4 version software by selecting the ZED board.

***Keywords* :** Vedic multiplier, square architecture, Carry save adder(CSA), Kogge stone adder(KSA)

I. INTRODUCTION

VLSI involves creating electronic circuits on a single chip or die, which can contain millions or even billions of transistors. The innovation of VLSI has revolutionized the electronics industry, leading to the production of smaller, more powerful, and energy-efficient devices.The need for high-speed processing has been on the rise due to the expansion of computer and signal processing applications. Efficient arithmetic operations are crucial for achieving optimal performance in real-time systems, cryptography, and digital image processing applications. Moreover, the efficiency of multiplication plays a key role in digital signal processing takes such as correlation, filtering, frequency analysis, and image processing. The quest for fast squaring circuits with efficient outcomes has been a longstanding area of interest. Minimizing time delay and power consumption are essential requirements for numerous applications. The Vedic algorithm is one of the algorithms developed to enhance efficiency and reduced costs by simplifying multiplication.

Digital signal processors (DSPs) play a crucial role in various fields. Convolution, Fourier transformations, and other disciplines heavily rely on fast multiplication and squaring operations. Similarly, microprocessors, DSPs, and modern electronic machines greatly benefit from integer multiplication and squaring. These operations are fundamental in mathematics and require more hardware circuitry and execution time compared to addition and subtraction. To enhance this speed of a CPU, arithmetic-coprocessors are necessary as they handle numerical competitions, including multiplications. In today's world, high power computing applications such as image processing, digital signal processing, graphics, and robotics demand significant computing power. For DSP applications, squaring algorithms need to address concerns regarding latency and throughput. Latency refers to the actual delay in computing a function and measures the stability of input devices. The squaring circuit not only exhibits high delay but also contributes significantly to power dissipation. Therefore, minimizing power consumption and reducing delay through various optimization techniques are crucial objectives.

II BACKGROUND AND RELATED WORK

The process of squaring is commonly used in various fields of Engineering and Technology , especially in domain of VLSI Signal Processing. In this regard several approaches to squaring have been suggested in the existing literature.

T. Sravanthi and A. Madhu Planned " FPGA Implementation of Vedic Multiplier and Square architecture" based upon vedhic mathematics. This paper proposes a FPGA implementation of vedhic multiplier design that uses single carry save adder .The proposed design reduce the delay and power consumption compare to other multipliers.

DR, Nagaraju and Shobhana Planned "Design and Analysis of Squaring circuit using various adders". In this paper presents a squaring circuit using different adders. In this project the efficiency of squaring circuit will be analyze to achieve better performance in terms of power, speed and area.

Karabiner sethi and Rutuparna panda planned " An Improved Squaring circuit for binary numbers" . In this paper , a high speed squaring circuit for binary numbers is proposed. High speed Vedic multiplier is used for design of the proposed squaring circuit. The proposed squaring circuit seems to have better performance in terms of speed.

Avinash Jain and Shaheen Khan Planned " Vedic Based squaring circuit using parallel prefix adders". This paper proposes a novel method using Vedic mathematics for calculating the square of binary numbers. The circuit improved by using parallel prefix adder. Parallel prefix adder provide the best delay performance at the expense of large circuit implementation.

R K.Barik, M.Pradhan, and R.Panda Planned "Time efficient signed Vedic multiplier using redundant binary representation," This paper presents a new method of signed digit multiplication. The proposed design is based on Urdhava Tirryagbhyam (UT) sutra Vedic multiplication and it is found to have high speed performance .

S.Jaikumar, M. Karpagam, and L. Raju Planned "A novel approach to implement high speed squaring circuit using ancient Vedic mathematics techniques," This paper represents a better and efficient module of designing the squaring method and this squaring technique reduce the path delay in executing program.

P. S. Kasliwal, B. P. Patil, and D. K. Gautam Planned "Performance evaluation of squaring operation by Vedic mathematics,"In this paper squaring operation is efficient over conventional multipliers that it can save area occupied on chip and also gives the faster computational speed.

Athira.T. S, Divya.R, Karthik.M, "Design of Kogge-Stone for fast addition", In this paper, propose a kogge-stone adder with low power consumption and delay. The Kogge stone adder is fastest adder reduce power consumption and delay in comparision with other conventional logics.

G. Ganesh Kumar, C.Venkata Sudhakar and M.Naresh Babu Planned "Design of High Speed Square by using Vedic Multiplication Techniques",This is a highly modular design in which smaller blocks can be used to build higher blocks. The high speed square algorithm exhibits improved efficiency in terms of speed.

III. EXISTING METHOD

In the Existing method squarer circuit is designed by using Vedic multiplier and Parallel adder. Multiplier is a major block in designing digital circuits. The 4-bit Vedic multiplier based on ancient Indian Vedic mathematics sutra and the Vedic method of multiplication difference in the conventional method[6]. One of the main benefit of this technique it can be easily extended to handle larger number of bits by breaking them down into smaller components and it is also implemented in the circuit easily.The result of the circuit demonstrate that the implemented squaring circuit are more efficient in terms of delay.

2-bit Multiplier

2-bit multiplier which consists of one and gate and two half adder blocks as shown in figure1.here the two inputs are [1:0] a, [1:0] b and the outputs are [3:0] p.

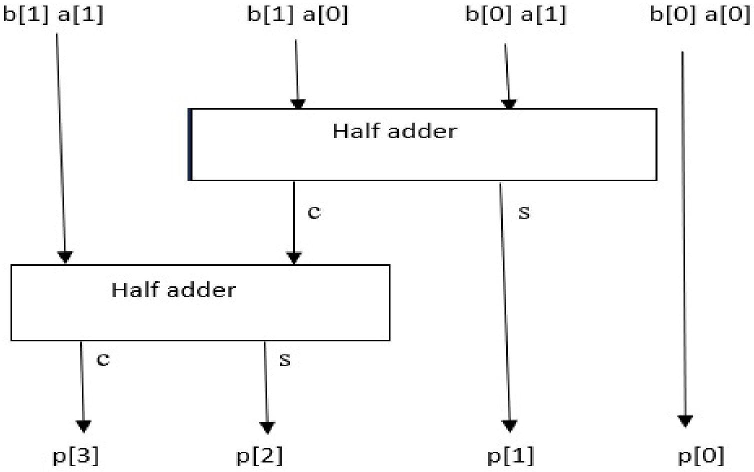

Figure 1. 2- bit Multiplier

The outputs are

P[0] =a[0]&b[0].

P[1] = Sum of first half adder = (a[1]&b[0]) EXOR (a[0]&b[1]).

The carry of first half adder is given to the input of second half adder.

P[2] = Sum of second half adder = ((a[1]&b[1]) EXOR((a[1]&b[0]) &(a[0]&b[1])).

P[3] = carry of second half adder = ((a[1]&b[1]) &((a[1]&b[0]) &(a[0]&b[1])).

2-bit squarer circuit

When both inputs of a 2- bit multiplier are set to the same number (a=b) a 2-bit squarer circuit can be generated.

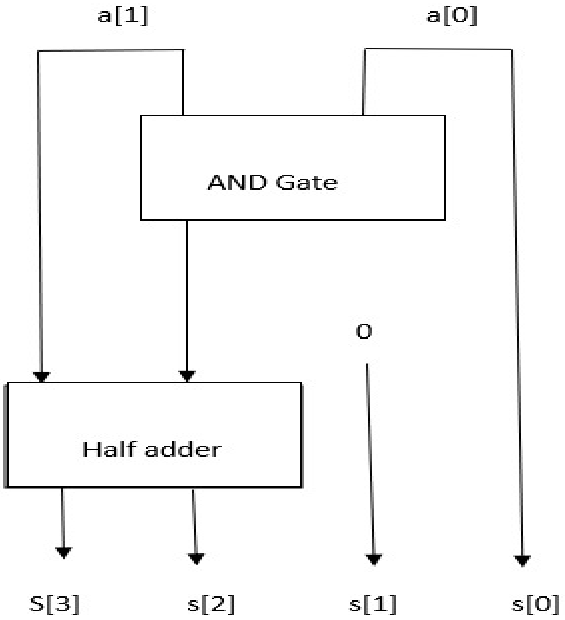

Figure 2. 2- bit Squarer circuit

The outputs are

P[0]= s[0] = a[0]&a[0] = a[0].

P[1] = s[1] = Sum of first half adder = (a[1]&a[0]) EXOR (a[0]&a[1]).= 0

The carry of first half adder is given to the input of second half adder.

P[2] = s[2] = Sum of second half adder = ((a[1]&a[1]) EXOR((a[1]&a[0]) &(a[0]&a[1])) = (a[1] EXOR (a[1] &a[0])).

P[3] = s[3] = carry of second half adder = ((a[1]&a[1]) &((a[1]&a[0]) &(a[0]&a[1])) = (a[1] & (a[1] &a[0])).

4-bit Vedic Multiplier

The block diagram of 4-bit Vedic multiplier shown in figure 3. [3:0] a and [3:0] b are the given inputs and produce 8-bit output [7:0] y. Vedic multiplier as one of the fastest and low power multiplier .Vedic multiplier deals with arithmetic operations. In this multiplier the product bits are added by using the carry save adder. Carry Save Adder is used for high-speed addition of multiple binary numbers. It works by first saving the individual bits of each number and then combining them in a parallel to produce the final result.

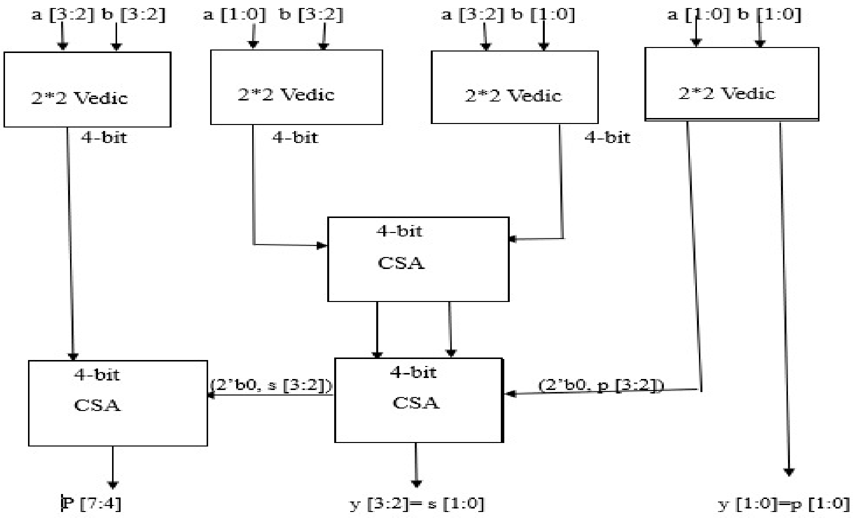

Figure 3. 4 - bit Vedic multiplier

IV.PROPOSED SYSTEM

The proposed system can be designing a 16-bit square architecture which can be used for Vedic multiplier with carry save adder and Kogge stone adder and IBO circuit. The CSA is a digital circuit used for high-speed addition of multiple binary numbers. CSA reduce the number of carry operations.The Kogge stone adder is more suitable for faster operation of Vedic multiplier. Hence, square architecture design using a kogge stone adder proves to be highly efficient and also provides less complexity in terms of designing the square architecture compared to CSA. The IBO circuit is used in square architecture .When input from the OR gate is ‘0’ there is no alternation to the output. If the input’1’ binary output incremented to the next higher order bit.

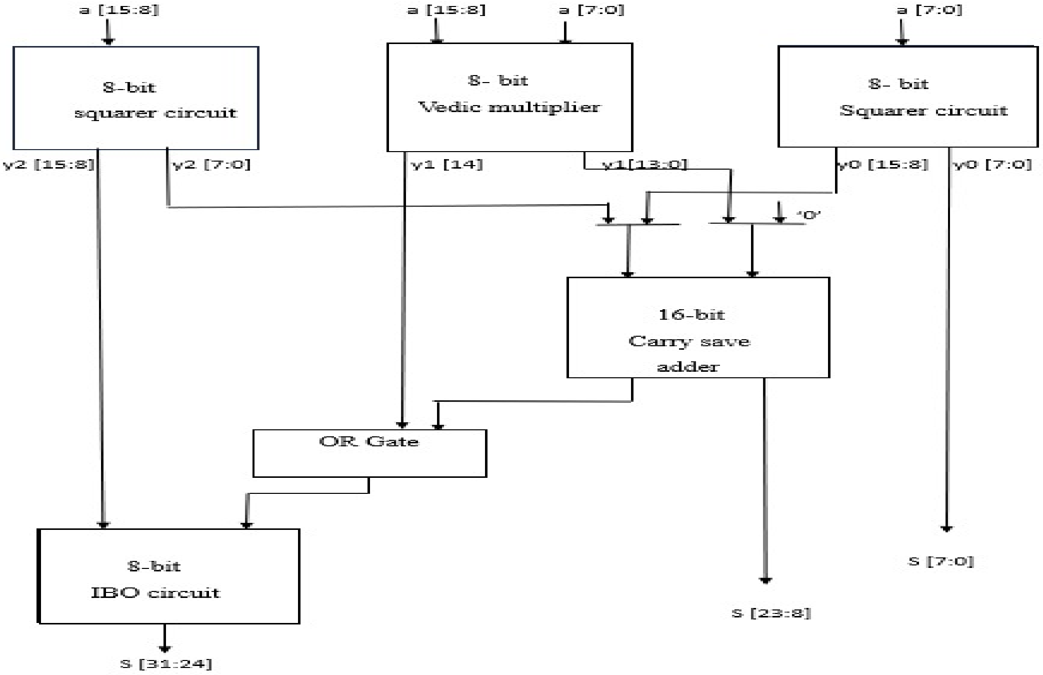

Figure 4. 16-bit square architecture using carry save adder

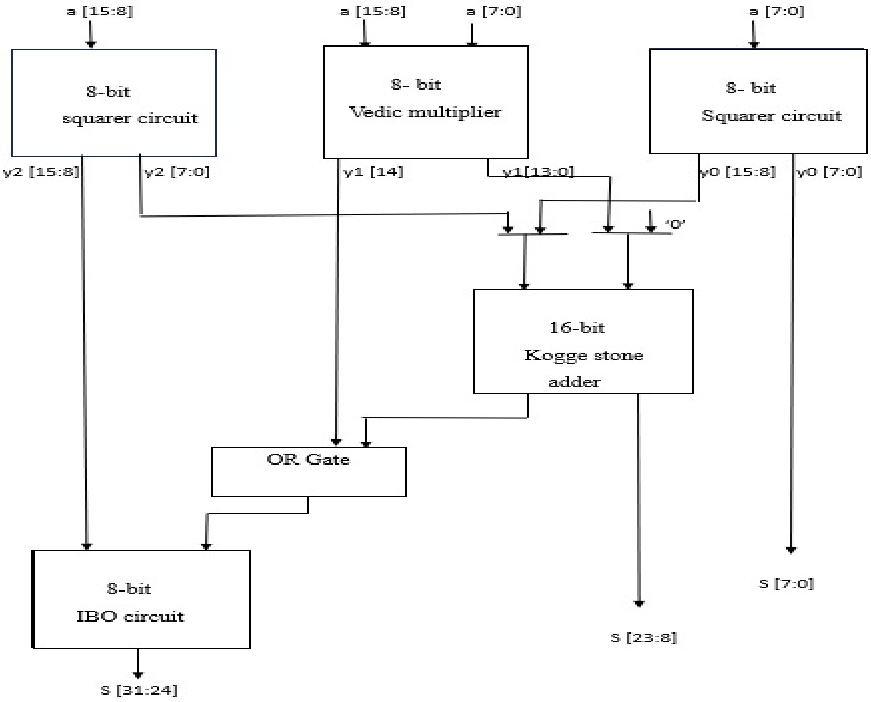

Figure 5. 16-bit square architecture using kogge stone adder

V RESULT AND ANALYSIS

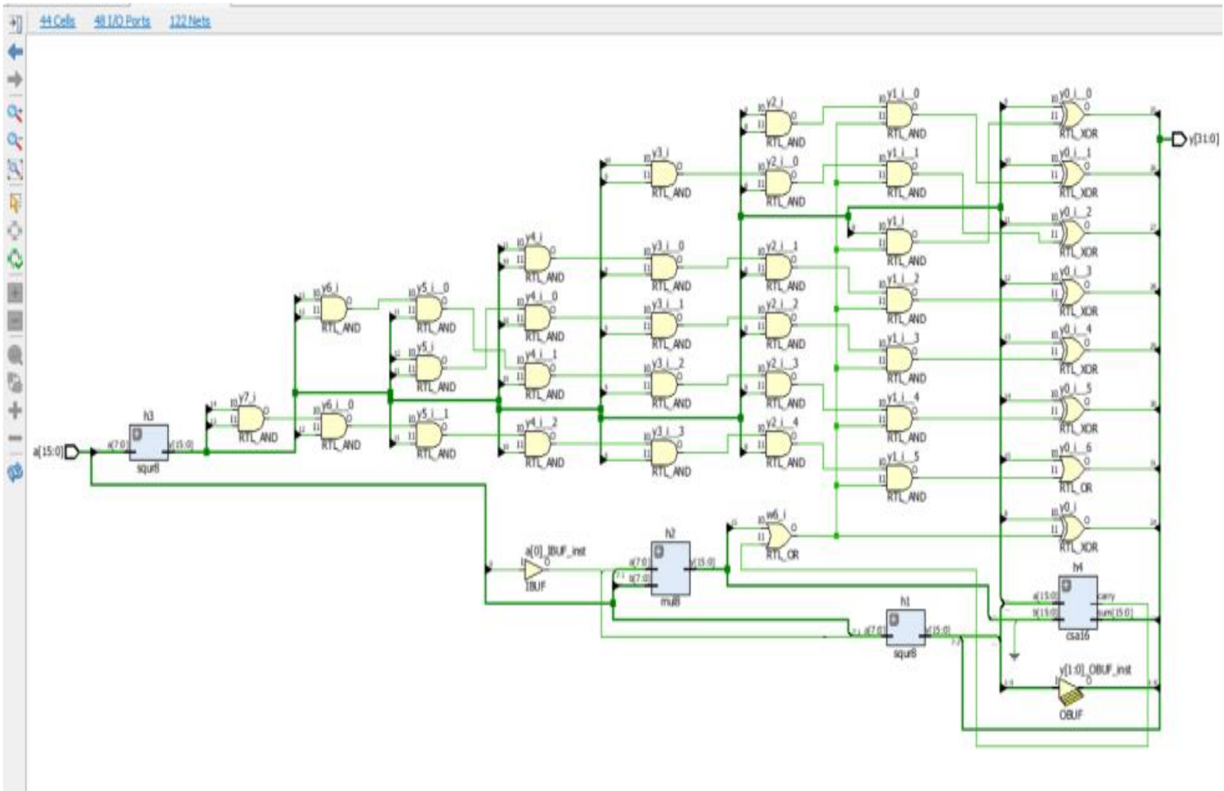

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Figure 6. RTL for square Architecture using CSA

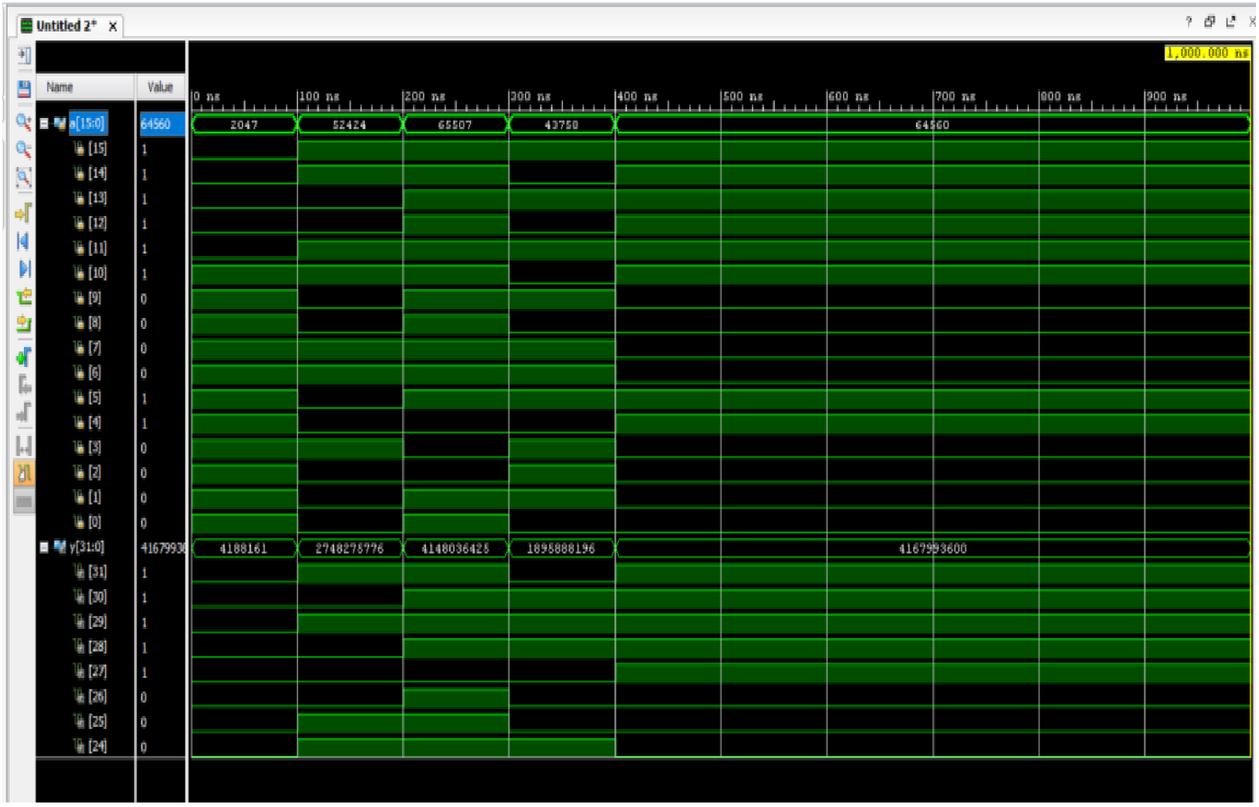

Figure 7. Simulation result of square architecture using CSA

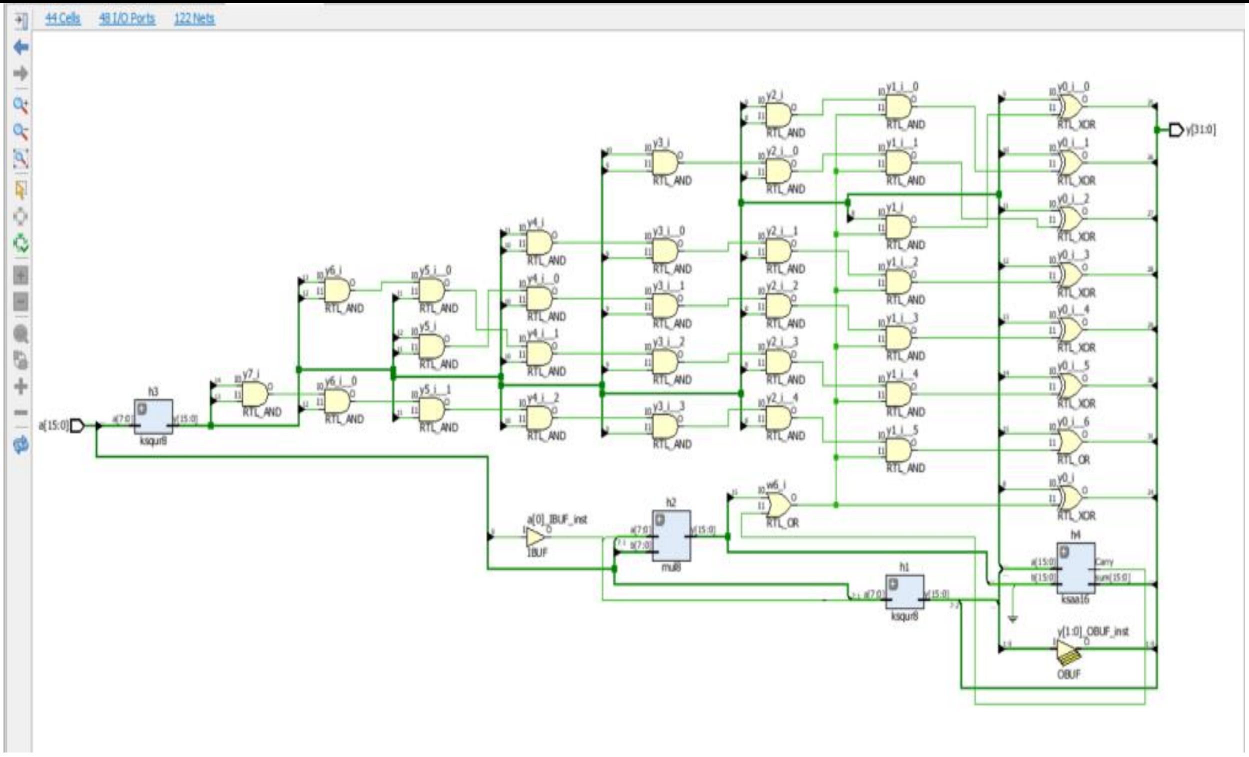

Figure 8. RTL for square architecture using Kogge stone adder

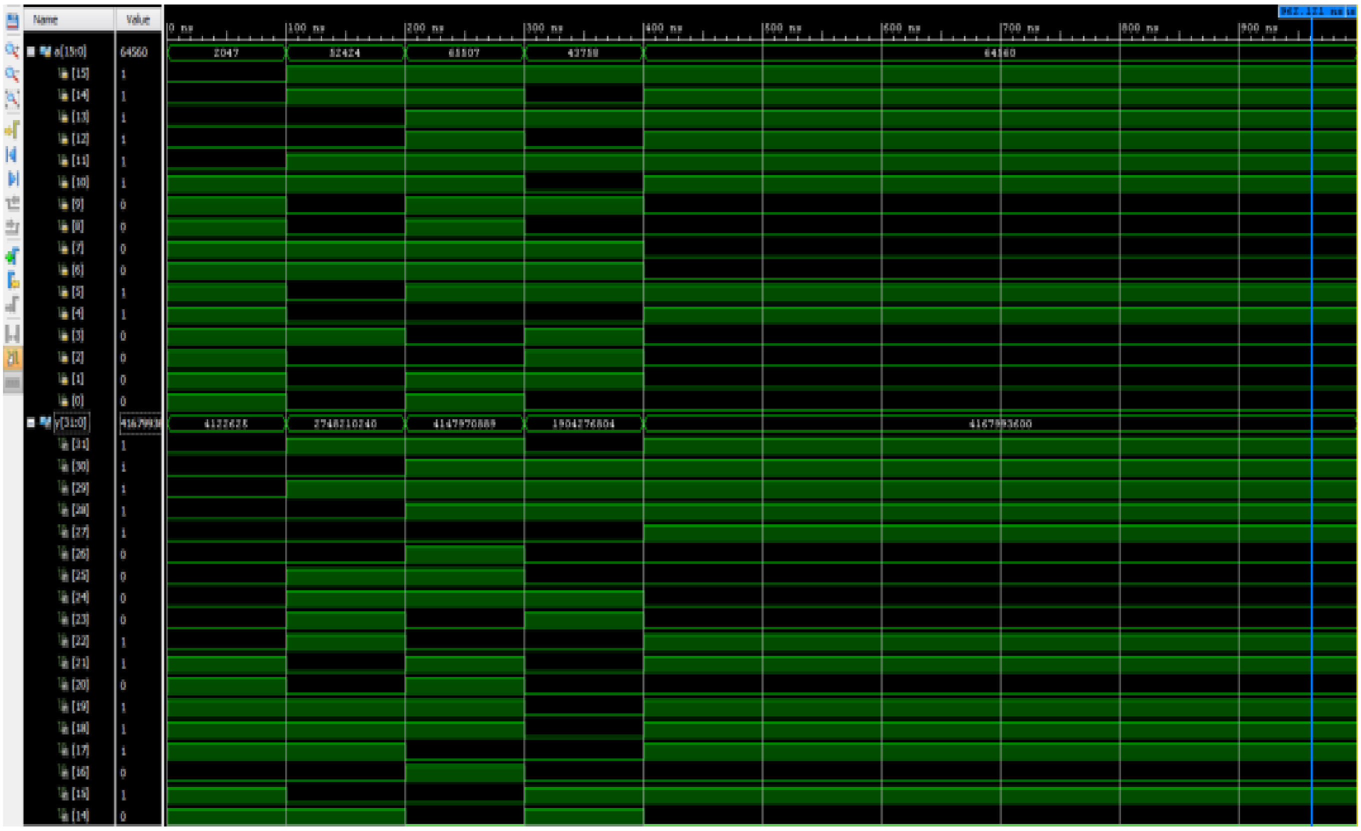

Figure 9. Simulation result of square architecture using kogge stone adder

Table 1. Comparison Table

Parameters	16-bit Square architecture using Vedic multiplier and carry save adder	16-bit square architecture using Vedic multiplier and Kogge stone adder
LUT	222	216
Power(w)	28.898	28.732
Delay(ns)	19.791	18.237

VI. CONCLUSION

The proposed architecture based on Vedic multiplier with carry save adder and kogge stone adder. The kogge stone adder gives better performance in power consumption and delay compared to carry save adder. The design of 16-bit square architecture was implemented on Xilinx Vivado 2016.4 version software by using a ZED board.

FUTURE SCOPE

Future work could explore different parallel prefix adder and widely used Techniques for designing squarer circuit. By looking at the advanced techniques, the project can pave the way for even low-power and high speed squarer circuit.

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