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Double-Pass Transistor Logic Is Utilized In The Development Of A Novel Binary-To-Ternary Converter.

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ABSTRACT

A comparison of the ternary circuit versus the binary circuit reveals that the ternary circuit is superior in terms of interconnect complexity, propagation time, and energy usage. The purpose of this work is to present a unique binary-to-ternary converter that makes use of a Double Pass-Transistor (DPL) that includes four bits as input and three trits as output. It is possible that this work may raise the data rate while simultaneously reducing the amount of power that is consumed, which is why it is so important. In addition to this, the converter that has been developed can also serve as a bridge between binary and ternary circuits. Simulation and testing of the suggested circuit are carried out with the help of a Micro-Cap V10 PSPICE simulator including CMOS process technology. Following that, it is compared to many binary-to-ternary converters in order to arrive at the conclusion that a considerable improvement was obtained.

Keywords: Double-pass, Transistor logic, Binary-to-ternary, Novel, Multiple-Valued Logic.

1. INTRODUCTION

The limits of binary circuits are mostly caused by the enormous number of connections that are required, which in turn necessitates a large chip surface and a significant increase in the amount of energy that is used. On the other hand, Multiple-Valued Logic (MVL), which contains more than two values, contributes to the reduction of interconnections, chip area, and energy consumption [1].

Over the course of the last 10 years, MVL has been a subject of interest for scholars who are interested in binary logic. It has also been utilized in a variety of contemporary application fields, such as Electronic Design Automation (EDA) tools, in order to tackle binary logic difficulties [2]. Furthermore, MVL may be applied in a variety of contexts, including communication systems [3, cloud vehicular networks [4, wireless sensor networks [5, circuit designs such as Logic Gates, Memory, and Memristor circuits [6–10], and software (algorithm) [11].

Additionally, it has been demonstrated that radix three, often known as ternary logic, is the most effective radix in terms of offering less complexity and reduced cost efficiency in comparison to other radixes [12]. Furthermore, there are two different logic systems that may be utilized in ternary logic. The balanced ternary logic, which corresponds to the equation (-Vdd, 0, Vdd), and the basic ternary logic, which corresponds to the equation (0, Vdd/2, Vdd), are both accessible. While the decimal number 15 requires four binary digits (bits) to store, four ternary digits (trits) are sufficient to store up to the decimal number 80 (34-1). This is an example of how MVL makes it possible to store a significantly greater amount of information in a single digit.

Recently, the design of binary-to-ternary converters has emerged as a dynamic area of research, and the articles that are selected are considered to be of significant importance.

For the sake of illustration, a new circuit that transforms two binary bits into one ternary digit (trit) was presented in [13] and [14]. A unique binary-to-ternary converter that is based on the Josephson junction (JJ) was proposed by the authors when they published [15]. The converter circuit that was built is characterized by a dual supply operation in [16], whereas the suggested circuit that was adapted in the context of Quantumdot Cellular Automata is described in [17]. Finally, in [18], the authors introduced a unique binary-to-ternary converter that is based on DPL. This converter provides enhanced performance in comparison to all of the publications that were discussed earlier.

All of the binary-to-ternary converters that have been mentioned above have a number of drawbacks, including high power consumption [15], [16], a significant propagation delay [16], [18], a complicated circuit [16], [17], and even mistakes in the output when two binary inputs are set to high level voltage [13], [14]. As a result, the purpose of this paper is to propose a novel binary-to-ternary converter that offers a significant reduction in power consumption in comparison to circuits that utilize CMOS technology. Additionally, it reduces the propagation delay and offers a small, straightforward, and error-free circuit implementation (for all possible inputs). The suggested circuit uses Double Pass-Transistor Logic (DPL) to convert four binary bits into three ternary trits. It is simulated using Micro-Cap V10 PSPICE simulator, and it displays a significant decrease in the number of devices, the propagation latency, and the amount of energy that is consumed.

Following is the structure of the remaining parts of the paper: The history of DPL is discussed in Section II of this document. This part will explain the suggested conversion strategy, which is presented in part III. Section IV will cover the simulation results and comparisons, and section V will conclude with some concluding thoughts.

2. DOUBLE PASS-TRANSISTOR LOGIC (DPL)

DPL [19] is a modified form of complementary pass-transistor logic (CPL), as illustrated in Figure 1. It is achieved by combining PMOS transistors in parallel with NMOS transistors in order to overcome the issues of noise margin and speed deterioration at decreased supply voltages that are associated with

CPL circuits. In addition, fundamental logic gates that employ DPL should ideally have the same propagation delay in order to be able to be utilized for time-equalized applications such as wave pipelining.

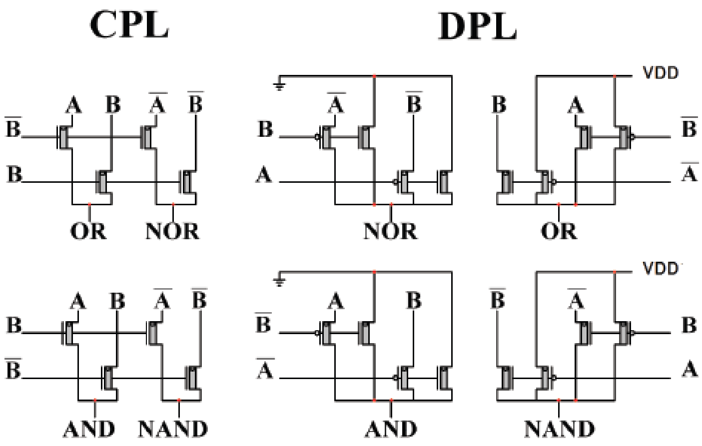

Fig. 1. DPL Gates Design

3. PROPOSED CONVERSION CIRCUIT

In Figure 2, a unique binary-to-ternary converter model with a four-to-three ratio has been created.

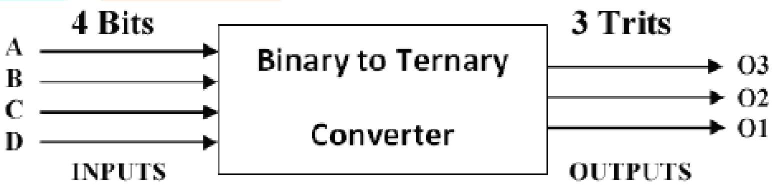

Fig. 2. Binary-to-ternary model

As can be seen in Figure 2, the input consists of four binary bits written as A, B, C, and D. "A" is the most significant bit (MSB) during the input process, whereas "D" is the least significant bit (LSB) during the same process. O3, O2, and O1 are the three trits that are delivered as output. Through the utilization of straightforward ternary logic (0, 1, 2), the output "O3" represents the most significant trit (MST), whereas "O1" represents the least significant trit (LST). The remaining eleven trits combinations might be utilized for extra features such as error detection, whereas just sixteen of the twenty-seven trits combinations were used to represent all of the four-bit combinations simultaneously. The converter circuit has the potential to make sixteen different combinations, which are displayed in Table I. In an effort to reduce the amount of power that is consumed, the suggested circuit makes use of a voltage supply of 1.8V. According to the information presented in Section II, DPL is utilized in order to get rid of the noise.

Ternary trits are represented by the values (0: Low, 1: Medium, and 2: High), while binary digits are described as (0: Low, and 1: High). For both the binary and the ternary system, the letter "0" will be used to represent low-level voltage (0V), the letter "1" will represent medium-level voltage (0.9V), and the letter "2" will represent high-level voltage (1.8V).

TABLE I
BINARY-TO-TERNARY TRUTH TABLE

	Binary Inputs				Ternary Outputs		
Decimal	A	B	C	D	O3	O2	O1
0	0	0	0	0	0	0	0
1	0	0	0	2	0	0	1
2	0	0	2	0	0	0	2
3	0	0	2	2	0	1	0
4	0	2	0	0	0	1	1
5	0	2	0	2	0	1	2
6	0	2	2	0	0	2	0
7	0	2	2	2	0	2	1
8	2	0	0	0	0	2	2
9	2	0	0	2	1	0	0
10	2	0	2	0	1	0	1
11	2	0	2	2	1	0	2
12	2	2	0	0	1	1	0
13	2	2	0	2	1	1	1
14	2	2	2	0	1	1	2
15	2	2	2	2	1	2	0

To begin the process of constructing the suggested circuit, a unique approach is utilized. This technique involves decomposing each ternary output in Table I into two intermediate binary outputs, which are displayed in Table II and Table III respectively.

TABLE II

Decomposition O1 to two intermediate Binary Outputs

Ternary Output	Intermediate Binary Outputs	
O1	O1a	O1b
Logic 0 (0V)	0	0
Logic 1 (0.9V)	0	2
Logic 2 (1.8V)	2	0

TABLE III
DECOMPOSITION OF THE THREE TERNARY OUTPUTS

Binary Inputs				Ternary Outputs as Intermediate Binary				
				O3	O2		O1	
A	B	C	D	O3b	O2a	O2b	O1a	O1b
0	0	0	0	0	0	0	0	0
0	0	0	2	0	0	0	0	2
0	0	2	0	0	0	0	2	0
0	0	2	2	0	0	2	0	0
0	2	0	0	0	0	2	0	2
0	2	0	2	0	0	2	2	0
0	2	2	0	0	2	0	0	0
0	2	2	2	0	2	0	0	2
2	0	0	0	0	2	0	2	0
2	0	0	2	2	0	0	0	0
2	0	2	0	2	0	0	0	2
2	0	2	2	2	0	0	2	0
2	2	0	0	2	0	2	0	0
2	2	0	2	2	0	2	0	2
2	2	2	0	2	0	2	2	0
2	2	2	2	2	2	0	0	0

In the second stage, Karnaugh maps are utilized in order to obtain an optimal circuit for each of the intermediate outputs that are listed in Table III.

Equations 1 through 5 are the end result of the minimization procedure.

$$O1a = \overline{A}\,\overline{B}\,C\,\overline{D} + \overline{A}\,B\overline{C}\,D + A\,\overline{B}\,\overline{C}\,\overline{D} + A\,\overline{B}\,C\,D + A\,B\,C\,\overline{D} \quad (1)$$

$$O1b = \overline{A}\,\overline{B}\,\overline{C}\,D + \overline{A}\,B\overline{C}\,\overline{D} + \overline{A}B\,C\,D + A\overline{B}\,C\,\overline{D} + A\,B\overline{C}\,D \quad (2)$$

$$O2a = \overline{A}\,B\,C + \overline{A}\,B\,\overline{C}\,D + B\,C\,D + A\overline{B}\,\overline{C}\,\overline{D} \quad (3)$$

$$O2b = B\overline{C} + A\,B\overline{D} + \overline{A}\,\overline{B}\,C\,D \quad (4)$$

$$O3b = AB + AC + AD \quad (5)$$

The binary-toternary converter circuit depicted in Figure 3 is where the equations that were derived from the process are implemented.

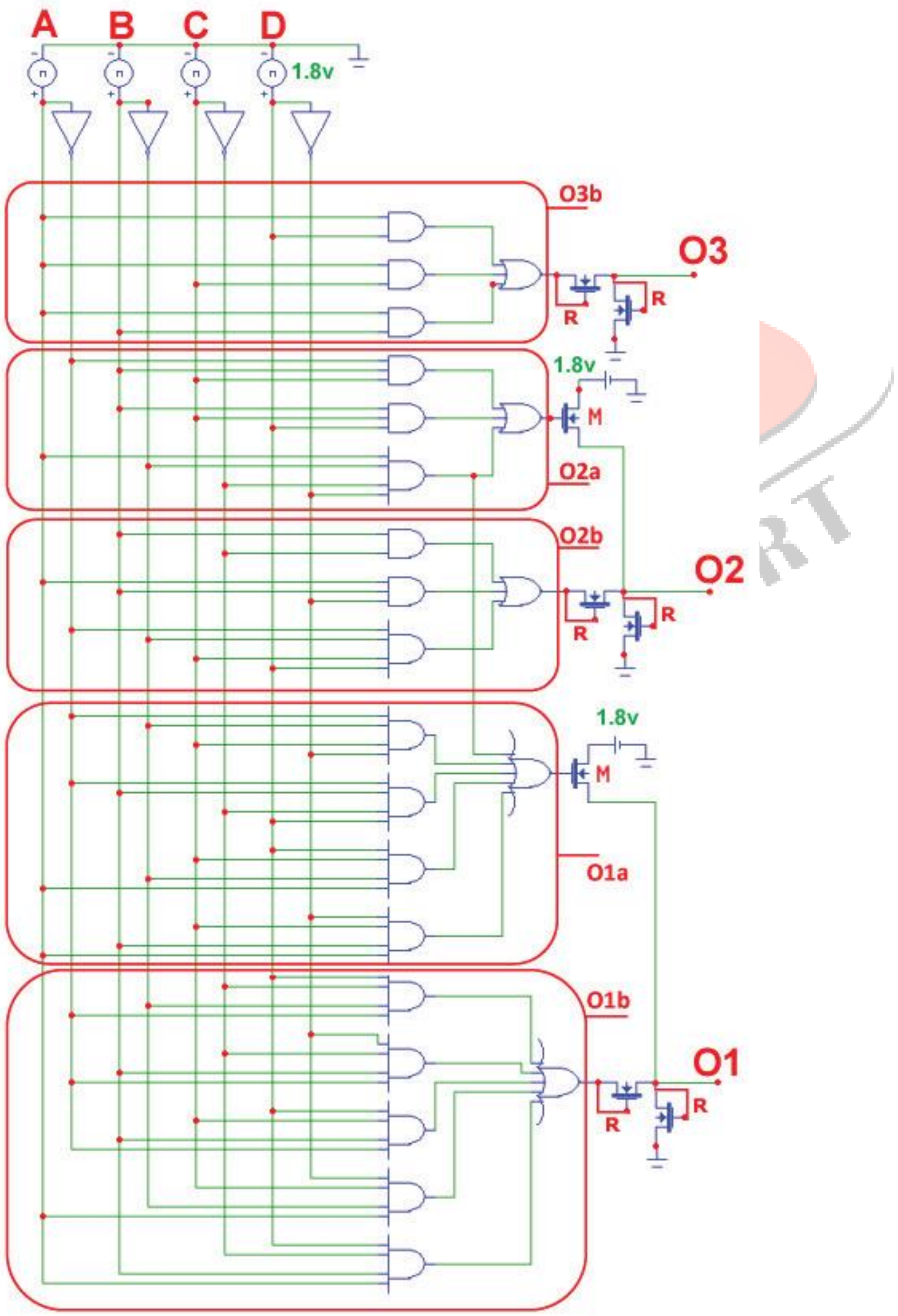

Fig. 3. Proposed binary-to-ternary Converter Circuit

The binary-to-ternary converter is depicted in Figure 3, which has four binary inputs (A, B, C, and D) and three ternary outputs (O1, O2, and O1) respectively. the binary outputs that are intermediate and are identified as O1a, O1b, O2a, O2b, and O3b respectively.

A MOSFET (M) that has been enhanced and is being utilized as a switch using its inputs (O1a and O2a). In order to send the 1.8 volts to the ultimate output O1, the transistor M will be switched "ON" when the O1a or O2a voltage is at a high level. Conversely, when the O1a or O1b voltage is at a low level, the transistor M will be turned "OFF."

Additionally, a voltage divider is created by the addition of two transistors (R) that are placed after the intermediate outputs (O1b, O2b, and O3b). As an illustration, take the case where the output O1 is equal to 0.9V and the output O1b is equal to 1.8V. When O1b is equal to 0V and O1a is equal to 1.8V, the two transistors (Rs) will transform into two parallel resistors with equivalent resistance (Req), which will result in a decrease in the output voltage O1 to 1.7V. This is explained in Table IV.

TABLE IV
COMBINATION OF TERNARY OUTPUT O1

O1a	O1b	Transistor (M)	(2 Rs)	O1
0V	0V	OFF	Req	0V (Logic 0)
0V	1.8V	OFF	Divider	0.9V (Logic 1)
1.8V	0V	ON	Req	1.7V (Logic 2)
1.8V	1.8V	This Case Does Not Exist* Whereas, in [13] and [14] have errors		

When it comes to output (O2) and (O3), the identical procedure will be carried out. The suggested design has a significant advantage over earlier converter designs described in [13] and [14] due to the fact that it does not produce any errors for any combination of input characteristics. The fact that the intermediate binary outputs Oia and Oib (i=1, 2) cannot both be high at the same time is proven in Tables III and IV. This presents a considerable benefit in terms of simplifying the circuit.

The total number of devices comprised in the proposed circuit, as determined by the calculations in Table V.

TABLE V
DEVICE COUNT IN PROPOSED CIRCUIT (FIG.3)

Device Name	No. of devices	No. of Transistors	Subtotal
Inverter Gate	4	1 input *2 =2	8
2 inputs AND Gate	2	2 inputs *2 = 4	8
3 inputs AND Gate	3	3 inputs *2 = 6	18
4 inputs AND Gate	11	4 inputs *2 = 8	88
3 inputs OR Gate	3	3 inputs *2 = 6	18
5 inputs OR Gate	2	5 inputs *2 = 10	20
MOSFET	8	1	8
Internal Resistor (one per each gate Fig.1)			25
Internal Capacitor (one per each gate Fig. 1)			25
Total No. ofDevices			**218**

3. SIMULATION RESULTS AND COMPARISONS

An innovative binary-to-ternary converter that is based on DPL was proposed by the authors in [18]. This converter provides superior performance to the binary-to-ternary converters that were presented in [13]–[17]. Consequently, the converter that has been presented will be evaluated in comparison to the most recent converter circuit designs that are detailed in [18]. The two circuits are developed, simulated, and evaluated using the same software, which is Micro-Cap V10 PSPICE Simulator with CMOS technology 0.18 μm. This is done to ensure that the comparisons are fair at all times.

As was previously reported in [19] and illustrated in Figure 1, the simulated circuits make use of an implementation of the AND and OR DPL gates. According to the information provided in [20], the average power is 4.08 μw, the average propagation delay is 42.56 ps, and the temperature is 25 degrees Celsius.

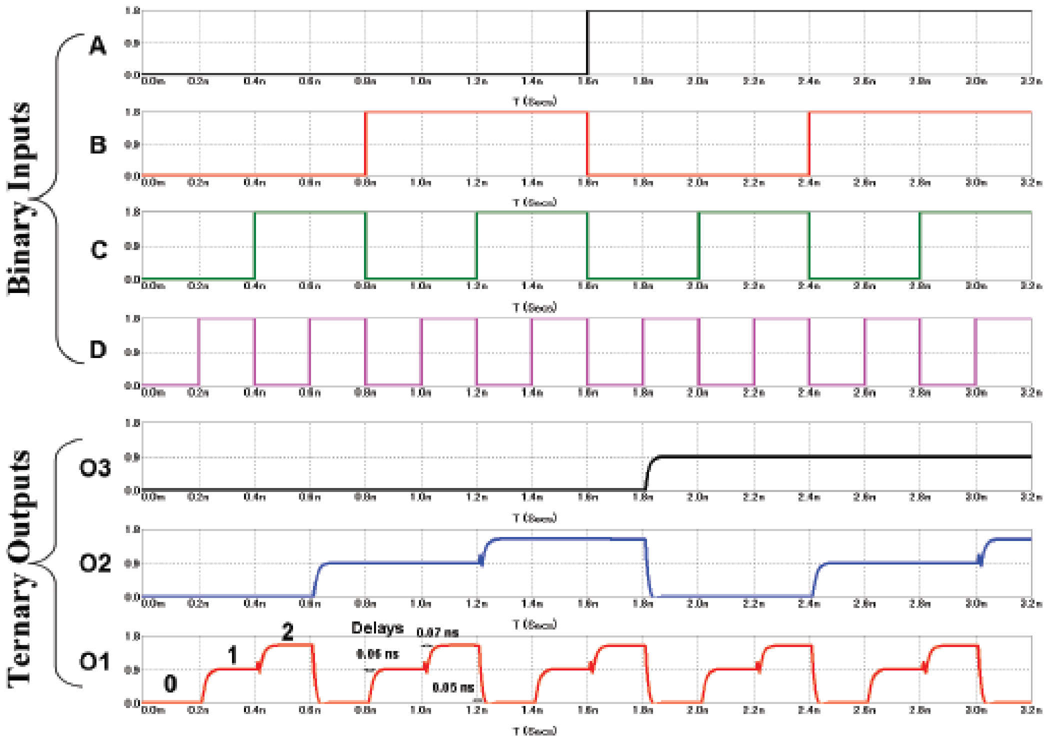

Fig. 4. The simulation transient analysis of proposed circuit

The simulated transient analysis of the proposed circuit is depicted in Figure 4. When the temperature is 25 degrees Celsius, the power supply is 1.8 volts, and the frequency is 5 gigahertz. The following performance parameters will be utilized in order to make a comparison to [18]: the frequency, the number of devices included inside the circuit, the maximum propagation delay, the average power consumption, the maximum energy consumption, and the type of logic gates that are utilized. Propagation delays in the circuit that is being suggested are as follows: It takes 0.06 nanoseconds to get from the binary "0" to the "1" position, 0.07 nanoseconds to go from the "1" to the "2" position, and 0.05 nanoseconds to go from the "2" to the "0" position. Based on the simulator, it has been determined that the suggested circuit has an average power consumption of 349.9 μw.

Table VI provides a summary of that comparison.

TABLE VI
COMPARISON TO THE LATEST NOVEL CONVERTER IN [18]

	Converter [18]	Proposed	Improvement
Frequency	0.33 GHz	5 GHz	1415%
Device Count	426	218	48.83%
MAX. Delay	0.91 ns	0.07 ns	92.31%
Avg. Power	270.42 µw	349.9 µw	-29.4%
MAX. Energy	246 10^{-18}J	24.5 10^{-18}J	90%
Type of used gates	Ternary & binary gates	binary gates	Faster, as [21]

The suggested converter with a ratio of 4:3 is larger than the most recent converter with a ratio of 3:2 in [18]. In spite of this, the converter that has been developed achieves superior results in comparison to [18], as can be shown in Table VI.

6. CONCLUSION.

A binary-to-ternary converter that makes use of many innovative strategies is proposed in this research. Using a Double Pass-Transistor (DPL), the suggested method involves the utilization of four bits in order to generate three trits.

The Micro-Cap V10 PSPICE simulator was used to construct and simulate the circuit using the software. In conclusion, the results of logical analysis and simulation illustrate the advantages of the technique in terms of reduced latency and energy usage in comparison to alternative converters.

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