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Designing A Programmable Delay Timer On Cadence Using 45nm Technology

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Abstract: This research explores the design and implemen-tation of a programmable delay timer using Cadence tools and 45nm CMOS technology. The goal is to develop a high-precision timer with low power consumption and a small area footprint. Utilizing the 45nm process technology, we created a comprehensive library of cells, including detailed layouts and transistor-level schematics. The proposed timer design shows potential for future VLSI applications, meeting the demand for energy-efficient and high-performance digital circuits. In this paper designed and implemented the Programmable delay Timerbased system core from RTL to GDSII. The Programmable Delay Timer underwent functional verification using the NC Launch tool. Subsequently, a gate-level netlist was generated with a 45nmtechnology library file in the Genus tool. After carrying out Area,power, and timing reports the optimized results are 1155 μm^2, 0.00313498 mW and 9.890 ps.

Index Terms - Programmable Delay Timer, RTL-to-GDSII, Cadence ASIC design, power optimization.

I. INTRODUCTION

In the realm of digital integrated circuits, precise timing control stands as the critical factor distinguishing success fromfailure. Programmable delay timers play a pivotal role in ensuring that signals propagate through a digital system with the required timing accuracy, enabling synchronous operation and synchronization of various components. These timers find applications across diverse domains, from microprocessors and microcontrollers to telecommunications and signal processing.

The journey from conceptualization to silicon involves a series of intricate steps collectively known as the RTL (Reg- ister Transfer Level) to GDSII (Graphic Data System II) flow. This transformation process converts a high-level functional description into a physical layout ready for fabrication. While this flow is generic to digital design, the nuances of designing a programmable delay timer demand special attention due to stringent timing requirements and the need for precise control over delay intervals.

This paper delves into the specifics of implementing a programmable delay timer using a comprehensive RTL toGDSII flow. We explore each stage of the design process, starting from RTL coding and synthesis to the final tape- out stage where the GDSII file is generated. Throughout this journey, we highlight the unique challenges faced during

Fig. 1. Sub module of Programmable Delay timer

programmable delay timer design and propose effective solu- tions. By elucidating a systematic approach, we aim to equip designers with the knowledge and tools necessary to tackle these complexities within the RTL to GDSII framework.The figure 1 presents a simplified model of a Programmable DelayTimer.

I. LITERATURE SURVEY

Programmable delay timers have been a subject of research and development due to their critical role in various digital systems. This chapter reviews the significant contributions andadvancements in the field, highlighting key developments and innovations.

A. Key Research Areas

Standard Cell Library Design and Characterization: Developing a comprehensive standard cell library suitable for 45nm CMOS process. Creating necessary cells with detailed layout and transistor-level schematics. Ensuring full synthesizability for efficient integration into larger designs

- **Low Power and High-Speed Full Adder Designs:** In- vestigating various full adder designs using 45nm CMOStechnology. Balancing power consumption and propaga- tion delay for optimal performance
- **1-Bit Full Adder Analysis**Exploring different techniquesfor designing 1-bit full adders in Cadence 45nm technol- ogy. Considering layout and transistor-level details
- **AI for Augmentation:** Leveraging AI to augment humancapabilities. Combining AI's data synthesis abilities with human intuition for better decision-making. Applications include personalized medicine, clinical data analysis, andcreative problem-solving4.
- **Data Science:** Extracting meaningful insights from di- verse and massive data sources. Using digital signal processing algorithms to uncover patterns and structures. Applying data science to fields like chemical informatics,energy efficiency, and disease dynamics4.

II. METHODOLOGY

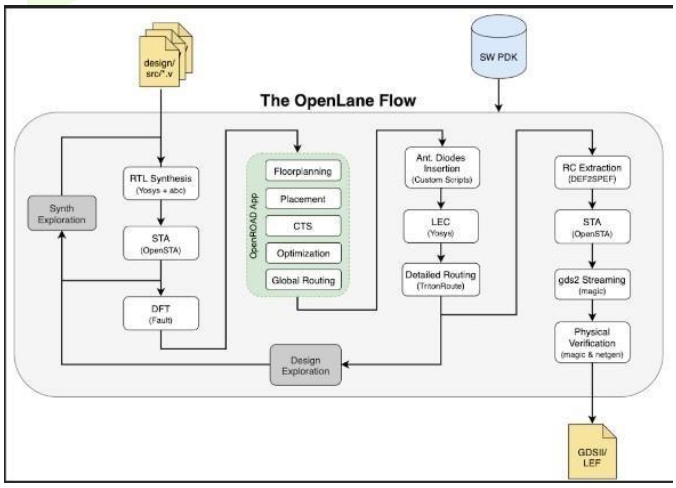


Fig. 2. RTL to GDSII Flow

This thesis aims to implement the RTL to GDSII flow fora Programmable Delay Timer. The design process employs a 45nm technology library, including slow.lib and fast.lib files, alibrary exchange file (.lef), Synopsys design constraints (.sdc) file, and various scripts for synthesis, static timing analysis, and physical design.

In the frontend phase, the functionality of the ProgrammableDelay Timer was verified using the NC Launch simulator tool by Cadence. Following verification, the Cadence Genus tool generate's the gate-level netlist.

The backend physical design was carried out with the Cadence Innovus tool, involving steps like floorplanning, partitioning, placement, and routing. Partitioning simplified complex circuits, floorplanning assigned boundaries to all blocks, placement arranged standard cells in the core area, and routing established connections according to the netlist. Performance was analyzed and optimized in both pre-CTS and post-CTS stages. This work encompasses both the frontend and backend aspects of the RTL to GDSII flow, as shown in Figure 1.

A. Simulation Part

The simulation part is carried in the Xcelium, Xcelium is the engine that performs the actual simulation, while NC- Launch provides the front-end interface for user interaction and control. Required files are:

Register Transfer Level (RTL) code: This is the high-level description of the circuit's behavior, written in a hardware description language (HDL) like Verilog or VHDL.

Testbench: This is a separate HDL file that generates input signals and checks the output responses of the design under test (DUT). It simulates the environment in which the DUT will operate.

The typical simulation flow involves the following steps:

- Compilation:The RTL design and testbench are com- piled into an executable simulation model.
- Elaboration:The simulation model is linked with the standard cell libraries and technology libraries.
- Simulation: The testbench generates stimuli, the DUT responds, and the outputs are compared with expected results.
- Debugging: If errors or violations are detected, the design is debugged and modified.
- Regression: The simulation is repeated with different testbenches to ensure the design's robustness under vari- ous scenarios.

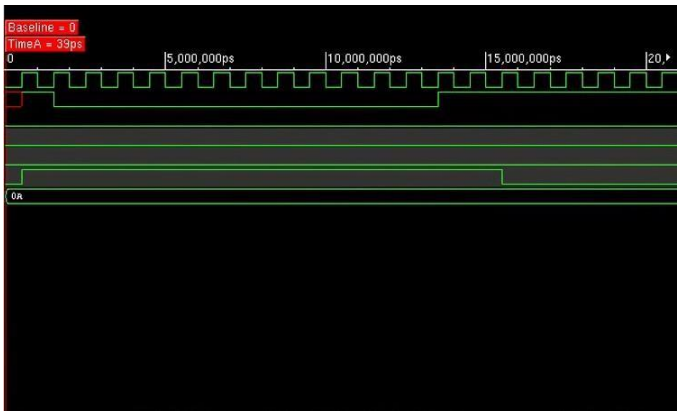
B. Synthesis Part

The synthesis process, executed using the Genus tool, transforms the register transfer logic (RTL) design into a gate- level netlist. This transformation requires RTL code, Synopsys Design Constraints (SDC) file, and a Tcl script to automate the entire flow. The resulting gate-level netlist, along with a modified SDC file, serves as input to the physical design process. Additionally, the synthesis tool generates reports on timing, area, and power to evaluate the design's performance at the gate level.

C. Physical Design Part

The physical design process, utilizing the Cadence Innovus tool, involves the placement and routing of a gate-level Verilog netlist. Innovus places standard cells, performs power routing, and generates comprehensive reports on timing, area, power, and design rule checks (DRCs). This process requires inputs such as the gate-level netlist, technology library files (.lib and lef)

III. EXPERIMENTAL RESULTS



The simulation output of a Programmable Delay Timer is shown in Fig. 3.

Fig. 3. Simulation Resuult

Utilizing the Cadence Genus synthesis tool, a gate-levelnetlist was derived from a functionally validated RTL de- sign, incorporating a 45 nm technology library and design constraints. This process yielded various reports, including a Synopsys Design Constraint (.sdc) file. Figure 4 illustratesthe synthesized top-level schematic of Programmable Delay Timer.

In the latter stages of the design process, the Cadence Innovus tool was employed. Initially, floor planning was conducted, where the core and IO utilization were defined, followed by the addition of power rings and stripes within the core area. The floor plan was configured with 70% of the area allocated to core utilization for standard cell placement, and 30% designated for routing, maintaining an aspect ratio of 0.8. Subsequent to floor planning, all standard cells were placed, and routing was performed. Design optimization followed these steps. At each stage of placement and routing, reports were generated, focusing on the analysis of area, power, and

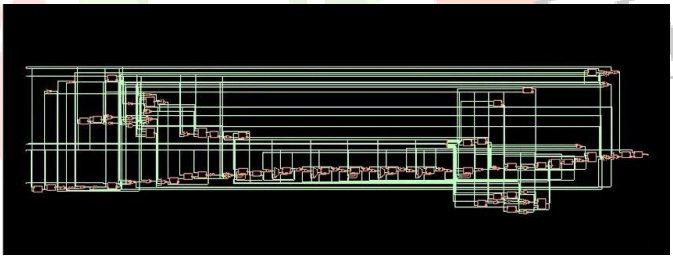


Fig. 4. Top Level synthesis

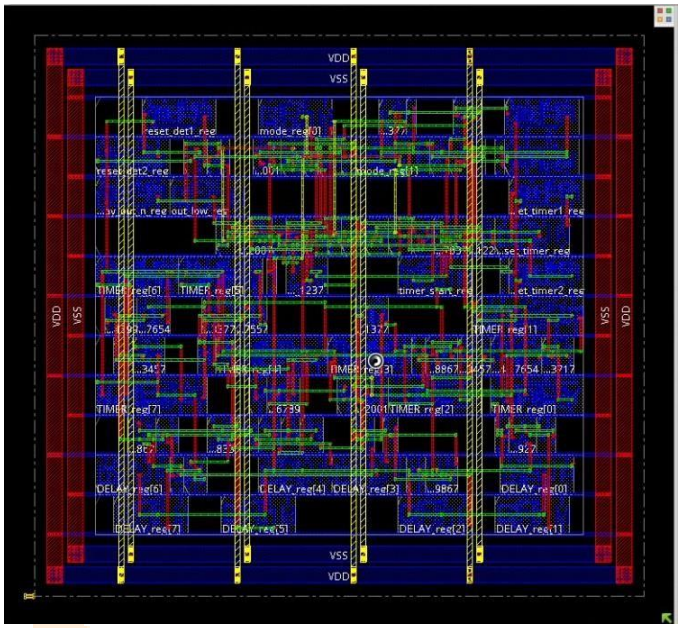


Fig. 5. Physical Design of Programmable Delay Timer

timing metrics. The physical design of the Programmable Delay timer resulting from this process is depicted in Figure5.

IV. ANALYSIS OF RESULTS

The results analysis primarily focuses on area, power, and delay metrics throughout the design flow. Power analysis includes various power reports, while timing analysis encom- passes arrival time and slack. Table 1 presents the synthesis results, Table 2 displays pre-CTS results, and Table 3 show- cases the optimized post-CTS results.

TABLE I SYNTHESIS RESULT

Timing(ps)	Area (μm^2)	Total Power (mW)
Required = 10000	274.284	Leakage Power = 5.517
Arrival = 8453		Dynamic Power = 3186.468
Slack = 1547		Total Power = 3191.985

TABLE II
PRE-CTS RESULT (SPECIAL ROUTE)

Timing(ps)	Area (μm^2)	Total Power (mW)
Required = 9.726	1155	Internal Power = 0.00224364
Arrival = 9.615		Switching Power = 0.0088580
Slack = 0.111		Leakage Power = 0.00000553
		Total Power = 0.00313498

TABLE III
PRE-CTS RESULT (NANO ROUTE)

Timing(ps)	Area (μm^2)	Total Power (mW)
Required = 9.725	1155	Internal Power = 0.00224364
Arrival = 9.370		Switching Power = 0.00088580
Slack = 0.356		Leakage Power = 0.00000553
		Total Power = 0.00313498

TABLE IV POST-CTS RESULT

Timing(ps)	Area (μm^2)	Total Power (mW)
Required = 10.000	1155	Internal Power = 0.00224364
Arrival = 9.890		Switching Power = 0.00088580
Slack = 0.110		Leakage Power = 0.00000553
		Total Power = 0.00313498

v. CONCLUSION AND FUTURE SCOPE

In this study, we examined the design and implementation of programmable delay timers using Cadence tools within the 45nm process technology. Our key findings include:

Standard Cell Library Characterization We developed stan- dard cell libraries for the 180nm, 90nm, and 45nm tech- nology nodes. The characterization results included metrics such as delay, leakage power, and area for various design styles, driving strengths, and process corners. These libraries are valuable resources for academic and research purposes, facilitating efficient chip implementation.

Digital Design Flow Our work adhered to a systematic digital design flow, focusing on the creation of well-designed and verified blocks. These blocks help shorten development time and manage chip complexity, contributing to efficient ASIC designs.

While our research provides valuable insights, several areasremain for further exploration:

Automation of Standard Cell Design Future work couldfocus on automating standard cell design using Cadence language or scripting, streamlining the library creation processand enhancing productivity.

Advanced Buffer Optimization Techniques Investigate more sophisticated buffer designs that balance power, delay, and other performance metrics. Explore adaptive buffering strate- gies based on dynamic workload variations.

Process Node Scaling Extend our study to smaller process nodes (e.g., 32nm, 22nm, or beyond) to analyze how standard cell characteristics evolve with technology scaling.

Power-Area Trade-offs Optimize standard cell layouts to minimize area while maintaining performance. Investigate trade-offs between area reduction and potential impact on timing.

Application-Specific Libraries Develop specialized librariestailored to specific applications (e.g., IoT, edge computing,
or AI accelerators) considering unique requirements such as ultra-low power or high-speed operation.

In summary, our research establishes a foundation for efficient programmable delay timer designs. By addressing the future scope areas, we can continue to advance digital integrated circuits and contribute to the evolving field of semiconductor technology.

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