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A Low-Power 10T SRAM Cell Design With SAPON And DTMOS Integration

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Abstract: This study delves into a 10T SRAM cell with little power incorporating two extra sleep transistors, distinguished by strong written and verbal stability. The 10T SRAM cell's core module houses these slumber gates as footers and header transistors. Using the Sapon method and DTMOS emerges as the optimal strategy to expand this approach for reduced power consumption at 3.858×10^{-8} and latency at 1.503×10^{-10} The entirety of this design was simulated utilizing Tanner EDA's 16nm CMOS Technology.

Index Terms - SRAM, layered semiconductor, Schmitt activation circuit.

I. INTRODUCTION

Reducing power consumption has been crucial towards the creation of system-on-chips (SoCs), which find application in areas like bio-implants, smartphones, autonomous wireless sensors, and energy collection devices. These systems typically run on minimal energy sourced from batteries or renewable sources. S-RAM takes up a significant portion of the SoC, necessitating a focus on reducing SRAM energy usage as part of the broader goal to cut overall energy expenditure. The most efficient method to conserve energy involves lowering power consumption by diminishing the Vdd. As VDD decreases, power usage drops exponentially. Yet, this power reduction comes with drawbacks, such as increased delay times and elevated soft error rates (SERs), resulting in decreased operational efficiency. Within the sub-threshold voltage (Vth) zone, where VDD is less than Vth, delays escalate dramatically. Although this achieves ultra-low power levels, energy consumption spikes due to amplified static energy costs. Operating close to Vth, where VDD is just above Vth, enables significant power savings over super-Vth operations, alongside a notable reduction in delay compared to sub-Vth operations. Balancing power and delay in the near-Vth region is vital for minimizing energy usage. Near-Vth operation presents issues like soft errors caused by α-particles, increasing SER. To tackle this, In order to minimize multi-bit mistakes, a bit-interleaving scheme is used, a common issue in non-bit-interleaving setups. The near-Vth region also exhibits sensitivity to Vth variations in transistor currents, especially impacting SRAM cells due to the requirement for smaller transistors for higher density. In light of these considerations, we introduce ST 9T, obviating the need for a write-back mechanism. This design promises reduced use of energy relative to others while occupying a smaller cell area. Its standout features include the use of standard and Schmitt-trigger inverters in a cross-coupled structure for enhanced read stability, a unified bit-line structure for minimized energy use and space, and superior write performance achieved through a tailored Sapon technique in conjunction with the ST inverter write assist method.

II. LITERATURE SURVEY

This research introduces tailored to meet the requirements for stable and energy-efficient SRAM in contemporary microprocessors functioning at reduced Vdds. We present a 12T Power Gated Schmitt Trigger SRAM cell architecture, with the goal of boosting read and write stability without necessitating supplementary peripheral circuits or control signals per cell. The design methodology employed SYNOPSYS Custom Designer for schematic development, layout, and result acquisition.

The design achieves the following notable outcomes:

A die size of 1.25 square millimeters. Power usage of 2.43 milliwatts.

Slack time of 31.45 nanoseconds.

The SRAM incorporates a 16-bit addressable word line and boasts a memory capacity of 512 bytes. It underwent simulation over an operating frequency spectrum of 25–200 MHz under a Vdd of 1V. Significantly, the primary contributor to power consumption in this fully customized design is identified as the banking and row decoders, indicating opportunities for optimization in subsequent versions. [1].This study advances the initiative to create energy-efficient SRAM technologies appropriate for sophisticated microprocessor applications, underscoring the significance of pioneering cell designs and engineering approaches in attaining low- power operation without sacrificing performance or stability. [2]. The growing necessity to reduce power consumption in memory designs has led to a shift towards operating memories at lower Vdds. Research into sub-threshold operation for logic circuits indicates that minimal energy consumption is feasible in this regime. These findings imply a convergence for energy-limited applications where SRAM operates at sub-threshold voltages aligned with logic operations. Given that sub-threshold voltages offer limited space for large static noise margins (SNM), a deep comprehension of how various design choices and other factors influence SNM is essential. This study examines the dependence of SNM on sizing, V_DD, temperature, and both local and global threshold variations for sub-threshold bit cells in a 65-nm process [3]. Power management has emerged as the foremost design consideration for semiconductor engineers today. Despite Moore's Law continuing to add more transistors, power constraints now limit the practical application of these devices. Voltage scaling methods have gained traction as a means to decrease energy usage, with sub- threshold design marking the ultimate stage of voltage scaling. Though highly energy-efficient, sub-threshold design has remained confined to specialized applications due to significant performance drawbacks. This article delves into near-threshold computing (NTC), a design paradigm where the Vdd closely matches the transistor's threshold voltage. This approach combines the energy benefits of sub-threshold operation with improved performance and variability traits, making it suitable for a wide array of power- sensitive computing domains, from sensor networks to high-performance servers. The paper discusses the challenges hindering the broader acceptance of NTC and outlines recent efforts to address these hurdles. [4]. The design and analysis of low power CMOS Static Random Access Memory (SRAM) cells, particularly focusing on 7-transistor (7T) and 9-transistor (9T) configurations, aim to address the challenges of reducing power consumption while maintaining stability and performance in modern integrated circuits. These configurations are explored as alternatives to the conventional 6T SRAM cell to achieve better trade-offs between power efficiency, read/write stability, and area overhead.7T SRAM Cell: This configuration introduces an additional transistor compared to the standard 6T cell, typically used to enhance read stability or reduce leakage current during standby mode. The extra transistor can act as a read buffer or a sleep transistor to cut off the cell from the bit lines during idle periods, thereby reducing static power consumption [5].

III. Low Power 10T SRAM Working

A low standby power SRAM cell with 10T (LP10T) and high static noise margins is shown in this study. Our suggested design's salient characteristics comprise of A single-ended structure, Utilization of distinct bit lines for read and write functions, Enhanced read stability achieved through Schmitt-trigger and conventional inverters are arranged cross-coupled, and an additional read path is included.Execution of fictitious differential write operations leveraging the write-bit line (WBL) and the WWLA control signal,Enhanced write-ability made possible by writing-assist and pseudo-differential write operations, Reduction of the cell's dormant or escape power usage.

LP10TSRAM:

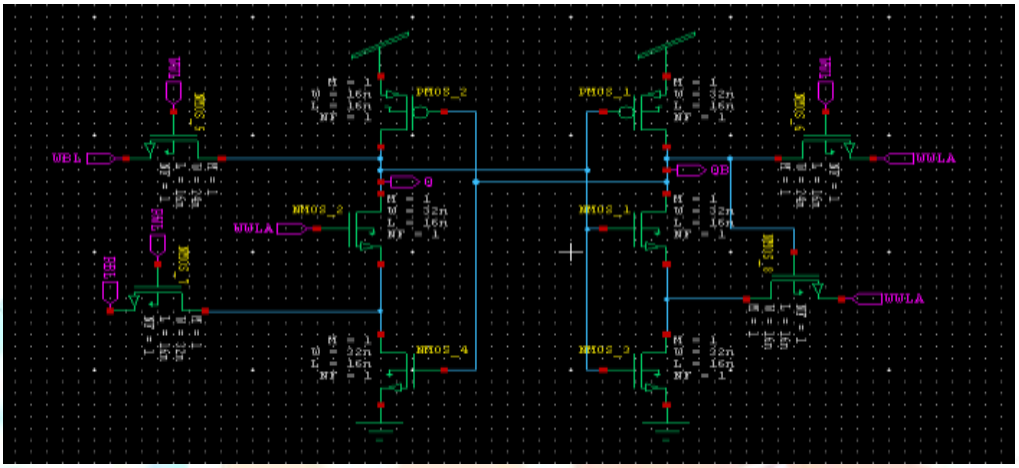

Fig1: Schematic diagram of LP10TSRAM

The suggested LP10T SRAM cell is built upon the cross-coupled architecture of a normal converter with a layered semiconductor (PUL, PDL1, and PDL2) and a pulse trigger-based converter (PUR, PDR1, PDR2, and NF). The cell core stores the information from the actual internal memory clusters Q and QB. Row-based composition word line (WWL) is used to regulate the write accessibility transistors, ACL1 and ACR1. The read accessibility transistor, or ACL2, is gated by the row-based read phrase line (RWL). The column-based command signal (WWLA) governs the read/write support transistor PDL2, which is positioned between the Q and phantom Q (PQ) nodes. Moreover, it is linked to the NF transistor's drain. Separate bit lines, such as column-based RBLas well as WBL for reading and writing, are used in the proposed cell.

Truth table:

	Operations			
Signals	Hold	read	Write '0'	Write '1'
RBL	1	1	1	1
WBL	1	1	0	1
RWL	0	1	0	0
WWL	0	0	1	1
WWLA	1	1	1	0

A. Maintain Position

Both the RWL as well as WWL indicators have been set to '0' during the hold Phase. The storage nodes are decoupled from the bit lines as a result of this operation, which eliminates the access for reading and writing transistors, as shown inFig 2. The WWLA signals can be switched to '1' in this setup, activating PDL2, guaranteeing that the cell's latch safely preserves the data that has been saved.

B. Bit line with One End Examine the operation

When WWL is decreased to '1', which disables write routes, PDL2 is activated during the read process? As a result, the standard inverter affects the storage node Q. RBL is initially pre-charged to VDD. When RWL is asserted, ACL2 is turned ON, and depending on the number stored at Q, the capacity volt of RBL either drains or stays in its initial elevated pre-charged condition.With the combination of a strong cross-coupled structure with ST and standard inverters, as well as a unique read path, our suggested LP10T SRAM cell solves the read failure problem. Compared to its traditional counterpart, the ST inverter has an exceptionally higher trip voltage. This enhancement stems from the reduction in the strength of PDR2 as Vx increases via the feedback transistor NF. Consequently, as the input voltage to the inverter escalates, the ST inverter demonstrates greater resilience and stability compared to its standard counterpart.In the read '0' operation, the Read Bit Line (RBL) is discharged to GND via a pathway involving the ACL2 and PDL1 transistors. As RBL discharges, the voltage at the PQ node rises from 0 to ΔV (ΔV equals 0.15 V under extreme Process-Voltage-Temperature (PVT) variations), which subsequently causes an increase in the Q node's voltage through PDL2. This rise ensures that the stored data in the cell remains unchanged, as the voltage does not exceed the trip voltage of the ST inverter. Consequently, the read '0' operation is executed successfully. Thanks to the elimination of the read disturbance issue by our proposed cell, the Read Static Noise Margin (RSNM) matches the Hold Static Noise Margin (HSNM). Nonetheless, when the output voltage of the ST inverter is high (Vout = VDD), the NF transistor activates, leading to a charge in the Vx node. This scenario complicates the alteration of Vout's high value. To address this, we increased the channel length of the PUR transistor in the ST inverter, balancing the '0' and '1' margins.

C. Write Operation using Pseudo Differential

Changing the Read Word program Line (RWL) indication to '0' to deactivate the read pathway by turning off ACL2 is the first step in starting a write operation. The Write Bit Line (WBL) in our suggested LP10T SRAM cell is driven to '0' to perform the write '0' operation, while WWLA stays at VDD, triggering PDL2. By doing this, a connection is made between the Q node and GND. The write access semiconductors (ACL1 and ACR1) are activated upon the occurrence of the control pulse WWL, enabling the discharge of the stored value of the Q node to the bitline and GND. The QB node is charged concurrently with the activation of the PUR transistor. Furthermore, WWLA makes it easier to write '0' onto the Q node by using the ACR1 transistor to inject '1' onto the QB node. Meanwhile, QB is set to '1', causing the NF transistor to switch on and creating a build-up of charge in the Vx node.The process of writing a '1' into the Q node of the newly developed LP10T SRAM cell involves several steps. Initially, the Write Bit Line (WBL) is raised to VDD. Due to the single-ended design of our proposed cell, inserting a '1' presents a unique challenge. To address this, we introduce an NMOS transistor, labeled PDL2, controlled by WWLA. During the write '1' operation, WWLA is deactivated ('0'), causing PDL2 to cut off. This action severs the connection between GND and the Q node, facilitating the writing of '1'. Subsequently, activating WWL powers up the write access transistors, allowing the value on WBL to be transferred to the Q node. Concurrently, transistors

PDR1 and PDR2 start to activate, leading to the discharge of data stored in node QB to GND. Simultaneously, WWLA assists in writing '1' to the Q node by discharging the QB node via ACR1. With QB set to '0', PUL activates, charging the Q node to VDD. Thus, despite employing a single-ended architecture for the write operation, our design effectively mimics differential operation through strategic use of the WWLA control signal and ACR1 transistor.We observed that the current circuit exhibits higher power consumption, prompting us to develop a novel low-power technology. Let's delve into discussing this innovation.

IV. Proposed Method

In this Chapter, here discussing about the novel design of SRAM using two transistors. The insertion of two transistors represents in above and bottom of the main circuit. Sapon technique is one of the best approach in this low power technologyworld.

Introduction to Sapon Technique:

The SAPON technique is centered on the concept of controlling leakage power, which is a significant contributor to power consumption in VLSI circuits. Leakage power occurs due to the unwanted flow of current through transistors even when theyare supposed to be off. To address this issue, SAPON places two leakage-control transistors outside the main logic circuit.

These transistors act as resistors that increase the opposing between the Vdd and Gnd, thereby controlling the leakagecurrents.

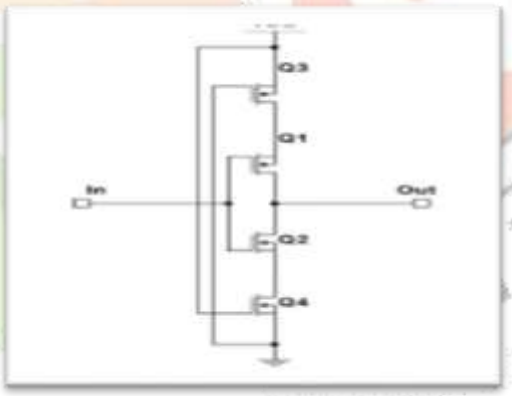

Fig2: Block diagram of Sapon technique

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Here's a more detailed explanation of how the SAPON technique works:

- Transistor Placement: The SAPON transistors are arranged in a stack configuration outside the main logic circuit. This arrangement allows them to provide effective leakage control without being part of the main logic pathway.

- Active Operation: The gate terminals of these SAPON transistors are connected to both the Gnd and

Vdd. This connection ensures that the transistors operate in the active region throughout the operation cycles, which is crucial for their function as leakage-control devices.

- Lowering Leakage Current: The SAPON transistors lower the beneath the threshold current that leaks during the equilibrium phase and the short contact leakage current throughout the transition phase by raising the opposing connecting Vdd and Gnd. To do this, a greater voltage dip across the transistors is produced, which lowers the current that passes through them.

- Simulation Results: Simulations have shown that the SAPON technique leads to a substantial reduction in power consumption for various logic gates, including inverters, NAND, NOR, and multiplexers. It has been demonstrated to consume 23% less power compared to traditional methods like LECTOR, LCNT, and STACK ONOFIC.

- Area Overhead: Despite its power reduction benefits, the SAPON technique has a comparable area overhead to other leakage control techniques, meaning it does not significantly increase the physical size of the circuit.

The SAPON technique is a viable strategy for creating VLSI designs with minimal power consumption, especially for applications where power efficiency is paramount, such as in battery-operated devices.

Introduction to DTMOS Technique:

The Dynamic Threshold Metal-Oxide-Semiconductor (DTMOS) technique is a methodology applied in the design of semiconductor devices aimed at enhancing performance and decreasing power usage. DTMOS operates by dynamically modifying the Vth of a MOSFET according to the operational circumstances. Such modification is generally accomplished by linking the body (substrate) of the MOSFET to its gate With the transistor switched off, the body effect elevates the threshold voltage, curtailing leakage currents and conserving energy. Conversely, when activated, the threshold voltage diminishes, boosting the drive current and optimizing performance.

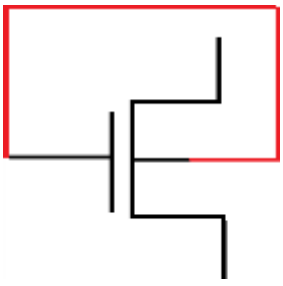

Fig3: Block diagram of DTMOS technique

Advantages of DTMOS

1. Energy Efficiency:

Decreased leakage currents in the off position contribute to diminished static power usage.

2. Boosted Performance:

Reduction in threshold voltage during activation facilitates quicker switching times and superior functionality.

3. Flexibility:

DTMOS adapts threshold voltage for varying power and performance needs

In SRAM Cells:

Within Static Random-Access Memory (SRAM) cells, DTMOS aids in attaining lower power utilization without sacrificing read/write capabilities. Body Bias Regulation**,** Accurate regulation of the body bias necessitates meticulous engineering to guarantee the advantages of DTMOS are leveraged without introducing reliability concerns.The DTMOS approach represents a sophisticated strategy for curbing power usage and augmenting performance in contemporary electronics. Through dynamic modulation of the threshold voltage in MOSFETs, DTMOS facilitates proficient energy management, proving invaluable in scenarios demanding a harmony between power conservation and peak performance.

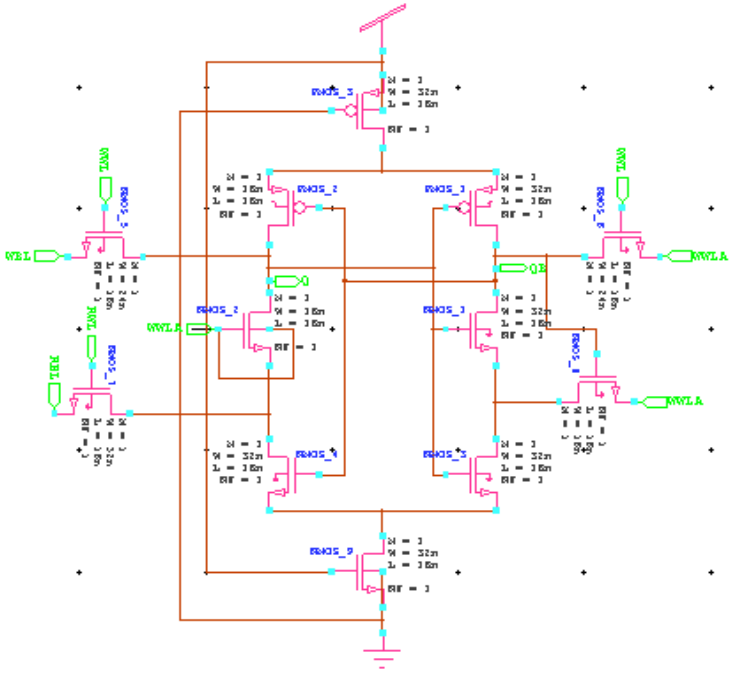

Fig4: Schematic of proposed SRAM using Sapon Technique & DTMOS Technique

V. RESULT AND ANALYSIS

The Results and Discussion portion offers a thorough assessment of the Proposed SRAM architecture, utilizing S-edit within Tanner EDA. Prior to proceeding with simulations, the design phase meticulously verified the schematic and connections for accuracy. Simulations were conducted through T-Spice, encompassing essential procedures such as integrating a technology file, setting the simulation duration, identifying input sources, and adding directives for computing power usage and latency. Initiation of the simulation was accomplished by selecting "run simulation."After the simulation concluded, a detailed inspection of the waveforms was undertaken to evaluate the Proposed SRAM structure's performance across different

scenarios. This scrutiny extended to a comprehensive review of MOSFET operation, power consumption levels, and delay times. Insights gleaned from the waveform analysis shed light on the dynamic characteristics of the proposed design, facilitating an in-depth evaluation of its operational efficiency and performance indicators.Analyzing MOSFET usage provided significant understanding regarding the efficiency and resource allocation within the engineered Flip-Flop (FF) structure. It was necessary to closely examine electrical usage levels in order to evaluate the suggested design's conservation of energy. In order to comprehend the adaptability and operating speed of the suggested 10T SRAM arrangement, delay factors were also examined.

The Results and Discussion segment provides an exhaustive examination of the suggested SRAM configuration., integrating simulation outcomes with insightful discussions to provide a holistic understanding of the design's performance and potential areasfor improvement.

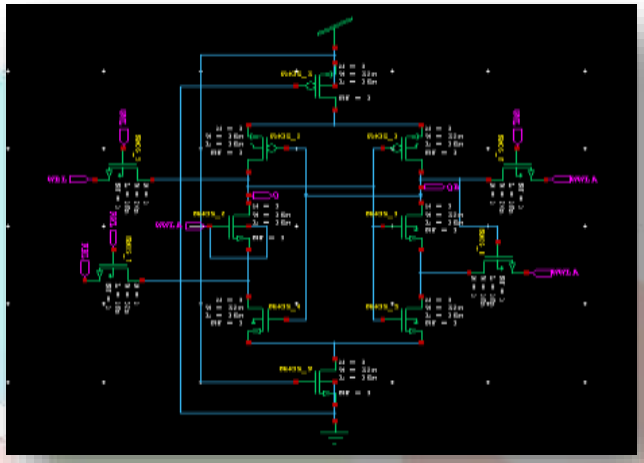

Fig 5: Schematic of proposed SRAM

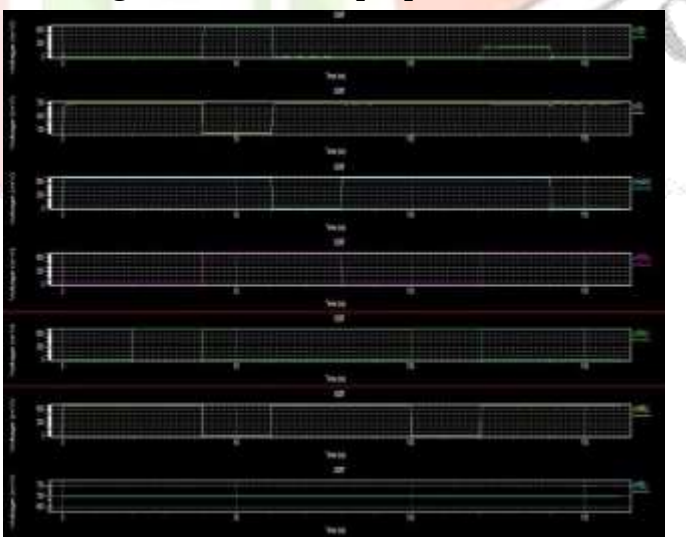

Fig 6: Simulation Waveforms

COMPARISION TABLE:

	Area	Power	Delay
Existing	10	5.125×10^{-8}	2.00×10^{-8}
Proposed	12	3.858×10^{-8}	1.503×10^{-10}

In existing method we design the 10T SRAM with access transistors, for strengthening the signal we add 2 transistors. While design the existing method the Power values is 5.125x10^-8 while we try to reduce the power, we use the low power technique as "Sapon approach and DTMOS technique". Using Sapon approach and DTMOS technique we have observed that Power got decreased trading area with constant delay.

VI. CONCLUSION

This study presents an enhanced SRAM cell design incorporating an extra sleep transistor, aimed at achieving reduced power consumption and increased stability. Our approach integrates both Sapon methodology and DTMOS technology within the traditional 10T SRAM circuit structure. Comparing the outcomes makes it evident that the suggested strategy offers lesser power consumption than the conventional SRAM circuit observing from simulated results obtained by Tanner EDA.

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