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Dynamic Clock Keeper For On-Chip Network Solving Synchronization Problems

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***Abstract*—** The emerging growth of the Internet of Things has created various opportunities to develop high-value, prioritized solutions in digital systems. A prime factor in achieving timing synchronization in high-stability digital devices is the need for a robust technical system with a stabilized clock. In low-energy satellite synchronization sources, there is a problem with frequency tuning, where the main system cannot cope with the evening process. The primary issue in existing frameworks for synchronization in network-on-chip creation is considered a timing problem and evaluated as a dynamic network. The presented system focuses on creating a stabilized network-on-chip model, in which clock synchronization is achieved using a frequency-tuneable all-digital network-on-chip. The configurable network concept framework is developed with the help of a stabilized clock distribution network. The percentage system of the clock is designed to compensate for the physical connections in the network. To evaluate the proposed system's performance and quality of network synchronization, power analysis and latency calculations are conducted.

Keywords— Network on chip, Configurable design, Digital design, Low power design, Dynamic networks.

I. INTRODUCTION

To reduce the number of data collision problems occurring at each node, the data packets received from the nodes are provided with a unique token, which passes through a ring topology. Heavy traffic is managed by centralizing the server to communicate with the nodes. Ring topology is utilized in the configurable network-on-chip devices, focusing on circular data alignment. To connect devices from one node to another for communication between data packets, the commonly utilized topology is ring topology. The presented approach addresses the drawbacks in the existing framework. A unidirectional ring network is used to provide wide directional data access and data formatting. Most ring topologies travel in a single direction and do not support multiple directions.

The major disadvantage of the proposed ring topology is that whenever the connections break, communication is impacted. In many cases, ring topology is utilized in local area networks to connect various nodes locally with low-level configurations. Depending on the number of nodes, the adopted topology determines the type of connecting network created. In a ring topology network, a coaxial cable-based RJ-45 cable is used for network connectivity.

Network-on-chip is a process of implementing network nodes into a single silicon wafer to communicate with various features inside a very high-speed integrated circuit. In many cases, large-scale designs are not preferred for all kinds of applications. In certain conditions, a single chip is preferred to implement various applications into a single wafer. The large-scale design networks are configured with the network-on-chip concept; thus, only the required modules are configured by the network, while other modules are ignored. This allows for multipurpose processing to be implemented on a single silicon platform.

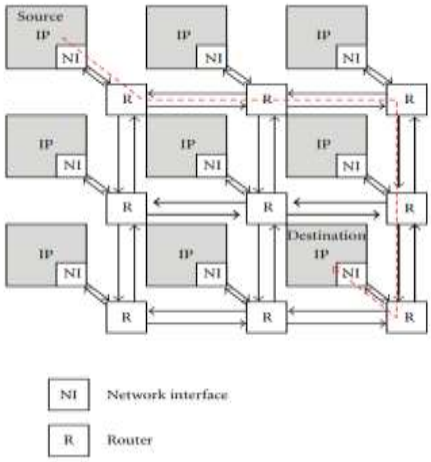

Fig 1. Network on Chip organization

In order to improve network performance, various multi-processing systems are implemented in the core network processing area. The development of general-purpose processors required for software networks is significantly enhanced in various applications, providing development and network customization to support layer-based configuration. As the density of VLSI design systems increases, the complexity of operations and the switching of transistors also significantly increases. To accommodate a large density of transistors with high frequencies and shorter operating path loops, a multi-processor on-chip system and multi-processor architecture are evaluated. To facilitate on-chip communication integrated with various heterogeneous functions, the semiconductor industry focuses on creating multi-processors with a network-on-chip architecture.

The rest of the paper is organized as detailed literature study discussed in Section II, followed with proposed design methodology is discussed in Section III. The obtained results after the simulation of proposed architecture is explored in Section IV. The paper is concluded with future work and comparison of statistical parameters.

II. BACKGROUND STUDY

Yang et al. (2018) The work presents a unique design for the functionality of network-on-chip implementation using an arbitration method, which provides on-demand high-speed utilization and resonant wavelength with network configuration. According to simulations of network-on-chip performance, the proposed system considers the packet size tunable facility to provide authenticated multi-processing traffic patterns. The system focuses on reducing waveguides and analyzing ultra-low power applications to provide high power efficiency.

Seitanidis et al. (2018) The author presented the development of a complex power consumption model for on-chip systems, emphasizing primary design constraints to accurately estimate the role of power consumption in altering digital circuits and measuring system performance. This was achieved by implementing low-cost, long battery life, and reliable digital systems. The proposed approach focuses on a high-level methodology to provide data patterns that consume more power in the network-on-chip. Power consumption is evaluated by making the system reconfigurable, resulting in 4x and 8x higher power consumption based on frequency to trigger the data patterns.

Cheng et al. (2018) The author presented a fault detection system for diagnosing data errors in network-on-chip operations. Various latency overhead problems and slicing of digital packets were developed to diagnose the repairing process and detect data faults. Latency overhead produced by channel slicing in long packets is utilized in network concept devices. The exit conductor detects gate faults by comparing them with the existing state-of-the-art processes. Additionally, various faults present in the router circuits are detected and evaluated. Low logic devices, achieving 64% energy efficiency, are integrated to enhance the reliability of energy efficiency.

D. Xu et al. (2023) As fabrication scales down to nano-level, compressing logical circuits inside miniature chips becomes increasingly complex. To address this challenge, developers focus on creating reliable network-on-chip devices equipped with fault-tolerant routing algorithms. This strategy aims to efficiently manage high congestion and prevent device failures, crucial for network concept design. The design significantly reduces channel functions and responds to network conditions to ensure that packets from failed links do not disrupt normal operations. To achieve a robust network concept, the presented system features three configurable multifunctional channels for network-on-chip development on ships.

Keeping various existing drawbacks discussed in the background study the primary reason for clock errors and non-synchronization is due to the unstable operating clock, fast flowing clock signals, unexpected glitches occurring in the clock signals etc.

To evaluate a model focus on stabilized network on chip community, then a dynamic clock keeper circuit is required.

III. PROPOSED METHODOLOGY

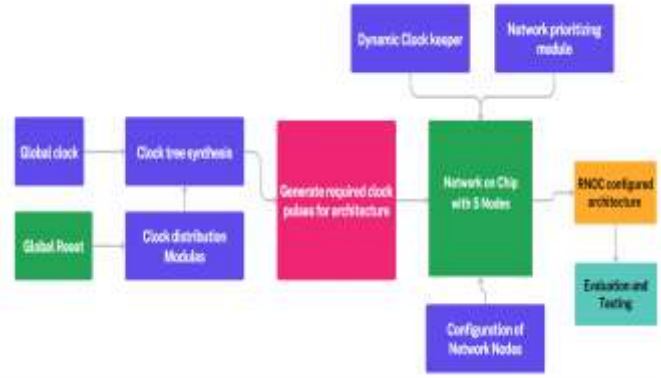

Fig 2. Proposed NOC model

Fig 2. Shows the proposed reconfigurable network on chip design. The figure illustrates the proposed network-on-ship architecture, which is organized with five different nodes. Each node is connected to a dedicated clock distribution network that controls the flow within the network-on-ship. A reference clock generates the required timing for synchronization. The stable architecture shows interconnected nodes with specific configurations that facilitate uninterrupted communication among processing elements in the network-on-ship.

Processing elements are linked via data encapsulation, allowing only single packets to pass according to priority and application requirements. Each node operates within a finite state machine concept, ensuring all submodules synchronize with the main model. Configuration bits maintain connectivity and enhance performance, enabling nodes to communicate efficiently even if connectivity is disrupted. Nodes prioritize communication paths based on node priority, minimizing interruptions and enhancing overall network stability.

Each network node holds a different application circuit implemented inside the single FPGA. The application circuits are getting tuned through configurable connections evaluated. The dynamic clock keeper proposed here keeps the monitoring strategy towards the network nodes, hence the synchronization issue is reduced. The dynamic clock is tuneable through clock distribution network. From the 40Mhz operating clock considered here, the clock distributor generates a frame of 20 different clock signals. The global reset will clear the FPGA hardware completely. The dynamic clock keeper get tuned with clock distributor circuit hence the clocks generated from the distributor is enabled through low level configurations such as 8 bit or 4 bit.

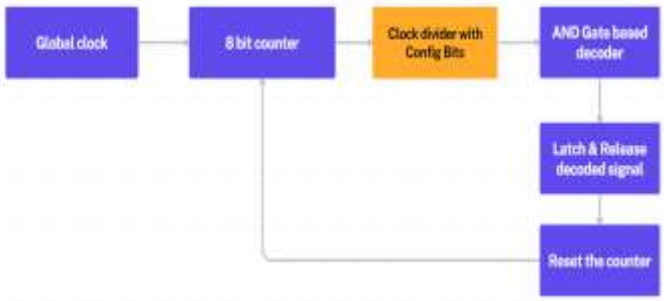

Fig 3. Configurable clock circuit

Fig 3. Shows the configurable clock circuit. From the global clock generated from the crystal oscillator, the 8 bit dedicated counter is developed to generate required clocks. The configuration bit control the decoder positions. The AND gate based simple decoder is configured here in which the generated clocks are hold with respect to clock signal and released to control the counter operation.

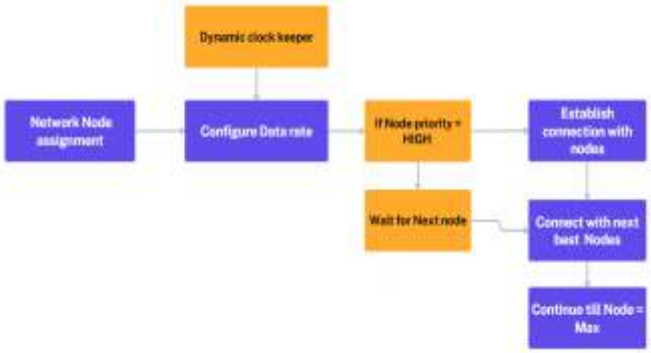

Fig 4. Data packing mechanism

Fig 4. Shows the data packing mechanism evaluated in the proposed model. If the node priority is high then the node connectivity is established. The network nodes and its priority is always kept dynamic and altered through simple configurations.

IV. RESULTS AND DISCUSSIONS

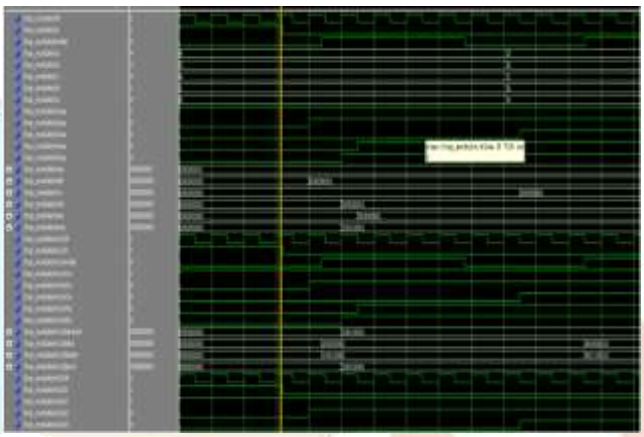

Fig 5. Configurable network nodes

Fig 5. Shows configurable network nodes associated in the proposed network on chip model.

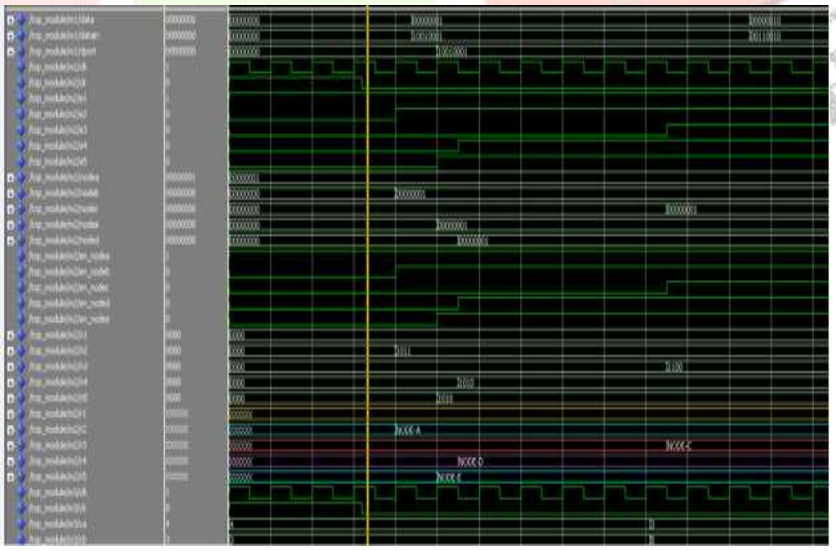

Fig 6. Generation of control mechanism

Fig 5. Shows generation of control mechanism with dynamic clock keeper continously generates and validates the stabilized clock signals flowing into the architecture.

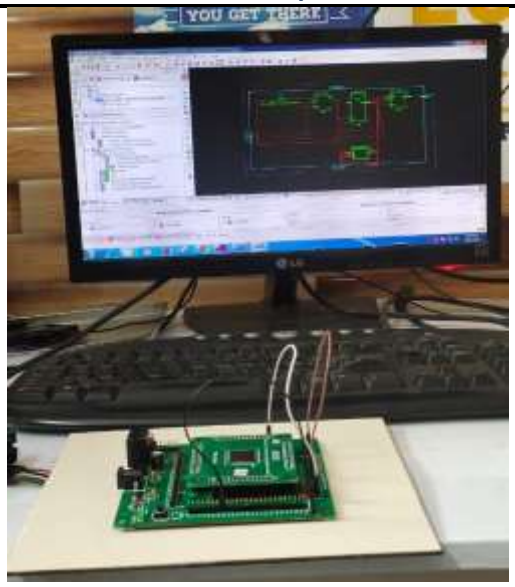

Fig 6. The test set up of proposed Dynamic Clock keeper

Fig 6. Shows the hardware implementation process connected with XILINX XC95144XL coolrunner CPLD family is dumped with the dynamic clock keeper and configurable network on chip design. The hardware works with 40MHz crystal oscillator. The reconfiguration bits are assigned with the jtag switches connected with 4-bit configuration. The configuration generates adoptive clock signals stabilized without clock glitches, electrical spikes, jitter and clock skews. The integrated hardware result depicts the network on chip communication with stabilized clock and without the dynamic clock keeper.

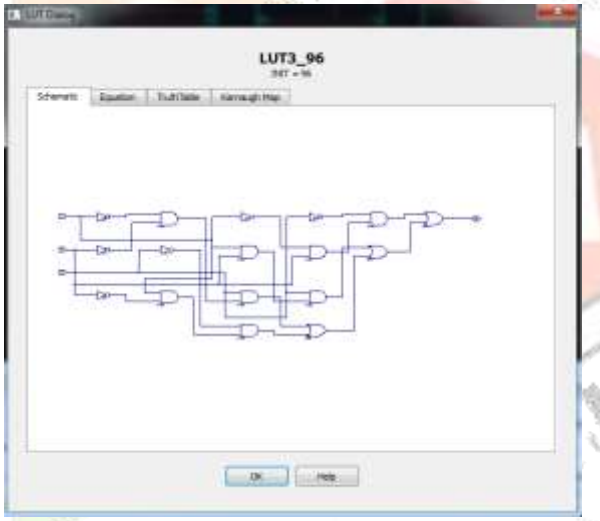

Fig 7. LUT internal design

Fig 7. Shows the LUT internal structure generated by the XILINX ISE software after the completion of synthesis process.

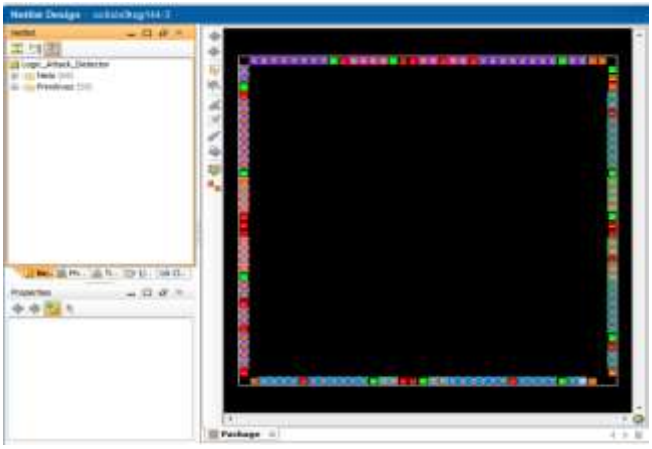

Fig 8. Chip configurations

Fig 8. Shows the chip configuration and its internal view of XC95144XL IC after the implementation using Plan Ahead tool.

TABLE 1 PERFORMANCE MEASURE

Parameters	Existing System (F.Shi et al. 2022)	Proposed approach
Network Nodes	24	25
Time Resolution	1us	1us
max time error	19us	15ns
Method	Delay compensation	Dynamic Clock keeper
Chip	cc2530	XC95144xl

TABLE 1. shows the performance measure of proposed dynamic clock keeper with respect to the existing model developed using delay compensation circuit.

V. CONCLUSION

Network-on-chip involves integrating network nodes into a single silicon wafer to facilitate communication among various features within a high-speed integrated circuit. Large-scale designs may not be suitable for all applications, making a single-chip approach preferable in certain scenarios. The system presented focuses on establishing a stable network-on-chip model, employing frequency-tunable all-digital technology for clock synchronization. A configurable network framework is developed using a stabilized clock distribution network, with the clock system designed to compensate for physical network connections. To assess the system's performance and network synchronization quality, power analysis and latency calculations are performed. The proposed method achieves a maximum timing error of 19 ns.

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