



HYBRID POWER OPTIMIZATION STRATEGIES FOR RECONFIGURABLE ALUs

¹R. SREEJA, ²Dr. T. SOMASSOUNDARAM

¹M. Tech Student, ²Professor (Guide) & HOD

¹Electronics and Communication Engineering (VLSI Design)

²Electronics and Communication Engineering (VLSI Design)

¹SRI VENKATESWARA COLLEGE OF ENGINEERING AND TECHNOLOGY(AUTONOMOUS)

²SRI VENKATESWARA COLLEGE OF ENGINEERING AND TECHNOLOGY(AUTONOMOUS)

Abstract:

Reduction in power dissipation is an essential design issue in VLSI circuit. One of the important blocks in any processor is Arithmetic Logic Unit and it performs arithmetic and logical operations. If operations are more and more complex, then power dissipation is more. The clock network is a major source of power dissipation so we can reduce significant amount of power if we can gate the clock whenever it isn't required. From the literature, we have noticed that there several methods/techniques used to reduce the power within ALU, the used methods are moderate and still there is scope to reduce power using blend of techniques. So low power ALU is designed using clock gating techniques besides using PIPO and Booth's algorithm concept. By giving specific opcode, we can enable the specific operation and other operations are in inactive mode, so we can see less power dissipation in ALU. Low power ALU is having two 8 bit input data with cin, bin, enable and 2 bit shift data and a decoder 4:16 to select the 16 operations by giving 4 bit opcode to it as a input with start enable function. At each iteration the proposed design is implemented with one of these clock gating techniques i.e latch free clock gated technique, latch based clock gated technique, flipflop based clock gated technique, and synthesis based clock gating technique with parallel in parallel out (PIPO) shift registers. These all techniques are performed with operation selection feature and PIPO shift registers in this design.

Key words: —Dynamic power, Register Transfer Level, clock gating

I. INTRODUCTION:

Reduction in power dissipation is an essential design issue in VLSI circuit. Few decades back designers mostly focus on area, delay and testability to optimize. While technology scaling down, we can see more power leakage and dissipation in chip. In order to reduce power dissipation and leakage power while scaling, we need to adopt the optimize techniques like clock gating, voltage scaling etc. Now a days designers are focusing in four dimensions to build any application. Those are four dimensions are area, delay, testability and power. For any application, consumers expect light weight, early response and not getting hot. For example consumers expect mobile as light weight with multiple operations and quick response. For multiple operations, we need to integrate multiple ICs into one chip. These causes more power consumption and phone getting hot and also area increases.

For reducing area, we are scaling down technology but we can see power dissipation more and chip may getting hot. For maintaining cool system, quick response and less area, we need to go for low power techniques. Fig. 1. Four dimensions to Optimize VLSI chip Power is the combination of static power dissipation and dynamic power dissipation. Static power dissipation will occur when circuit in off condition. As technology scales down, static power dissipation becomes more and more important in terms of leakage power. Leakage power due to drain induced barrier lowering (DIBL), channel punch through, hot electron effect, reverse bias source/drain junction leakages and etc. Dynamic power dissipation occurs when the

charging and discharging occurs at output capacitance in particular node and also at operating frequency. We can see dynamic power dissipation when signal transitions happens at that particular node otherwise we can't see dynamic power dissipation. Switching activity is mainly responsible for dynamic power consumption which is related to clock signal.

In our proposed work, we mainly focused on dynamic power dissipation and it reduced by making less signal activities in proposed design. The clock network is a major source of power dissipation so we can reduce significant amount of power if we can gate the clock whenever it isn't required. By using operation selection, we can make active specific operation only and other operations are in inactive mode then we can't see signal transitions in other operations so we can get less dynamic power dissipation when operation selection instruction used. In the previous decades, the real test for the VLSI architect was region, execution, cost and power utilization. As of late, in any case, this has started to change and, progressively control utilization is being given practically identical weight to region and speed contemplations. The thoughts for lessening power utilization vary from application to application and circuits to circuits. In the zone of small scale controlled battery worked compact applications, for example, mobile phones, the objective is to keep the battery lifetime and weight sensible and bundling cost low.

Scaling of CMOS gadgets has empowered the semiconductor business to take care of its demand for higher execution and higher coordination densities. However as the component measure gets to be distinctly littler, in light of short direct lengths it brings about expanded sub-threshold leakage current through a transistor when it is off condition. Another purpose behind expanded sub-threshold leakage current is that, transistors can't be turned off totally. Henceforth leakage control dissipation has turned into a vital bit of the aggregate power utilization for silicon innovations. The significant three plan parameters are power, speed and area. In CMOS VLSI circuits, control dissipation is basically because of the three essential elements: dynamic, static and short out.

II. EXISTING METHOD:

Power consumption optimization is crucial in VLSI circuits, particularly for the Arithmetic Logic Unit (ALU), a key processor component. The ALU performs arithmetic and logic operations, which directly impact energy use. The network clock is a major energy source, and turning it off when not needed can save significant energy.

One method to reduce power consumption involves using clock gating along with Parallel Input Parallel Output (PIPO) registers and the Booth algorithm to create a low-power ALU. Special opcodes perform operations while disabling others, using inputs like carry (cin), borrow (bin), enable signals, and 2-bit data transfers. A 4:16 decoder selects one of 16 operations using a 4-bit opcode. Clock gating turns off the clock signal when parts are inactive, reducing power loss from switching transistors. This is effective for flip-flops storing intermediate values or control signals, cutting unnecessary switching. PIPO registers store input data and intermediate results, speeding up ALU performance by processing data in parallel.

The Booth algorithm reduces the number of required arithmetic operations, particularly useful for dividing signed binary numbers, and encoding multipliers to minimize additions. Using clock gating, PIPO registers, and the Booth algorithm, the ALU can reduce power consumption, improve performance, and extend battery life for portable devices.

The proposed design uses various clock gating techniques with PIPO shift registers, tested at frequencies from 100MHz to 1GHz on a Virtex-6 FPGA with 40nm technology. This approach aims to analyze dynamic power dissipation in ALUs with and without clock gating, combining PIPO and the Booth algorithm.

Existing techniques for power optimization in configurable ALUs include gate-level optimization (using low-power gate structures), circuit-level optimization (voltage and current scaling, threshold voltage adjustment), power gating (shutting down inactive parts), clock gating, data encoding (reducing switching activity), and architectural optimizations (using low-power components and efficient data transfer methods).

These techniques vary in effectiveness based on ALU design and application. Combining them can achieve optimal power optimization. Circuit-level methods include voltage scaling (lowering supply voltage), current scaling (adjusting bias currents), and threshold voltage adjustment (reducing leakage currents). Dynamic voltage scaling adjusts supply voltage based on workload, while leakage power reduction techniques minimize static power dissipation.

Architectural optimizations involve designing system architecture to reduce power while maintaining performance. Dynamic Voltage and Frequency Scaling (DVFS) adjusts operating voltage and frequency based on system needs, saving power during low activity and boosting performance during high activity. Efficient communication and data transfer methods reduce power by minimizing data movement and using energy-saving encoding.

Low-power ALUs combine clock gating, PIPO registers, and the Booth algorithm to enable specific operations while keeping others inactive, reducing power dissipation. Various clock gating techniques, tested at different frequencies, aim to optimize dynamic power consumption in ALUs. Combining power and clock gating can effectively reduce both dynamic and leakage power in digital CMOS circuits.

III. PROPOSED METHOD:

Performance and Operation of ALU

The proposed work presents an 8-bit Arithmetic and Logic Unit (ALU) that performs various arithmetic and logical operations, including addition, subtraction, multiplication, division, AND, NAND, OR, NOR, XOR, XNOR, arithmetic and logical shifts, 1's complement, and 2's complement. Multiplication and division operations utilize Booth's algorithm. The ALU design features a Parallel Input Parallel Output (PIPO) register using low-power D flip-flops, which are based on the master-slave concept of D latches.

The ALU design is simulated using the Xilinx 14.4 simulator and implemented on a Virtex-6 FPGA. Power analysis is conducted with the Xpower Analyzer. The results, including opcodes for enabling specific instructions, are detailed in the results section.

Different Clock Gating Techniques

Clock gating techniques focus on reducing dynamic power dissipation. The techniques explored include latch-free clock gating, latch-based clock gating, flip-flop-based clock gating, and synthesis-based clock gating in a 16-bit ALU. These techniques are applied to operations such as addition, subtraction, increment, decrement, NOR, XOR, XNOR, AND, NAND, OR, complement, and shift operations. Dynamic power dissipation is analyzed for various frequencies.

1. Latch-Free Clock Gating Technique:

- Uses basic gates like AND or NOR for clock gating.
- Main drawback: glitches in the gated clock signal if the enable signal is not synchronized with the clock.

2. Latch-Based Clock Gating Technique:

- Solves glitches in latch-free designs by controlling the enable signal with a latch.
- Gated clock becomes high only when the system clock and latch output are both high.

3. Flip-Flop Based Clock Gating Technique:

- Utilizes flip-flops to store the enable signal and synchronize the gated clock signal with the main clock.
- Combinational logic gates like AND or NAND gates control the clock gating.

4. Synthesis-Based Clock Gating Technique:

- Uses hardware description language tools to automatically add clock gating logic during the design process.
- Optimizes power consumption without affecting performance.

5. Detailed Implementation Results

The ALU design incorporates various clock gating techniques and is analyzed for dynamic power dissipation on a Virtex-6 FPGA. Two specific techniques, flip-flop-based and negative latch-based clock gating, show significant power reduction by restricting clock signal transitions. Negative latch-based clock gating demonstrates lower dynamic power dissipation compared to flip-flop-based clock gating.

6. Power Optimization Techniques

For dynamic power dissipation, D flip-flop-based clock gating is used. For static power dissipation, the leakage control transistor (LECTOR) technique is employed in AND gates after the D flip-flop. These combined techniques aim to reduce both dynamic and static power consumption in the ALU design.

IV. ADVANTAGES:

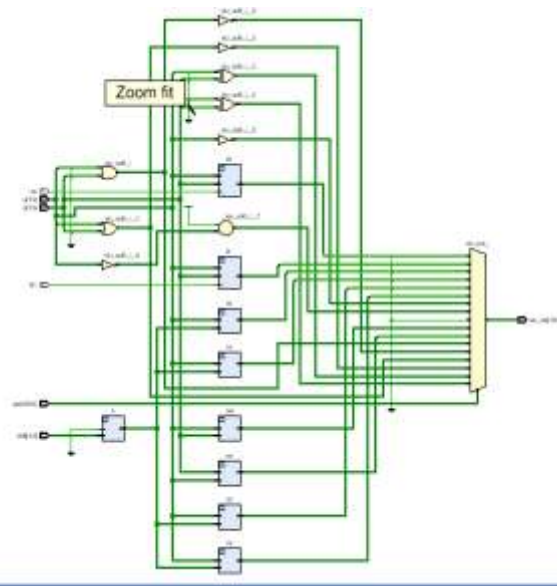
- ❖ **Reduced Power Consumption:** Significant reduction in power consumption through various optimization strategies, leading to energy savings.
- ❖ **Longer Battery Life:** Crucial for battery-powered devices like mobile phones, laptops, and IoT devices, enhancing usability and portability by achieving longer battery life.
- ❖ **Enhanced Performance:** Faster execution times and improved throughput through performance optimization, allowing efficient computations without sacrificing performance.
- ❖ **Flexibility and Adaptability:** Ensures adaptability and efficiency across different computational tasks, allowing dynamic reconfiguration and efficient utilization of hardware resources.
- ❖ **Scalability:** Enables scalable ALU design while keeping power consumption under control, crucial as the complexity and size of the ALU increase.
- ❖ **Reliability and Thermal Management:** Mitigates thermal issues and enhances overall system reliability by ensuring ALU operates within acceptable temperature ranges.
- ❖ **Cost Savings:** Reduces power consumption, potentially requiring a smaller power supply, leading to cost savings in power management components, cooling systems, and overall system design.

V. APPLICATIONS:

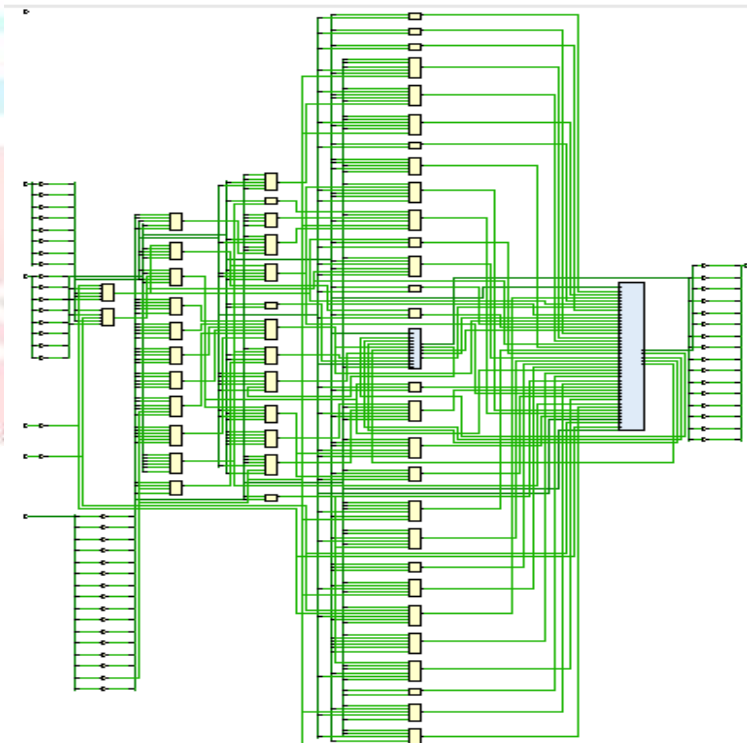
- ❖ **Mobile Devices:** Essential for smartphones, tablets, and wearables to achieve longer battery life, enabling extended usage and better user experience.
- ❖ **Internet of Things (IoT):** Crucial for energy-efficient operation and maximizing lifespan of IoT devices, reducing the need for frequent battery replacements or recharging.
- ❖ **Embedded Systems:** Critical in automotive, aerospace, industrial automation, and healthcare applications for efficient operation while meeting power constraints and ensuring reliable performance.
- ❖ **Data Centers:** Helps reduce overall energy consumption, achieve higher computational efficiency, reduce electricity costs, and minimize environmental impact.
- ❖ **High-Performance Computing (HPC):** Balances performance and power consumption in power-limited HPC systems, achieving higher energy efficiency and reducing operating costs.
- ❖ **Automotive Electronics:** Maximizes vehicle battery life and ensures reliable operation of electronic systems, including infotainment and advanced driver assistance systems (ADAS).
- ❖ **Portable and Wearable Devices:** Enables extended usage and improved user experience for laptops, tablets, and wearable devices by optimizing power consumption for longer battery life and better mobility.

VI. RESULTS:

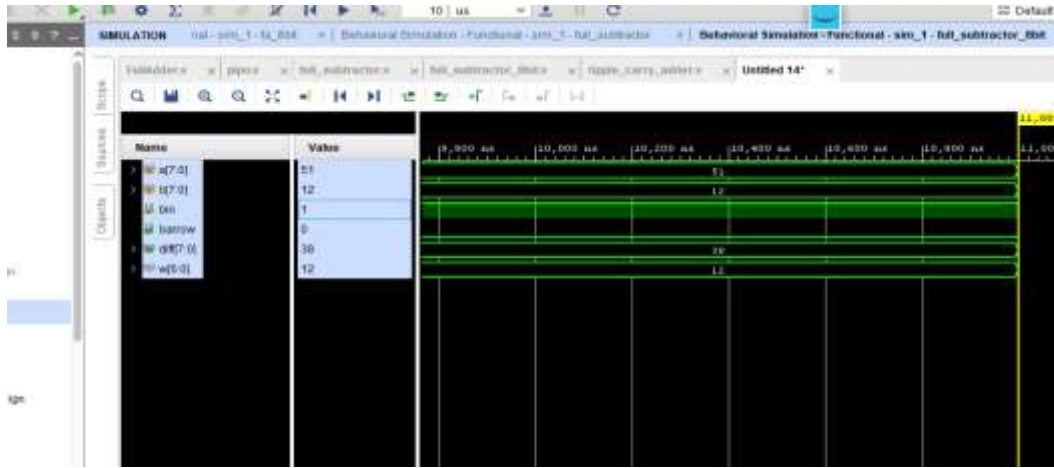
RTL Schematic:



Technology schematic:



Simulation:



Area:

Name	Slice LUTs (134600)	Slice (33650)	LUT as Logic (134600)	Bonded IOB (400)
ALU	353	101	353	50
m0 (booth_mul)	169	50	169	0
m1 (booth_div)	144	49	144	0

Delay:

Max Delay Paths

```
Slack: inf
Source: b[1]
        (input port)
Destination: alu_out[0]
              (output port)
Path Group: (none)
Path Type: Max at Slow Process Corner
Data Path Delay: 32.568ns (logic 14.980ns (45.996%) route 17.588ns (54.004%))
Logic Levels: 43 (CARRY4=21 IBUF=1 LUT2=7 LUT3=7 LUT4=1 LUT6=5 OBUF=1)
```

Power:

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

Total On-Chip Power: 5.928 W
Design Power Budget: Not Specified
Power Budget Margin: N/A
Junction Temperature: 36.1°C
 Thermal Margin: 48.9°C (25.8 V)
 Effective θ JA: 1.9°C/W
 Power supplied to off-chip devices: 0 W
 Confidence level: Low

[Launch Power Constraint Advisor](#) to find and fix invalid switching activity

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 10.437 W
Design Power Budget: Not Specified

Power estimation from Synthesized netlist. Activity derived from constraints files, simulation files or vectorless analysis. Note: these early estimates can change after implementation.

Total On-Chip Power: 444.893 W (Junction temp exceeded!)

Evaluation table for Area, Delay:

Name	^ ₁ Slice LUTs (134600)	Slice (33650)	LUT as Logic (134600)	Bonded IOB (400)
ALU	353	101	353	50
m0 (booth_mul)	169	50	169	0
m1 (booth_div)	144	49	144	0

VII. CONCLUSION

Power optimization in configurable ALU using blend of techniques presents a comprehensive investigation into reducing power consumption in a configurable Arithmetic Logic Unit (ALU) through the application of various techniques. The goal of the research is to address the increasing demand for low-power designs in modern computer systems. The paper explores a range of power optimization techniques, including gate-level optimization, circuit-level optimization, and algorithmic optimization. These techniques are combined in a blended approach to achieve significant power savings while maintaining the desired functionality of the ALU.

The results of the study demonstrate the effectiveness of the proposed power optimization techniques. By carefully analyzing and optimizing the ALU design at different levels, the researchers were able to achieve substantial reductions in power consumption without compromising the performance of the ALU.

VIII. REFERENCES

- [1] B. Geetha, B. Padmavathi, and V. Perumal, "Design methodologies and circuit optimization techniques for low power cmos VLSI design," in 2017 IEEE International Conference on Power, Control, Signals and Instrumentation Engineering (ICPCSI), IEEE, 2017, pp. 1759–176.
- [2] B. Padmavathi, B. Geetha, and K. Bhuvaneshwari, "Low power design techniques and implementation strategies adopted in vlsi circuits," in 2017 IEEE International Conference on Power, Control, Signals and Instrumentation Engineering (ICPCSI), IEEE, 2017, pp. 1764–1767
- [3] U. Kaur and R. Mehra, "Low power cmos counter using clock gated flip-flop," Int. J. Eng. Adv. Tech, vol. 2, pp. 796–8, 2013Pratibhadevi Tapashetti, Dr.Rajkumar B Kulkarni and Dr.S S Patil, " MAC Architectures Based on Modified Booth Algorithm", International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, Vol. 5, Issue 12, pp. 2320 – 3765, December 2016.

- [4] M. P. Dev, D. Baghel, B. Pandey, M. Pattanaik, and A. Shukla, "Clock gated low power sequential circuit design," in 2013 IEEE Conference on Information & Communication Technologies, IEEE, 2013, pp. 440–444.
- [5] R.UMA, Vidya Vijayan and M. Mohanapriya, "Area, Delay and Power Comparison of Adder Topologies" International Journal of VLSI design & Communication Systems (VLSICS) Vol.3, No.1, February 2012, in-press.
- [6] G. Shrivastava and S. Singh, "Power optimization of sequential circuit based alu using gated clock & pulse enable logic," in 2014 International Conference on Computational Intelligence and Communication Networks, IEEE, 2014, pp. 1006–1010.
- [7] R. N. A. Shiny, B. Fahimunnisha, S. Akilandeswari, and S. J. Venula, "Integration of clock gating and power gating in digital circuits," in 2019 5th international conference on Advanced Computing & Communication Systems (ICACCS), IEEE, 2019, pp. 704–70

